Service Manual

Tektronix

2430
Digital Oscilloscope

070-4917-00

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to the Safety Summary prior to performing service.

Please check for change information at the rear of this manual.

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OPERATORS SAFETY SUMMARY

The general safety information in this part of the summary is for both operating and servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply and do not appear in this summary.

Terms in This Manual

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

Terms as Marked on Equipment

CAUTION indicates a personal injury hazard not immediately accessible as one reads the markings, or a hazard to property, including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

Symbols in This Manual

⚠ This symbol indicates where applicable cautionary or other information is to be found. For maximum input voltage see Table 1-1.

Symbols as Marked on Equipment

ϟ DANGER — High voltage.

⏚ Protective gound (earth) terminal.

⚠ ATTENTION — Refer to manual.

Power Source

This product is intended to operate from a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Grounding the Product

This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before making any connections to the product input or output terminals. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Danger Arising from Loss of Ground

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulated) can render an electric shock.

Use the Proper Power Cord

Use only the power cord and connector specified for the instrument.

Use the Proper Fuse

To avoid fire hazard, use only the fuse specified in the instrument parts list. A replacement fuse must meet the type, voltage rating, and current rating specifications for the fuse that it replaces.

Do Not Operate in Explosive Atmospheres

To avoid explosion, do not operate this instrument in an atmosphere of explosive gasses.

Do Not Remove Covers or Panels

To avoid personal injury, the instrument covers or panels should only be removed by qualified service personnel. Do not operate the instrument without covers and panels properly installed.

SERVICING SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

Refer also to the preceding Operators Safety Summary.

Do Not Service Alone

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

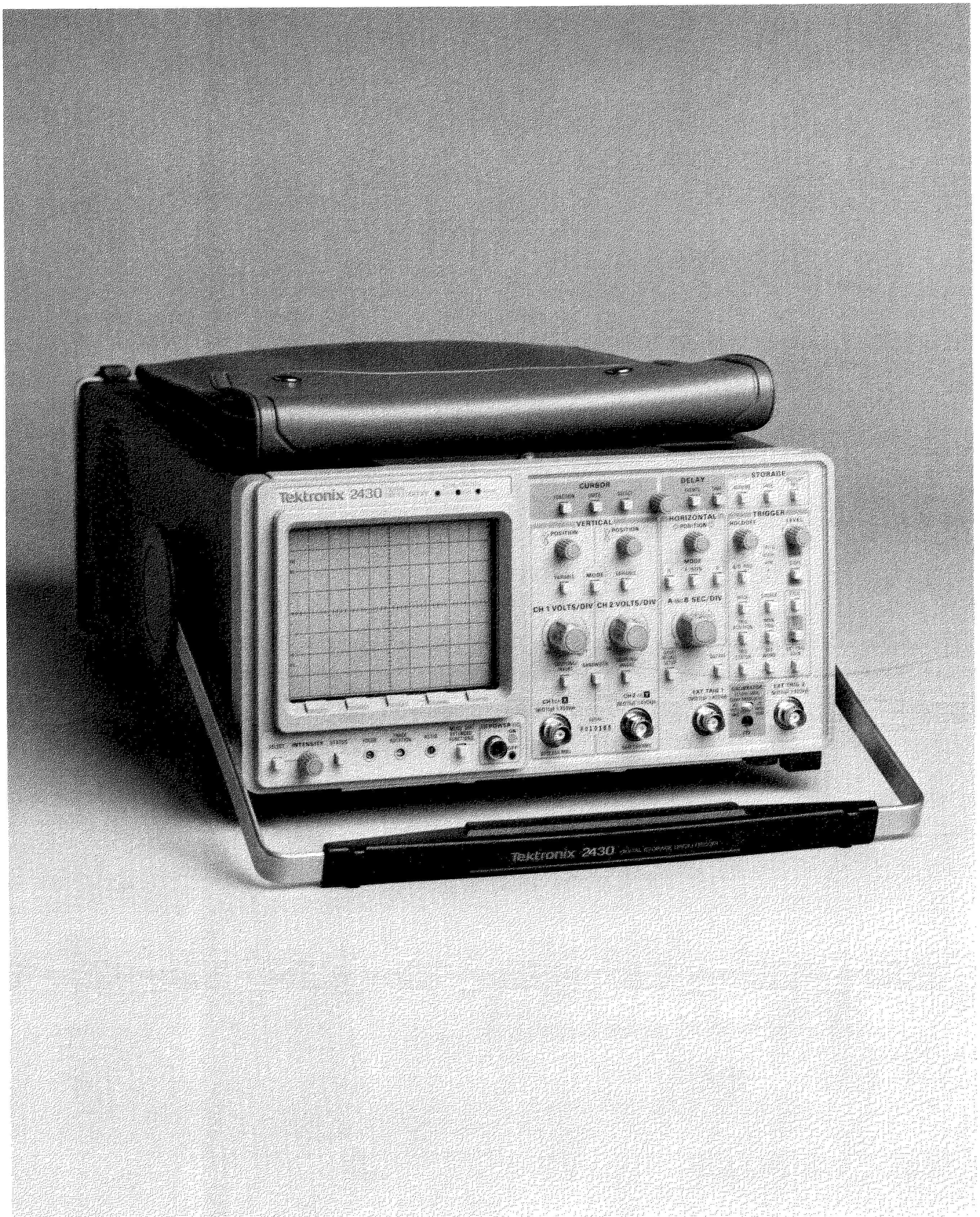
Use Care When Servicing With Power On

Dangerous voltages exist at several points in this product. To avoid personal injury, do not touch exposed connections or components while power is on.

Disconnect power before removing protective panels, soldering, or replacing components.

Power Source

This product is intended to operate from a power source that does not apply more than 250 volts rms bwetween the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding connector in the power cord is essential for safe operation.



4917-01

The 2430 Digital Oscilloscope.

SPECIFICATION

INTRODUCTION

The TEKTRONIX 2430 Digital Oscilloscope is a portable, dual-channel instrument with a maximum digitizing rate of 100 megasamples per second. The instrument is microprocessor controlled, menu driven, and displays crt readouts of the vertical and horizontal scale factors, trigger levels, trigger source, and cursor measurements. Menu-driven modes of the instrument are selected by pressing a bezel button under the menu choices displayed at the bottom of the crt. Selection of a mode is indicated by an underscoring of the menu choice in the display. The menus, system operating modes, and auxiliary functions are described in Section 3 of the Operators Manual, "Controls, Connectors, and Indicators."

The 2430 is capable of simultaneous acquisition of the Channel 1 and Channel 2 input signals. It has a real-time useful storage bandwidth of 40 MHz for single-event acquisitions and an equivalent-time bandwidth of 150 MHz for repetitive acquisitions. Since both channels are acquired simultaneously, the XY display is available to full bandwidth.

The two vertical channels have calibrated deflection factors from 2 mV to 5 V per division in a 1-2-5 sequence of 14 steps. Use of coded probes having attenuation factors of 1X, 10X, 100X, and 1000X extends the minimum sensitivity to 5,000 V per division (with the 1000X probe) and the maximum sensitivity to 200 μV per division (using a 1X probe in SAVE or AVERAGE expanded mode). VOLTS/DIV readouts are automatically switched to display a correct scale factor when properly coded probes are attached.

Horizontal Display Modes of A, A INTEN, and B Delayed are available. Two types of delay operation are available: B Delayed by Time and A Delayed by Events. The time base has 28 calibrated SEC/DIV settings in a 1-2-5 sequence from 5 ns per division to 5 s per division. An External Clock Mode is provided that accepts clocking signals from 1 MHz to 100 MHz.

A choice of VERT, CH1 or CH2, EXT1 or EXT2, LINE, and A*B or WORD (16-bit data word recognition) for the A Trigger signal SOURCE provides a wide range of specialized triggering capabilities. The B Trigger SOURCE choices are similar to the A Trigger SOURCE, but exclude A*B (A and B both) and LINE (power-source frequency). Trigger CPLG selections are AC, DC, HF REJ, LF REJ, and NOISE REJ. The Trigger LEVEL control amplitude setting is displayed in the crt readout. The Video Option adds a CPLG selection of TV that processes applied composite video signals for stable triggering. With the Video Option installed, the Trigger LEVEL control becomes the TV LINE number selector for FLD1 and FLD2 triggering.

Trigger MODE choices are AUTO LEVEL, AUTO (ROLL), NORM, and SINGLE SEQ (single sequence) for the A and A INTEN Horizontal Modes. Triggerable After Delay and Runs After Delay are provided for the B Horizontal Mode. AUTO LEVEL provides for automatic triggering on the applied trigger signal. AUTO Mode produces an auto trigger if a trigger signal is either not received within a defined time or is inadequate to produce a triggering event. When triggering conditions are met, normal triggering occurs. At SEC/DIV settings of 100 ms per division and slower, AUTO Mode becomes ROLL Mode. NORM (normal) Mode requires that the triggering signal meet all the triggering requirements before an acquisition trigger will be generated. In SINGLE SEQ Mode, a single complete acquisition is done on all called-up VERTICAL MODES, and the 2430 switches to the SAVE Mode.

The amount of pretrigger data displayed is selectable by choosing the trigger point position within the waveform record. Five pretrigger lengths are selectable, beginning at one-eighth of the record length and increasing to seven-eighths of the record length. Trigger position is independently selectable for the A and B acquisitions. Additional trigger positions within the record are selectable via the GPIB interface commands.

The record length of acquired waveforms is 1024 data points (512 max/min pairs in ENVELOPE Mode), of which 500 make up a one-screen display (50 data points per division for 10 divisions). The entire record may be viewed by using the Horizontal POSITION control to position any portion of the record within the viewing area.

Waveforms may be acquired in NORMAL, ENVELOPE, and AVG (averaging) Modes. NORMAL Mode provides a continuous acquisition display similar to that seen with an analog oscilloscope. AVG (averaging) Mode is especially useful for improving the signal-to-noise ratio of the displayed waveform by averaging from 2 to 256 acquisitions to remove uncorrelated noise. REPETITIVE Mode may be used in NORMAL and AVG Modes for equivalent-time sampling that extends the useful storage bandwidth to 150 MHz for recurring periodic signals.

The ENVELOPE Mode display presents a visual image of the amount of change (envelope) that occurs to a waveshape during the acquisition of from 1 to 256 waveforms. The continuous ENVELOPE Mode holds all changes in the display until reset by a control change. ENVELOPE Mode can capture single-event pulses (glitches) as narrow as 4 ns at the slowest SEC/DIV setting of 5 seconds per division.

Acquired waveforms may be saved in any of four REF waveform nonvolatile memories. Any or all of the saved reference waveforms may be displayed for comparison with the waveforms being currently acquired. The source and destination of waveforms to be saved may be user designated. Up to five front-panel control setups may be saved (when REF4 is designated for front-panel memory) in nonvolatile memory for recall at a later time.

Time and Voltage cursors are provided for making measurements on the displayed waveforms. Direct readout of the measured values are displayed on the crt. The cursors have alternate modes of readout operation for a choice of measurement types (i.e., volts at time, slope, frequency, absolute, dB, percent, degrees of phase, and delta measurements).

The 2430 has full TALKER/LISTENER GPIB capabilities that make the instrument ideal for making automated measurements in an installed system and a standard X-Y Recorder output for producing low-cost hard copies of acquired waveforms. The GPIB interface may also be used to drive a ThinkJet® printer to plot the acquired waveforms.

The following items are standard accessories shipped with the 2430 instrument:

- 2 Probe packages
- 1 Snap-lock accessories pouch
- 1 Zip-lock accessories pouch
- 1 Operators manual
- 1 Instrument Interface Guide
- 2 User Reference Guide
- 1 Fuse
- 1 Power cord (installed)
- 1 Blue plastic crt filter (installed)
- 1 Clear plastic crt filter
- 1 Front-panel cover

For part numbers and further information about standard accessories and a list of the optional accessories, refer to "Options and Accessories" (Section 7) either in this manual or in the Operators Manual. For additional information on accessories and ordering assistance, contact your Tektronix representative or local Tektronix Field Office.

PERFORMANCE CONDITIONS

The following electrical characteristics (Table 1-1) apply when the 2430 has been calibrated at an ambient temperature between +20°C and +30°C, has had a warm-up period of at least 20 minutes and is operating at an ambient temperature between −15°C and +55°C (unless otherwise noted).

Items listed in the "Performance Requirements" column are verifiable quantitative or qualitative limits that define the measurement capabilities of the 2430 Oscilloscope.

For optimum performance to specification, the 2430 SELF CAL may be done:

1. If the operating temperature has changed by more than 5°C since the last SELF CAL was done.

2. Immediately before making measurements requiring the highest degree of accuracy.

A complete adjustment procedure that includes the EXTENDED CAL and all the internal 2430 adjustments should normally be done after 2000 hours of operation or at one-year intervals if used infrequently.

Environmental Characteristics are given in Table 1-2. The 2430 meets the environmental requirements of MIL-T-28800C for Type III, Class 3, Style D equipment, with the humidity and temperature requirements defined in paragraphs 3.9.2.2, 3.9.2.3, and 3.9.2.4. The rackmounted 2430 meets the vibration and shock requirements of MIL-T-28800C for Type III, Class 5, Style D equipment when mounted using the rackmount rear-support kit supplied with both the 1R Option and the Rackmount Conversion kit.

Mechanical characteristics of the 2430 are listed in Table 1-3.

Video Option characteristics are given in Table 1-4.

Table 1-1

Electrical Characteristics

Characteristics	Performance Requirements
ACQUISITION SYSTEM—CHANNEL 1 AND CHANNEL 2	
Resolution	8 bits.[a] Displayed vertically with 25 digitization levels (DL)[b] per division, 10.24 divisions dynamic range.[a]
Record Length	1024 samples.[a] Displayed horizontally with 50 samples per division, 20.48-division trace length.[a]
Sample Rate	10 samples per second to 100 megasamples per second (5 s per division to 500 ns per division).
Sensitivity	
Range	80 μV per DL to 0.2 V per DL in a 1-2-5 sequence of 11 steps (2 mV per division to 5 V per division).
Accuracy	
Normal and Average Modes	Within ± (2% + 1 DL) at any VOLTS/DIV setting for a signal 1 kHz or less contained within ±75 DL (±3 divisions) of center when an Autocal has been performed within ±15°C of the operating temperature. Measured on a four- or five-division signal with VOLTS or V@T cursors; UNITS set to delta volts.
Envelope Mode	Add 1% to Normal Mode specifications.
Variable Range	Continuously variable between VOLTS/DIV settings. Extends sensitivity to 0.5 V per DL or greater, 12.5 V per division or greater.
Bandwidth	
Normal and Average Mode; Repet off; SEC/DIV at 0.5 μs or Faster	DC to 40 MHz (calculated useful storage bandwidth—USB).[a] $USB = \frac{F_{(sample\ freq\ max)}}{2.5}$
Normal and Average Modes with Repet On or Continuous Envelope Mode; SEC/DIV at 0.2 μs or Faster (−3 dB bandwidth)	DC to 150 MHz. Bandwidth with a P6131 probe is checked using the obtainable reference signal (six divisions or less) from a terminated 50 Ω system via probe-tip-to-BNC adapter.[a] Bandwidth with external termination is checked using a six-division reference signal from terminated 50 Ω system.[a] Bandwidth with internal termination is checked using a six-division reference signal from a terminated 50 Ω system.

[a]Performance Requirement not checked in the manual.
[b]"Digitization level" is abbreviated "DL" and is equal to 1/25 of a division times the vertical expansion factor.

Table 1-1 (cont)

Characteristics	Performance Requirements
AC Coupled Lower −3 dB Point	
1X Probe	10 Hz or less.[a]
10X Probe	1 Hz or less.[a]
Step Response, Repet and Average On; Average Set to 16	
Rise Time	2.3 ns or less (calculated).[a] $T_r \text{ (in ns)} = \frac{350}{\text{BW (in MHz)}}$
Envelope Mode Pulse Response	
Minimum Single Pulse Width for 50% or Greater Amplitude Capture at 85% or Greater Confidence	2 ns.[a]
Minimum Single Pulse Width for Guaranteed 50% or Greater Amplitude Capture	4 ns.[a]
Minimum Single Pulse Width for Guaranteed 80% or Greater Amplitude Capture	8 ns.[a]
Channel Isolation	100:1 or greater attenuation of the deselected channel at 100 MHz; 50:1 or greater attenuation at 150 MHz, for a 10-division input signal from 2 mV/div to 500 mV/div; with equal VOLTS/DIV settings on both channels.
Acquired Channel 2 Signal Delay with Respect to Channel 1 Signal at Full Bandwidth	±250 ps.[a]
Input R and C (1 MΩ)	
Resistance	1 MΩ ±0.5%.[a] In each attenuator, the input resistance of all VOLTS/DIV positions is matched to within 0.5%.[a]
Capacitance	15 pF ±2 pF.[a] In each attenuator, the input capacitance of all VOLTS/DIV positions is matched to within 0.5 pF.[a]

[a]Performance Requirement not checked in the manual.

Table 1-1 (cont)

Characteristics	Performance Requirements
Input R (50 Ω)	
Resistance	50 Ω ±1%.[a]
VSWR (DC to 150 MHz)	1.3:1 or better.[a]
Maximum Input Voltage ⚠	5 V rms; 0.5 W·sec for any one-second interval for instantaneous voltages from 5 V to 50 V.
Maximum Input Voltages ⚠	
Input Coupling Set to DC, AC, or GND	400 V (dc + peak ac); 800 V p-p ac at 10 kHz or less.[a]
Common-Mode Rejection Ratio (CMRR); ADD Mode with Either Channel Inverted	At least 10:1 at 50 MHz for common-mode signals of 10 divisions or less with VARIABLE VOLTS/DIV adjusted for best CMRR at 50 kHz.
POSITION	
Range	±(9.6 to 10.7) divisions ±0.4, ±0.7 div. At 50 mV per division with INVERT off, when Self Cal has been done within ±5°C of the operating temperature.
Gain Match Between NORMAL and SAVE	±3 DLs for positions within ±5 divisions from center.
Low-Frequency Linearity	
Normal or Average Mode	3 DLs or less compression or expansion of a two-division, center-screen signal when positioned anywhere within the acquisition window.
20 MHz Bandwidth Limiter	
−3 dB Bandwidth	13 MHz to 24 MHz.
50 MHz Bandwidth Limiter	
−3 dB Bandwidth	40 MHz to 55 MHz.
Rise Time	6.3 ns to 8.7 ns.[a] With a five-division, fast-rise step (rise time of 300 ps or less) using 50 Ω dc input coupling and VOLTS/DIV setting of 10 mV.[a]

[a]Performance Requirement not checked in the manual.

Table 1-1 (cont)

Characteristics	Performance Requirements
TRIGGERING—A AND B	
Minimum P-P Signal Amplitude for Stable Triggering from Channel 1, Channel 2, or ADD[d]	
A Trigger	
DC Coupled	0.35 division from DC to 50 MHz, increasing to 1.0 division at 150 MHz; 1.5 divisions at 150 MHz in ADD mode.
NOISE REJ Coupled	1.2 divisions or less from DC to 50 MHz, increasing to 3 divisions at 150 MHz; 4.5 divisions at 150 MHz in ADD mode.
AC Coupled	0.35 division from 60 Hz to 50 MHz; increasing to 1.0 division at 150 MHz, 1.5 divisions at 150 MHz in ADD mode. Attenuates signals below 60 Hz.
HF REJ Coupled	0.50 division from DC to 30 kHz. Attenuates signals above 30 kHz.
LF REJ Coupled	0.50 division from 80 kHz to 50 MHz; increasing to 1.0 division at 150 MHz; 1.5 divisions at 150 MHz in ADD mode. Attenuates signal below 80 kHz.
B Trigger	Multiply all A Trigger specifications by two.
A*B Selected	Multiply all A Trigger specifications by two.
Minimum P-P Signal Amplitude for Stable Triggering from EXT TRIG 1 or EXT TRIG 2 Source	
A Trigger	
EXT Gain = 1	
DC Coupled	17.5 mV from DC to 50 MHz, increasing to 50 mV at 150 MHz.
NOISE REJ Coupled	60 mV or less from DC to 50 MHz; increasing to 150 mV at 150 MHz.
AC Coupled	17.5 mV from 60 Hz to 50 MHz; increasing to 50 mV at 150 MHz. Attenuates signals below 60 Hz.
HF REJ Coupled	25 mV from DC to 30 kHz.
LF REJ Coupled	25 mV from 80 kHz to 50 MHz; increasing to 50 mV at 150 MHz.
EXT Gain = ÷5	Amplitudes are five times those specified for Ext Gain = 1.
B Trigger	Multiply all A Trigger amplitude specifications by two.
A*B Selected	Multiply all A Trigger amplitude specifications by two.
Maximum P-P Signal Rejected by NOISE REJ Coupling Signals within the Vertical Bandwidth	
Channel 1 or Channel 2 Source	0.4 division or greater for VOLTS/DIV settings of 10 mV and higher. Maximum noise rejected is reduced at 2 mV per division and 5 mV per division.
EXT TRIG 1 or EXT TRIG 2 Source	20 mV or greater when Ext Trig Gain = 1. 100 mV or greater when Ext Trig Gain = ÷5.

[d]A stable trigger is one that results in a uniform, regular display triggered on the selected slope. The trigger point must not switch between opposite slopes on the waveform, and the display must not "roll" across the screen on successive acquisitions. The TRIG'D LED stays constantly lit when the SEC/DIV setting is 2 ms or faster, but may flash when the SEC/DIV setting is 10 ms or slower.

Table 1-1 (cont)

Characteristics	Performance Requirements
EXT TRIG 1 and EXT TRIG 2 Inputs Resistance	1 MΩ ±1%.[a]
Capacitance	15 pF ±3 pF.[a]
Maximum Input Voltage ⚠	400 V (dc + peak ac); 800 V p-p ac at 10 kHz or less.[a]
LEVEL Control Range Channel 1 or Channel 2 Source	±18 divisions × VOLTS/DIV setting.[a]
EXT TRIG 1 or EXT TRIG 2 Source EXT GAIN = 1	±0.9 volt.[a]
EXT GAIN = ÷5	±4.5 volts.[a]
LEVEL Readout Accuracy (for triggering signals with transition times greater than 20 ns) Channel 1 or Channel 2 Source DC Coupled +15°C to +35°C	Within ± [3% of setting + 3% of p-p signal + (0.2 division × VOLTS/DIV setting) + 0.5 mV + (0.5 mV × probe attenuation factor)].
−15°C to +55°C (excluding +15°C to +35°C)	Add (1.5 mV x probe attenuation) to +15°C to +35°C specification.[a]
NOISE REJ Coupled	Add ± (0.6 division × VOLTS/DIV setting) to DC Coupled specifications. Checked at 50 mV per division.
EXT TRIG 1 or EXT TRIG 2 Source EXT GAIN = 1 DC Coupled	Within ± [3% of setting + 4% of p-p signal + 10 mV + (0.5 mV × probe attenuation factor)].
NOISE REJ Coupled	Add ±30 mV to DC Coupled specifications.
EXT GAIN = ÷5 DC Coupled	Within ± [3% of setting + 4% of p-p signal + 50 mv + (0.5 mV × probe attenuation factor)].
NOISE REJ Coupled	Add ±150 mV to DC Coupled specifications.

[a]**Performance Requirement not checked in manual.**

Table 1-1 (cont)

Characteristics	Performance Requirements		
Variable A Trigger Holdoff	A SEC/DIV[a]	MIN HO[a]	MAX HO[a]
	5 ns 10 ns 20 ns 50 ns 100 ns 200 ns	2-4 μs	9-15 μs
	500 ns	5-10 μs	
	1 μs 2 μs 5 μs	10-20 μs 20-40 μs 50-100 μs	100-150 μs
	10 μs 20 μs 50 μs	0.1-0.2 ms 0.2-0.4 ms 0.5-1.0 ms	1-1.5 ms
	100 μs 200 μs 500 μs	1-2 ms 2-4 ms 5-10 ms	10-15 ms
	1 ms 2 ms 5 ms	10-20 ms 20-40 ms 50-100 ms	90-150 ms
	10 ms 20 ms 50 ms	0.1-0.2 s 0.2-0.4 s 0.5-1.0 s	0.9-1.5 s
	100 ms 200 ms	1-2 s 2-4 s	9-15 s
	500 ms 1 s 2 s 5 s	5-10 s	
SLOPE Selection	Conforms to trigger-source waveform and ac-power-source waveform.		
Trigger Position Jitter (p-p)			
SEC/DIV 0.5 μs per Division or Greater			
A and B Triggered Sweeps	0.04 × SEC/DIV setting.[a]		
B RUNS AFTER Delay	0.08 × SEC/DIV setting.[a]		
SEC/DIV 0.2 μs per Division or Less	(0.02 × SEC/DIV setting) + 2 ns.[a] Checked at 5 ns/div with Repet OFF using a six-division, 10 MHz sine-wave input.[a]		

[a]Performance Requirement not checked in the manual.

Table 1-1 (cont)

Characteristics	Performance Requirements
TIME BASE	
Sample Rate Accuracy	
Average Over 100 or More Samples	±0.01%.[a]
External Clock	
Repetition Rate	
Minimum	1 MHz.[a]
Maximum	100 MHz.[a]
Events Count	1 to 65,536[a]
Events Maximum Repetition Rate	100 MHz.[a]
Signal Levels Required for EXT Clock or EVENTS	
Channel 1 or Channel 2 SOURCE	
DC Coupled	0.7 division from DC to 20 MHz; increasing to 2.0 divisions at 100 MHz; 3.0 divisions at 100 MHz in ADD mode.[a]
NOISE REJ Coupled	2.4 divisions or less from DC to 20 MHz; increasing to 6.0 divisions at 100 MHz; 9.0 divisions at 100 MHz in ADD mode.[a]
AC Coupled	0.7 division from 60 Hz to 20 MHz; increasing to 2.0 divisions at 100 MHz; 3.0 divisions at 100 MHz in ADD mode. Attenuates signals below 60 Hz.[a]
HF REJ Coupled	2.0 divisions from DC to 30 kHz. Attenuates signals above 30 kHz.[a]
LF REJ Coupled	2.0 divisions from 80 kHz to 20 MHz; increasing to 4.0 divisions at 100 MHz; 3.0 divisions at 100 MHz in ADD mode. Attenuates signals below 80 kHz.[a]
EXT TRIG 1 or EXT TRIG 2 Source	
Ext Gain = 1	
DC Coupled	35 mV from DC to 20 MHz; increasing to 100 mV at 100 MHz.[a]
NOISE REJ Coupled	120 mV or less from DC to 20 MHz; increasing to 300 mV at 100 MHz.[a]
AC Coupled	35 mV from 60 Hz to 20 MHz; increasing to 100 mV at 100 MHz. Attenuates signals below 60 Hz.[a]
HF REJ Coupled	50 mV from DC to 30 kHz.[a]
LF REJ Coupled	50 mV from 80 kHz to 20 MHz; increasing to 100 mV at 100 MHz.[a]
Ext Gain = ÷ 5	Amplitudes are five times those specified for Ext Gain = 1.[a]
Delay Time Range	(0.04 × B SEC/DIV) to (65,536 × 0.04 × B SEC/DIV).[a]
Delay Time Accuracy	Same as the sample rate accuracy.[a]
Delay Time Resolution	The greater of (0.04 × B SEC/DIV) or 20 ns.

[a]Performance Requirement not checked in the manual.

Table 1-1 (cont)

Characteristics	Performance Requirements
NONVOLATILE MEMORY	
Last and Recall Setup 1 Front-Panel Settings and Calibration Constants Retention Time	Greater than 3 years.[a]
Waveform Data and Recall Front-Panel Settings 2 through 5 Retention Time	
Storage Temperature	
25°C	Greater than 120 hours.[a]
50°C	Greater than 24 hours.[a]
Battery	3.5-volt lithium thionyl chloride; Type LTC-7P; UL listed.[a] **WARNING** *To avoid personal injury, observe proper procedures for handling and disposal of lithium batteries. Improper handling may cause fire, explosion, or severe burns. Don't recharge, crush, disassemble, heat the battery above 212°F (100°C), incinerate, or expose contents of the battery to water. Dispose of battery in accordance with local, state, and national regulations.* *Typically, small quantities (less than 20) can be safely disposed of with ordinary garbage in a sanitary landfill.* *Larger quantities must be sent by surface transport to a hazardous waste disposal facility. The batteries should be individually packaged to prevent shorting and packed in a sturdy container that is clearly labeled "Lithium Batteries—DO NOT OPEN."*

[a]Performance Requirement not checked in the manual.

Table 1-1 (cont)

Characteristics	Performance Requirements			
SIGNAL OUTPUTS				
CALIBRATOR	CALIBRATOR output amplitudes at 5 MHz are at least 50% of output amplitudes at 1 ms SEC/DIV setting.[a]			
Voltage (with A SEC/DIV switch set to 1 ms)				
1 MΩ Load	0.4 V ±1%.[a]			
50 Ω Load	0.2 V ±1.5%.[a]			
Current (short circuit load with A SEC/DIV switch set to 1 ms)	8 mA ±1.5%.[a]			
Repetition Period	**A SEC/DIV Setting[a]**	**Calibrator Frequency[a]**	**Calibrator Period[a]**	**Div/ Cycle[a]**
	5 ns 10 ns 20 ns 50 ns 100 ns 200 ns	5 MHz	200 ns	40 20 10 4 2 1
	500 ns 1 μs	500 kHz	2 μs	4 2
	5 μs 10 μs 20 μs	50 kHz	20 μs	4 2 1
	50 μs 100 μs 200 μs	5 kHz	200 μs	4 2 1
	500 μs 1 ms 2 ms	500 Hz	2 ms	4 2 1
	5 ms 10 ms 20 ms 50 ms 100 ms 200 ms 500 ms 1 s 2 s 5 s	50 Hz	20 ms	4 2 1 0.4 0.2 0.1 0.04 0.02 0.01 0.004
Accuracy	±0.01%.[a]			
Symmetry	Duration of high portion of output cycle is 50% of output period ± (lesser of 500 ns or 25% of period).[a]			

[a]Performance Requirement not checked in the manual.

Table 1-1 (cont)

Characteristics	Performance Requirements
CH 2 SIGNAL OUTPUT	
Output Voltage	20 mV per division ±10% into 1 MΩ. 10 mV per divison ±10% into 50 Ω.
Offset	±10 mV into 50 Ω, when dc balance has been performed within ±5°C of the operating temperature.
−3 dB Bandwidth	DC to greater than 50 MHz.
A TRIGGER, RECORD TRIGGER, and WORD RECOGNIZER Output	
Logic Polarity	Negative true. Trigger occurrence indicated by a HI to LO transition.[a]
Output Voltage HI	
Load of 400 μA or Less	2.5 V to 3.5 V.[a]
50 Ω Load to Ground	0.45 V or greater.[a]
Output Voltage LO	
Load of 4 mA or Less	0.5 V or less.[a]
50 Ω Load to Ground	0.15 V or less.[a]
PLOTTER	
X-Output and Y-Output	
Output Resistance	1 kΩ ±10%.
Output Range	± (2 V ±100 mV). Scale Factors Y—390 mV per division; X—390 mV per division.
Output Center	0 volts ±30 mV.
Home (Lower Left) Position	−2 V ±100 mV.
Slew Rate	Less than 8 volts per second.[a] The instantaneous slew rate is determined by the output stage time constant (3.3 ms) and can exceed 8 volts per second. The System μP computes the length of the stroke needed for each point and waits an appropriate time at each position before proceeding so that the X-Y plotter sees an effective slew rate of less than 8 volts per second.[a]
Pen Lift, SPST Relay Contact to Ground	
Polarity	Menu selectable.[a]
Maximum Applied Open-Circuit Voltage	±25 volts.[a]
Maximum Closed-Circuit Resistance	1 Ω or less.[a]
Maximum Closed-Circuit Current	250 mA or less.[a]

[a]Performance Requirement not checked in the manual.

Table 1-1 (cont)

Characteristics	Performance Requirements
DISPLAY	
Graticule	80 mm × 100 mm (8 × 10 divisions).[a]
Phosphor	P31.[a]
Nominal Accelerating Potential	16 kV.[a]
Waveform and Cursor Display, Vertical	
Resolution, Electrical	One part in 1024 (10 bit). Calibrated for 100 points per division.[a]
Gain Accuracy	Graticule indication of voltage cursor difference is within 1% of CRT cursor readout value, measured over center 6 divisions.
Centering; Vectors OFF	Within ±0.1 division.
Offset with Vectors ON	Less than 0.05 division.
Linearity	Less than 0.1 division difference between graticule indication and crt cursor readout when active volts cursor is positioned anywhere on screen and inactive cursor is at center screen.[a]
Vector Response	
NORMAL Mode	
Step Aberration	+4%, −4%, 4% p-p.
Fill	Edges of filled regions match reference lines within ±0.1 division.
ENVELOPE Mode	
Fill	Less than 1% change in p-p amplitude of a 6-division, filled ENVELOPE waveform when switching vectors ON and OFF.
Waveform and Cursor Display, Horizontal	
Resolution, Electrical	One part in 1024 (10 bit). Calibrated for 100 points per division.[a]
Gain Accuracy	Graticule indication at time cursor difference is within 1% of crt cursor readout value, measured over center 6 divisions.
Centering; Vectors OFF	Within ±0.1 division.
Offset with Vectors ON	Less than 0.05 division.
Linearity	Less than 0.1 division difference between graticule indication and crt cursor readout when active time cursor is positioned anywhere along center horizontal graticule line and inactive cursor is at center screen.[a]

[a]Performance Requirement not checked in the manual.

Table 1-1 (cont)

Characteristics	Performance Requirements
AC POWER SOURCE	
Source Voltage	
Nominal Ranges	
115 V	90 V to 132 V.[a]
230 V	180 V to 250 V.[a]
Source Frequency	48 Hz to 440 Hz.[a]
Fuse Rating	5 A, 250 V, AGC/3AG, Fast Blow; or 4 A, 250 V, 5 × 20 mm Time-Lag (T).[a] Each fuse type requires a different fuse cap.[a]
Power Consumption	
Typical (standard instrument)	160 watts (250 VA).[a]
Maximum (fully optioned instrument)	200 watts (300 VA).[a]
Primary Grounding[c]	Type test 0.1 Ω maximum. Routine test to check grounding continuity between chassis ground and protective earth ground.[a]

[a]Performance Requirement not checked in the manual.

[c]Routine test is with ROD-L/EPA Electronic Model 100AV Hi-Pot Tester. This tests both the Primary Circuit Dielectric Withstand and Primary Grounding in one operation. Contact Tektronix Product Safety prior to using any other piece of equipment to perform these tests.

Table 1-2

Environmental Characteristics

Characteristics	Performance Requirements
STANDARD INSTRUMENT	
Environmental Requirements	The 2430 Digital Oscilloscope meets the environmental requirements of MIL-T-28800C for Type III, Class 3, Style D equipment, with the humidity and temperature requirements defined in paragraphs 3.9.2.2, 3.9.2.3, and 3.9.2.4.
Temperature	
Operating	−15°C to +55°C.
Nonoperating (storage)	−62°C to +85°C.
Altitude	
Operating	To 15,000 feet (4500 meters). Maximum operating temperature decreased 1°C for each 1000 feet (300 meters) above 5000 feet (1500 meters).
Nonoperating (storage)	To 50,000 feet (15,000 meters).
Humidity	
Operating and Storage	Stored at 95% relative humidity for five cycles (120 hours) from 30°C to 60°C, with operation performance checks at 30°C and 55°C.
Vibration	
Operating	15 minutes along each of three axes at a total displacement of 0.025 inch (0.64 mm) p-p (4 g at 55 Hz), with frequency varied from 10 Hz to 55 Hz in one-minute sweeps. Hold 10 minutes at each major resonance, or if none exist, hold 10 minutes at 55 Hz (75 minutes total test time).
Shock	
Operating and Nonoperating	50-g, half-sine, 11-ms duration, three shocks on each face, for a total of 18 shocks.
Transit Drop (not in shipping package)	12-inch (300-mm) drop on each corner and each face (exceeds MIL-T-28800C, paragraphs 3.9.5.2 and 4.5.5.4.2).
Bench Handling	
Cabinet On and Cabinet Off	MIL-STD-810C, Method 516.2, Procedure V (MIL-T-28800C, Paragraph 4.5.5.4.3).
Topple (cabinet installed)	
Operating	Set on rear feet and allow to topple over onto each of four adjacent faces (Tektronix Standard 062-2858-00).
Packaged Transportation	
Drop	Meets the limits of the National Safe Transit Assn., test procedure 1A-B-2; 10 drops of 36 inches (914 mm) (Tektronix Standard 062-2858-00).
Vibration	Meets the limits of the National Safe Transit Assn., test procedure 1A-B-1; excursion of 1 inch (25.4 mm) p-p at 4.63 Hz (1.1 g) for 30 minutes (Tektronix Standard 062-2858-00).

Table 1-2 (cont)

Characteristics	Performance Requirements
Environmental Requirements (cont)	
EMI (electromagnetic interference)	Meets MIL-T-28800C; MIL-STD-461B, part 4 (CE-03 and CS-02), part 5 (CS-06 and RS-02), and part 7 (CS-01, RE-02, and RS-03—limited to 1 GHz); VDE 0871, Category B; Part 15 of FCC Rules and Regulations, Subpart J, Class A; and Tektronix Standard 062-2866-00.
Electrostatic Discharge Susceptibility	Meets Tektronix Standard 062-2862-00. The instrument will not change control states with discharges of less than 10 kV.
X-Ray Radiation	Meets requirements of Tektronix Standard 062-1860-00.
RACKMOUNTED INSTRUMENT	
Environmental Requirements	Listed characteristics for vibration and shock indicate those environments in which the rackmounted instrument meets or exceeds the requirements of MIL-T-28800C with respect to Type III, Class 5, Style D equipment with the rackmounting rear-support kit installed. Refer to the Standard Instrument Environmental Specification for the remaining performance requirements. Instruments will be capable of meeting or exceeding the requirements of Tektronix Standard 062-2853-00, class 5.
Temperature (operating)	−15°C to +55°C, ambient temperature measured at the instrument's air inlet. Fan exhaust temperature should not exceed +65°C.
Vibration	15 minutes along each of three major axes at a total displacement of 0.015 inch (0.38 mm) p-p (2.3 g at 55 Hz), with frequency varied from 10 Hz to 55 Hz to 10 Hz in one-minute sweeps. Hold 10 minutes at each major resonance, or if no major resonance present, hold 10 minutes at 55 Hz (75 minutes total test time).
Shock (operating and nonoperating)	30-g, half-sine, 11-ms duration, three shocks per axis in each direction, for a total of 18 shocks.

Table 1-3

Mechanical Characteristics

Characteristics	Description
STANDARD INSTRUMENT	
Weight	
With Front Cover, Accessories, and Accessories Pouch	≃12.8 kg (28.1 lbs).
Without Front Cover, Accessories, and Accessories Pouch	≃10.9 kg (23.9 lbs).
Domestic Shipping Weight	≃16.4 kg (36 lbs).
Overall Dimensions	See Figure 1-1 for a dimensional drawing.
Height	
With Feet and Accessories Pouch	190 mm (7.48 in).
Without Accessories Pouch	160 mm (6.3 in).
Width (with handle)	330 mm (13.0 in).
Depth	
With Front Cover	479 mm (18.86 in).
With Handle Extended	550 mm (21.65 in).
Cooling	Forced air circulation; no air filter.
Finish	Tektronix Blue vinyl-clad material on aluminum cabinet.
Construction	Aluminum-alloy/plastic-composite chassis (spot-molded). Plastic-laminate front panel. Glass-laminate circuit boards.
RACKMOUNTING	
Rackmounting Conversion Kit	
Weight	4.0 kg (8.8 lbs).
Domestic Shipping Weight	6.3 kg (13.8 lbs).
Height	178 mm (7 in).
Width	483 mm (19 in).
Depth	419 mm (16.5 in).
Rear Support Kit	
Weight	0.68 kg (1.5 lbs).
OPTION 1R	
Rackmounted Instrument (Option 1R)	
Weight	≃15.8 kg (34.9 lbs).
Domestic Shipping Weight	≃18.1 kg (39.9 lbs).
Height	178 mm (7 in).
Width	483 mm (19 in).
Depth	419 mm (16.5 in).

Table 1-4

Option 05 (TV Trigger) Electrical Characteristics

Characteristics	Performance Requirements
VERTICAL—CHANNEL 1 AND CHANNEL 2	
Frequency Response	
Full Bandwidth	
50 kHz to 5 MHz	Within ±1%.
Greater than 5 MHz to 10 MHz	Within +1%, −2%.
Greater than 10 MHz to 30 MHz	Within +2%, −3%. For VOLTS/DIV switch settings between 5 mV and 0.2 V per division with VARIABLE VOLTS/DIV set to CAL. Five-division, 50 kHz reference signals from a 50 Ω system. With external 50 Ω termination on a 1 MΩ input.
20 MHz Bandwidth Limit	
50 kHz to 5 MHz	Within +1%, −4%.
Square Wave Flatness	
Field Rate	
5 mV/div to 20 mV/div	±1%, 1% p-p at 60 Hz with input signal of 0.1 V.
50 mV/div	±1%, 1% p-p at 60 Hz with input signal of 1.0 V. With fast-rise step (rise time 1 ns or less), 1 MΩ dc input coupling, an external 50 Ω termination, and VARIABLE VOLTS/DIV set to CAL. Exclude the first 20 ns following the step transition and exclude the first 30 ns when 20 MHz BW LIMIT is set.
Line Rate	
5 mV/div to 20 mV/div	±1%, 1% p-p at 15 kHz with input signal of 0.1 V.
50 mV/div	±1%, 1% p-p at 15 kHz with input signal of 1.0 V.
TV (Back-Porch) Clamp (CH 2 Only)	
60 Hz Attenuation	18 dB or greater. For VOLTS/DIV switch settings between 5 mV and 0.2 V with VARIABLE VOLTS/DIV set to CAL. Six-division reference signal.
Back-Porch Reference	Within ±1.0 division of ground reference.

Table 1-4 (cont)

Characteristics	Performance Requirements
	TRIGGERING
Sync Separation	Stable video rejection and sync separation from sync-positive or sync-negative composite video, 525 to 1280 lines, 50 Hz or 60 Hz, interlaced or noninterlaced systems.
Trigger Modes	
A Horizontal Mode	All lines: Field 1, selected line (1 to n), Field 2, selected line (1 to n), Alt fields, selected line (1 to n). n is equal to or less than the number of lines in the frame and less than or equal to 1280.
B Horizontal Mode	Delayed by time.
Minimum Input Signal Amplitude for Stable Triggering[a]	
Channel 1 and Channel 2	
Composite Video	2 divisions.
Composite Sync	0.6 division. Peak signal amplitude within 18 divisions of input ground reference.
EXT TRIG 1 or EXT TRIG 2	
EXT GAIN = 1	
Composite Video	60 mV
Composite Sync	30 mV Peak signal amplitude within ±0.9 V from input ground reference.
EXT GAIN = ÷5	
Composite Video	300 mV
Composite Sync	150 mV Peak signal amplitude within ±4.9 V from input ground reference.

[a]Performance Requirement not checked in manual.

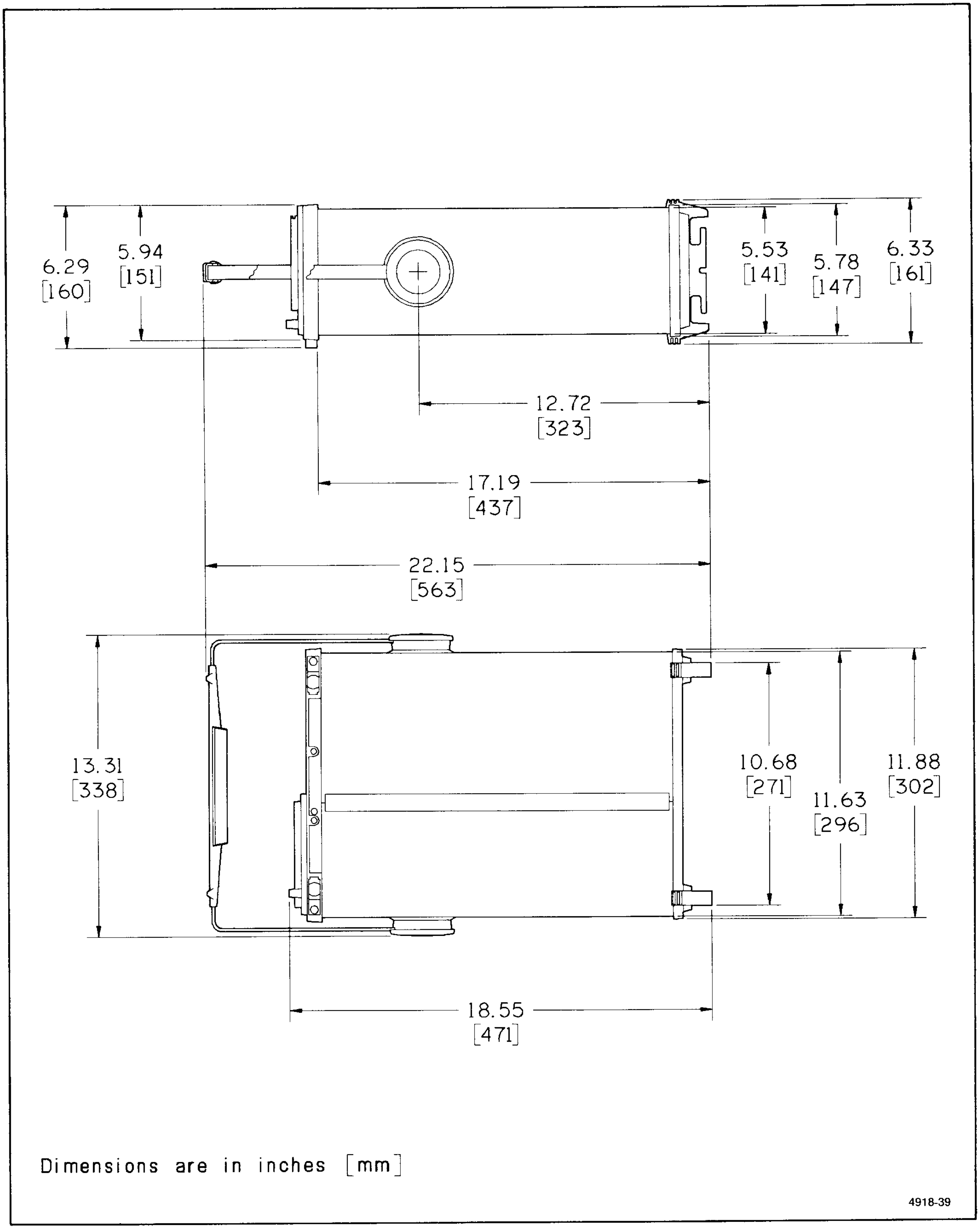


Figure 1-1. Dimensional drawing.

PREPARATION FOR USE

SAFETY

This section tells how to prepare for and to proceed with the initial start-up of the TEKTRONIX 2430 Digital Oscilloscope.

Refer to the Operators and Servicing Safety Summaries at the front of this manual for power source, grounding, and other safety considerations pertaining to the use of the instrument. Before connecting the oscilloscope to a power source, read both this section and the Safety Summaries.

CAUTION

This instrument may be damaged if operated with the LINE VOLTAGE SELECTOR switch set for the wrong applied ac input-source voltage or if the wrong line fuse is installed.

LINE VOLTAGE SELECTION

The 2430 operates from either a 115 V or 230 V nominal ac power-input source having a line frequency ranging from 48 Hz to 440 Hz. Before connecting the power cord to a power-input source, verify that the LINE VOLTAGE SELECTOR switch, located on the rear panel (see Figure 2-1), is set for the correct nominal ac input-source voltage. To convert the instrument for operation from one line-voltage range to the other, move the LINE VOLTAGE SELECTOR switch to the correct nominal ac source-voltage setting (see Table 2-1). The detachable power cord may have to be changed to match the particular power-source outlet.

LINE FUSE

To verify the proper value of the instrument's power-input fuse, perform the following procedure:

1. Press in the fuse-holder cap and release it with a slight counterclockwise rotation.

2. Pull the cap (with the attached fuse inside) out of the fuse holder.

3. Verify proper fuse value (see Table 2-1).

4. Install the proper fuse and reinstall the fuse-holder cap.

NOTE

A 4 A, 250 V, 5 × 20 mm Time-lag (T) fuse may be substituted for the factory-installed fuse. However, the two types of fuses are NOT directly interchangeable; each requires a different type of fuse cap.

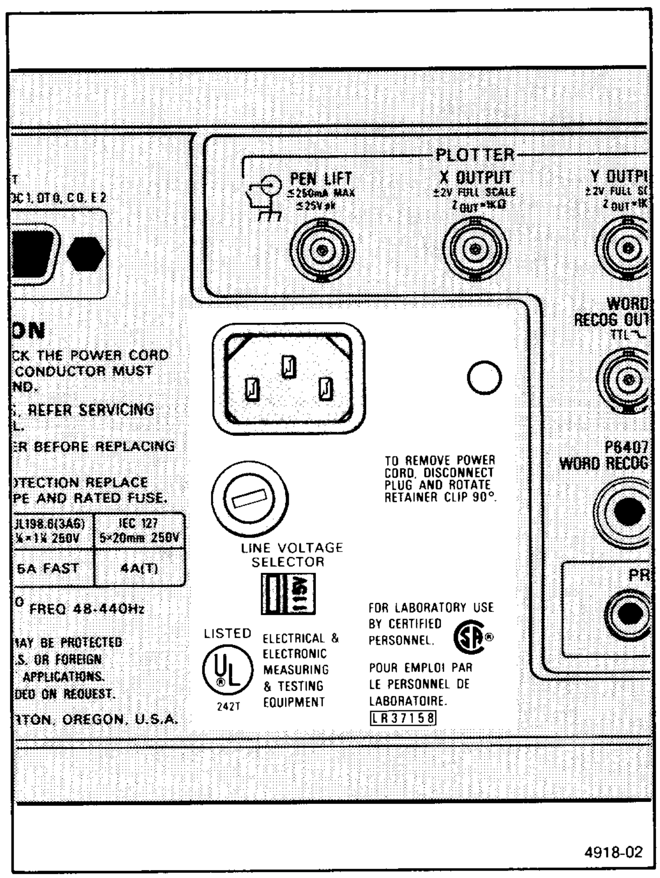
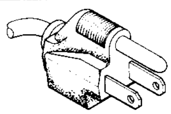
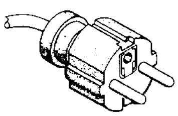
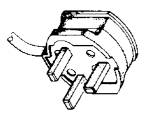
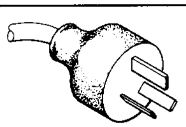
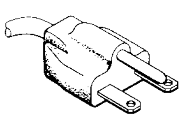
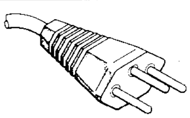


Figure 2-1. LINE VOLTAGE SELECTOR, line fuse, and power cord receptacle.

Table 2-1

Voltage, Fuse, and Power-Cord Data

Plug Configuration	Category	Power Cord And Plug Type	Line Voltage Selector Setting	Voltage Range (AC)	Factory Installed Instrument Fuse	Fuse Holder Cap	Reference Standards[b]
	U.S. Domestic Standard	U.S. 120V 15A	115V	90V to 132V	5A, 250V AGC/3AG Fast-blow (UL 198.6)	AGC/3AG	ANSI C73.11 NEMA 5-15-P UL 198.6
	Option A1	EURO 240V 10-16A	230V	180V to 250V	5A, 250V AGC/3AG Fast-blow (UL 198.6)	AGC/3AG	CEE(7), II, IV, VII IEC 83 IEC 127
	Option A2	UK[a] 240V 6A	230V	180V to 250V	5A, 250V AGC/3AG Fast-blow (UL 198.6)	AGC/3AG	BS 1363 IEC 83 IEC 127
	Option A3	Australian 240V 10A	230V	180V to 250V	5A, 250V AGC/3AG Fast-blow (UL 198.6)	AGC/3AG	AS C112 IEC 127
	Option A4	North American 240V 15A	230V	180V to 250V	5A, 250V AGC/3AG Fast-blow (UL 198.6)	AGC/3AG	ANSI C73.20 NEMA 6-15-P IEC 83 UL 198.6
	Option A5	Switzerland 220V 6A	230V	180V to 250V	5A, 250V AGC/3AG Fast-blow (UL 198.6)	AGC/3AG	SEV IEC 127

[a] A 6A, Type C fuse is also installed inside the plug of the Option A2 power cord.

[b] Reference Standards Abbreviations:

ANSI—American National Standards Institute
AS—Standards Association of Australia
BS—British Standards Institution
CEE—International Commission on Rules for the Approval of Electrical Equipment
IEC—International Electrotechnical Commission
NEMA—National Electrical Manufacturer's Association
SEV—Schweizevischer Elektrotechischer Verein
UL—Underwriters Laboratories Inc.

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POWER CORD

This instrument has a detachable three-wire power cord with a three-contact plug for connection to both the power source and protective ground. The power cord is secured to the rear panel by a cord-set securing clamp. The protective ground contact on the plug connects (through the power cord protective grounding conductor) to the accessible metal parts of the instrument. For electrical shock protection, insert this plug into a power-source outlet that has a properly grounded protective-ground contact.

Instruments are shipped with the required power cord as ordered by the customer. Information on the available power cords is presented in Table 2-1, and part numbers are listed in "Options and Accessories" (Section 7). Contact your Tektronix representative or local Tektronix Field Office for additional power-cord information.

INSTRUMENT COOLING

To prevent instrument damage from overheated components, adequate internal airflow must be maintained. Before turning on the power, first verify that air-intake holes on the bottom and side of the cabinet and the fan exhaust holes are free of any obstruction to airflow. The scope has a thermal cutout that will activate if overheating occurs. The scope shuts down immediately with no attempt to save waveforms or front-panel conditions if a cutout happens. Power will be disabled to the scope until the thermal cutout cools down, at which time the power-on sequence is redone. The resulting loss of the last front-panel and waveform data will cause the power-on self test to fail and is indicated to the user by a failed CKSUM-NVRAM test (number 6000 in the main EXTENDED DIAGNOSTICS menu). The cause of the overheating must be corrected before attempting prolonged operation of the scope. Pressing the MENU OFF/EXTENDED FUNCTIONS button exits the EXTENDED DIAGNOSTICS mode to the normal operating mode.

OPERATING INFORMATION

All operating information pertaining to the use of the menus, controls and connectors, operators familiarization, and basic applications is found in the 2430 Operators Manual. A User Reference Guide, supplied with the 2430, provides quick reference to the menu-selected features of the instrument. GPIB operating information is included in the Operators Manual. Additional information on the GPIB (General Purpose Interface Bus) may be found in the Instrument Interface Guide, written specifically for system programmers.

START-UP

The 2430 automatically performs power-up self tests each time the instrument is turned on. These tests provide the user with the highest possible confidence level that the instrument is fully functional. If no faults are encountered, the instrument will enter the Scope mode in the SAVE Storage mode. Failure of a test in the range of 6000 to 9300 may not indicate a fatal scope fault. Several conditions can occur that will cause a nonfatal failure of the tests. In each of these cases, the abnormal condition is brought to the user's attention by the scope entering the "EXTENDED DIAGNOSTICS" mode. Recovery from some abnormal conditions may be possible by simply pressing the MENU OFF button to enter the Scope mode. Running the "SELF CAL" procedure after the scope has warmed up ("NOT WARMED UP" message is removed from the main CAL/DIAG menu in about ten minutes after power-on) may also eliminate the cause of the nonfatal error. Refer to "Calibration and Diagnostics," located in Section 6 of this manual, for information on the power-up tests and the procedures to follow in the event of a failed test.

If the power-on self-test fails due to an actual component failure, the scope may still be usable for the immediate measurement purpose. For example, if the problem area is in CH 2, CH 1 may still be used with full confidence of making accurate measurements. Depending on the nature of the failure, the "UNCALD" message may or may not be displayed, but the failed test or tests will be indicated by a "FAIL" message displayed with the associated EXTENDED DIAGNOSTICS test. Press the MENU OFF/EXTENDED FUNCTIONS button to exit EXTENDED DIAGNOSTICS to check out the scope for use.

A fatal fault in the operating system will cause the scope to abort. No displays are possible, and the user is notified of an abort situation only by the flashing of the Trigger LED indicators (if that is possible). Cycling the power off then back on may clear the problem, but a failure of this magnitude will usually require the scope to be checked and repaired by a qualified service person. Persistent or reoccurring failures of the power-on or self-diagnostic test should be repaired at the first opportunity.

Operation of the diagnostics features and troubleshooting of the 2430 are detailed in Section 6 of this manual (Maintenance) under "Calibration and Diagnostics." Consult your service department, your local Tektronix Service Center, or nearest Tektronix representative if further assistance is needed.

POWER-DOWN

NOTE

DO NOT TURN THE 2430 OFF WHILE THE SELF CAL ROUTINE IS RUNNING. Turning off the power prior to completion of SELF CAL will invalidate the instrument calibration constants. The scope will then require a partial calibration to restore the constants to correct values that return the scope to normal operation. The extent of calibration required depends on which constants were invalidated.

For a normal power-off from the scope mode, an orderly power-down sequence that retains the save and saveref waveforms, the current front-panel control settings, and any stored front-panel settings is done. A power-off or transient power fluctuation during SELF CAL, active EXTENDED DIAGNOSTICS testing, EXTENDED CALIBRATION, or shut-down at any time due to overheating does not permit execution of the normal power-down sequence. The result of such an occurrence is the loss of stored calibration constants or last front-panel control settings (or both) and a failure of the next power-on self-test.

NOTE

In the event of a momentary power interruption that starts the power-off sequence of the 2430, the scope will redo the power-on procedure. If the scope was in the middle of a waveform acquisition when the power interruption occurred, that waveform data will not be saved, and the invalid waveform data display will be seen when power-on has completed. Press ACQUIRE to restart the acquisition and obtain valid waveform data.

If the scope remains off longer than the short-term nonvolatile SAVE waveform RAM can save data (more than three to five days), the waveforms (or front-panel setups) stored in the SAVE waveform memory may become lost. The result is that SAVE and SAVEREF waveforms stored at power-off are replaced by the invalid waveform display when the scope is again turned on. Each operating period of the scope refreshes the short-term nonvolatile memory.

REPACKAGING FOR SHIPMENT

It is recommended that the original carton and packing material be saved in the event it is necessary for the instrument to be reshipped using a commercial transport carrier. If the original materials are unfit or not available, then repackage the instrument using the following procedure:

1. Use a corrugated cardboard shipping carton having a test strength of at least 275 pounds and with an inside dimension at least six inches greater than the instrument dimensions.

2. If instrument is being shipped to a Tektronix Service Center, enclose the following information: the owner's address, name and phone number of a contact person, type and serial number of the instrument, reason for returning, and a complete description of the service required.

3. Completely wrap the instrument with polyethylene sheeting or equivalent to protect the outside finish and prevent entry of harmful substances into the instrument.

4. Cushion instrument on all sides using three inches of padding material or urethane foam, tightly packed between the carton and the instrument.

5. Seal the shipping carton with an industrial stapler or strapping tape.

6. Mark the address of the Tektronix Service Center and also your own return address on the shipping carton in two prominent locations.

THEORY OF OPERATION

SECTION ORGANIZATION

This section of the manual is divided into three subsections, with each subsection increasing in detail. The first subsection is the "Simplified Block Diagram Description" which contains a general summary of instrument operation by diagram. A simplified block diagram accompanies the text. Subsection two is the "Detailed Block Diagram Description" which discusses the circuit functions in greater detail and provides a more in-depth look at the acquisition system of the 2430. A detailed block diagram is located in the foldout pages at the rear of this manual. Generally, both block diagram descriptions follow the signal-flow path as much as possible and not the schematic diagram number order as is done in the "Detailed Circuit Description."

Subsection three is the "Detailed Circuit Description" which discusses the circuitry shown in the schematic diagram foldouts, also located at the rear of this manual. The schematic diagram number associated with each description is identified in the text and is shown on the block diagrams. For best understanding of the circuit being described, refer to the appropriate schematic diagram and the block diagrams. The order of discussion in the circuit descriptions follows the schematic diagram number order.

INTEGRATED CIRCUIT DESCRIPTIONS

Digital logic circuits perform most of the functions within the instrument. Functions and operation of the logic circuits are shown using logic symbols and terms. Most logic functions are described using the positive-logic convention. Positive logic is a notation system in which the more positive of the two logic levels is the HI (or 1) state; the more negative level is the LO (or 0) state. Voltages that constitute a HI or a LO state vary between specific devices. Refer to the device manufacturer's data book for specific electrical characteristics or logical operation of common parts.

The functioning of linear integrated circuit devices in this section is discussed using waveforms or other techniques such as voltage measurements and simplified diagrams, where required, to illustrate their operation.

SIMPLIFIED BLOCK DIAGRAM DESCRIPTION

This discussion is of the block diagram shown in Figure 3-1.

Attenuators and Preamplifiers (diagram 9)

ATTENUATORS. The Attenuators are settable to 1X, 10X, or 100X attenuation, to reduce the input signal level to within the dynamic range of the Preamplifiers. Input coupling for the signal to the Attenuators may be either AC or DC with 1 MΩ termination or DC with 50 Ω termination. Attenuator and coupling switching are controlled by the System μP using register-activated magnetic-latch switches.

PREAMPLIFIERS. The Preamplifiers provide switchable gain setting and buffering of the attenuated input signal. Single-ended input signals are converted to double-ended (differential) output signals. Variable Vertical Mode gain, vertical position, and DC Balance are controlled by input signals to the Preamplifiers. The System μP-controlled gain in combination with the switchable attenuator settings allow the complete range of available VOLTS/DIV switch settings from 2 mV to 5 V to be obtained. Trigger pickoffs provide a sample of the input signal to the trigger system for use as a triggering signal source. With the Video Option installed, a Channel 2 pickoff signal is supplied from the Preamplifiers as a trigger signal source. Also, a Channel 2 Offset signal used to control the back-porch clamping is provided from the Video Option to the Channel 2 Preamplifier.

Peak Detectors and CCD/Clock Drivers (diagram 10)

PEAK DETECTORS. Additional buffering of the signal to the CCDs is provided by the Peak Detectors for all acquisition modes. The bandwidth of the input amplifiers of the Peak Detectors is switchable for FULL, 50 MHz, and 20 MHz bandwidths. In Envelope acquisition mode, dual min-max Peak Detectors detect and hold the minimum and maximum peak signal amplitudes that occur between sampling clocks. Those min and max signal values are then applied to the CCDs for sampling. Control data from the System μP controls the bandwidth selection, and peak detector clock signals multiplex the signal samples from the Peak Detectors to the CCDs. A calibration signal input is provided to the Peak Detectors for use in automatic calibration and diagnostic testing of the acquisition system.

Common-mode adjust circuitry on the output of the Peak Detectors is used to control the overall gain of the Peak Detector/CCD acquisition subsystem. Using digital signals to the DAC system, analog voltages are generated that set the gain of the Common-mode adjust amplifiers. These amplifiers monitor the dc common-mode level of the Peak Detector outputs and match it to the control gain level set by the System μP. That dc level sets the CCD signal gain.

CCD/CLOCK DRIVERS. The CCDs are fast analog shift registers that can hold more that enough samples to fill the complete waveform record of 1024 samples per channel. The extra samples are used to account for the uncertainty of the trigger point location in the 32 samples stored in the input register. Once a trigger occurs, the samples not needed to fill the waveform records are basically discarded. For fast signals, waveform samples are stored very rapidly and then shifted out at a rate that can be handled by the A/D Converter. When the sample rate is slow enough to allow direct conversion of the input samples, a Short Pipeline mode is used to shift samples directly through the CCD registers. The Clock Driver portion of the devices produces the phase clocks that shift the analog data through the CCD registers. Other clocks used to sample the signal and transfer the samples into and out of the CCD arrays are generated in the CCD Clock and System Clock circuits (diagrams 11 and 7 respectively).

CCD Output (diagram 14)

The differential signals from both sides and both channels of the CCD arrays are combined and multiplexed onto a single data line to the A/D Converter. The output clocking is referenced to the sample and phase clocks to maintain the correct data timing relationships of the samples. Waveform data samples are therefore stored in the correct Acquisition Memory locations after being digitized.

A/D Converter and Acquisition Latches (diagram 15)

A/D CONVERTER. The combined samples of analog signals are converted to eight-bit data bytes by the A/D Converter. In Envelope Mode, the data bytes are applied to two magnitude comparators, along with the previous maximum and minimum data bytes to determine if it is greater in magnitude than the last maximum or minimum. If a new data byte is greater, the new data byte is latched into the Acquisition Latches; otherwise, latching does not occur. Clocking to direct the signals into the Acquisition

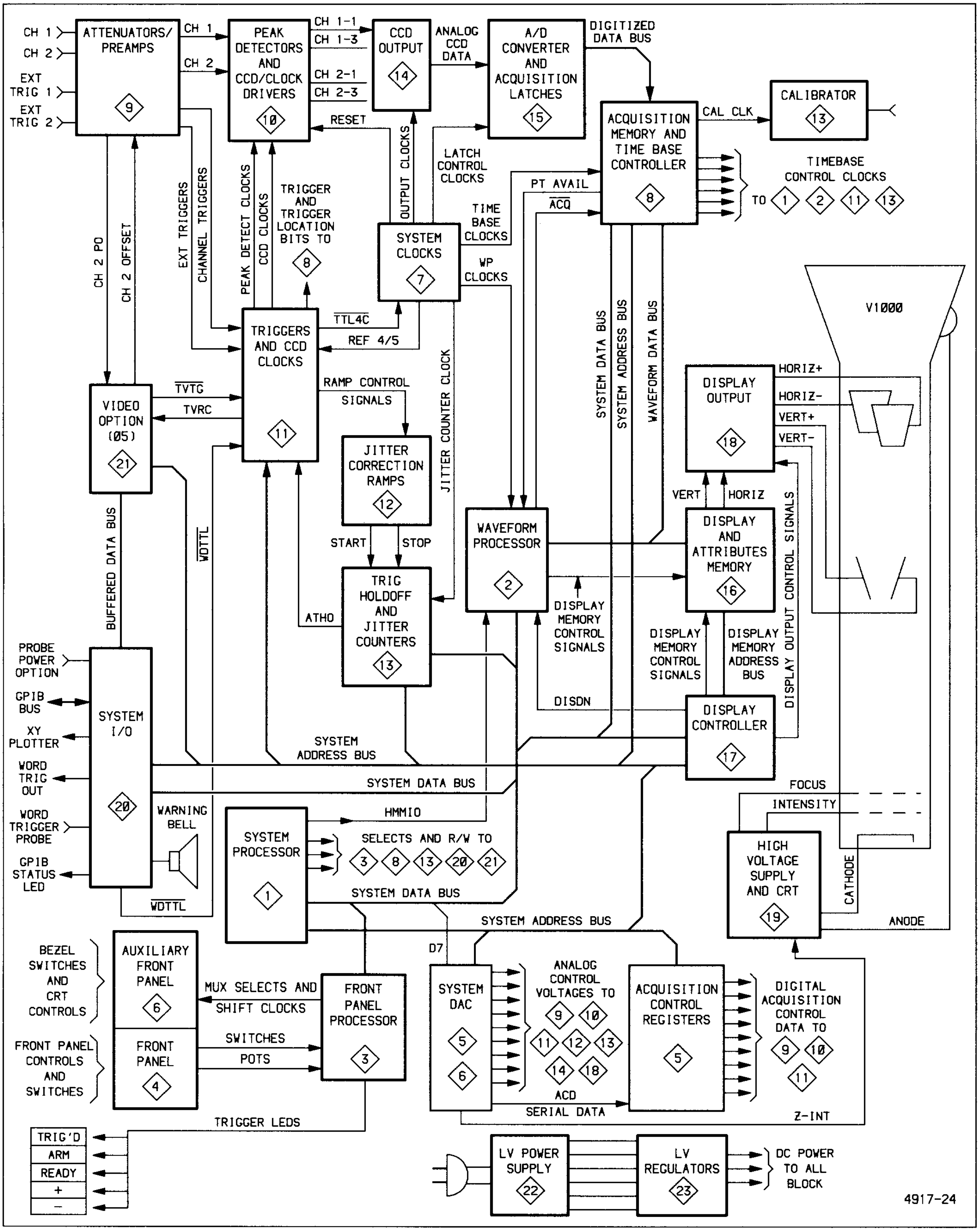


Figure 3-1. 2430 simplified block diagram.

Latches comes from the System Clock circuit and is referenced to the Output Clocks to maintain the correct data input to the magnitude comparators for making the Envelope min-max comparisons.

ACQUISITION LATCHES. For Normal and Average acquisitions, the data bytes are passed directly through the Acquisition Latches to the Acquisition Memory where they are stored temporarily before transfer to Waveform Processor Data Bus and the Waveform Processor Save Memory. The Envelope acquisition waveform bytes in the Acquisition Latches are the maximum and minimum data point values that occurred in the sampling interval. When the SEC/DIV setting reaches the maximum sampling rate, only one min-max pair is present during a sampling interval; and, in that case, the Envelope data byte comparisons are done by a firmware routine as the data is transferred from the Save Memory to the Display Memory.

Time Base Controller and Acquisition Memory (diagram 8)

ACQUISITION MEMORY. Digitized waveform data bytes are transferred from the Acquisition Latches to the Acquisition Memory under control of the Time Base Controller. The data is temporarily stored here before moving to the Waveform Processor Save Memory under control of the Waveform Processor.

TIME BASE CONTROLLER. The Time Base Controller, under direction of the System μP, monitors and controls the acquisition functions. When the pretrigger samples are obtained, the digitization process is started. Samples are counted to store the correct number in the Acquisition Memory, and the trigger point is properly located in the waveform record. Among the various tasks done by the Time Base Controller, Clock signals generated by the Time Base Controller provide the acquisition rate, the calibrator frequency, and enable the Trigger circuitry to accept a trigger after the pretrigger data is acquired.

Waveform Processor (diagram 2)

The Waveform Processor performs the high-speed data-handling operations required to produce and update the crt displays. Waveform data is transferred from the Acquisition Memory to a "Save" Memory in the Waveform μP work space. Waveforms may be digitally added, multiplied, or averaged, as part of the display processing that the Waveform Processor does before transferring the data to the Display Memory. The Save Memory is kept alive during periods of power-off by the stored charge on a "super cap." This short-term storage holds the Save waveforms, the reference waveforms and/or front-panel setups for a period of three to five days (nominal). The Waveform μP memory space and all devices on the Waveform μP address bus are addressable by the System μP via the Bus Connect circuitry for I/O operations.

The Bus Connect circuitry includes logic gating that arbitrates when the Waveform μP memory space (RAM) and addressable devices are under control of the System μP. The System μP may gain control by a BUS REQUEST to which the Waveform μP issues a BUS GRANT signal; or if the Waveform μP is held reset, the System μP issues a BUSTAKE signal. The BUSTAKE is used when the System μP writes a waveform display task list into the Waveform μP Command RAM space. When the reset is then removed from the Waveform μP, it does all the waveform data processing tasks given to it to do by the System μP without further need of System μP action.

Display and Attributes Memory (diagram 16)

The 512 data points to be displayed out of the 1024 data-point record are transferred to the Display Memory from the Waveform μP Save Memory after any required processing such as adding, subtracting, multiplying, or interpolating is done. Subsequent refreshes of the display are then continually made from data stored in the Display Memory, and that memory is only updated as necessary to display different waveforms or portions of the waveform record (a new horizontal position or new waveform called up for display). The Attributes Memory holds all the VOLTS/DIV and SEC/DIV scale factors for each of the waveforms displayed. Readouts of that data are also displayed on the crt. Waveform data to the XY Plotter is obtained directly from the Display Memory and only 512 data points for each waveform are available to be plotted.

Display Controller (diagram 17)

The Display Control System controls the display of the waveforms and readouts. Data bytes stored in the Display Memory are read out and D-to-A converted into vertical and horizontal current signals used to generate the waveform dots and readout characters. State-machine circuitry under control of the System μP performs all the display tasks assigned including control of the Z-Axis. The System μP and the Waveform μP are therefore free to carry on with other functions until it becomes necessary to make a display change (such as a menu or display mode change or a waveform data update). Display state-machine clocks are generated from the Time Base Controller 5 MHz clock signal.

Display Output (diagram 18)

Horizontal and vertical signal current from the Display Controller are converted into the deflection voltage signals used to drive the crt deflection plates by the Display Output circuitry. Vector generation circuitry provides a choice of either connected waveform dots (vectors on) or a dots-only waveform display. Display switching circuitry connects the correct deflection signals to the vertical and horizontal output amplifier for YT (vertical signal versus time), XY (horizontal signal versus versus vertical signal), or readout data. Dynamic offset correction of the vertical and horizontal output amplifiers is provided that minimizes trace shift due to intensity changes.

System Processor (diagram 1)

The System μP, under program direction, controls all the functions of the scope and coordinates the functions of the two other microprocessors (the Front-Panel μP and the Waveform μP). The System μP has a 16-bit address bus and a separate 8-bit data bus. No multiplexing of the data bus is required. Addresses are decoded to access the memory-mapped devices on the data bus, and control signals generated by the System μP control communication between the μP and the bus devices. An extensive interrupt circuit enables devices on the bus to request servicing when necessary to get new instructions or take other action. A power-up reset circuit permits an orderly power-on and power-off sequence of the System μP.

Permanent programming used to control the operation of the 2430 resides in the System ROM. The System ROM contains one 16K byte × 8-bit memory device and four 32K byte × 8-bit memory devices for a total of 144K bytes of memory. A page-switching scheme is used to permit the System μP to access all the available memory addresses of ROM.

System RAM consists of two memory devices. Temporary storage of data used in carrying out the various control functions is stored in the volatile System RAM. Nonvolatile storage of calibration constants and front-panel settings is provided by a battery-backup system for maintaining the memory during power-off in the nonvolatile RAM.

Front Panel Processor (diagram 3)

The Front Panel μP is a special-purpose device used to respond to switch and control changes. When a control changes, the Front Panel μP informs the System μP so that the operating state may be altered to match the requested change. Potentiometer controls are digitized to provide the necessary change data to the System μP. The System μP notes the control that changed, the amount and direction of change (if a pot), and sends out the necessary commands to make the change. New settings are updated in the nonvolatile RAM so that they will be available in the event of a power-off. On a power-on, the Front-Panel μP receives instructions as to how the switches are to be interpreted and then begins scanning the front panel, watching for a control to change. The System μP is then free to carry on with other functions.

Front Panel (diagram 4) and Auxiliary Front Panel (diagram 6)

All the buttons and knobs of the Front Panel and Auxiliary Front Panel are "soft" controls and do not directly activate a circuit function. This fact allows the switch functions and menu labels to be changed (especially the bezel buttons of the Auxiliary Front Panel which are used to make menu selections) as necessary. Buttons may be defined by the System μP to be push-push on-off, momentary contact, continuous, or toggle switches. Control changes are monitored by the Front Panel μP. Potentiometer controls are digitized; and when a change occurs, the amount and direction of change is sent to the System μP to make the appropriate operational changes. Push buttons that are pressed are interpreted as to what type of switch action occurred (from the switch-type definition list) and that information is sent to the System μP to make the appropriate operational changes.

All the buttons and knobs located to the right of the crt (facing the scope) are monitored via circuitry of the Front Panel. The Auxiliary Front Panel contains the circuitry required to monitor the bezel buttons (menu selection buttons), the push buttons, and the INTENSITY knob (all located directly beneath the crt). Probe coding for the vertical-channel and external-trigger BNC connectors and the 50 Ω overload circuits for CH 1 and CH 2 are also monitored via the Auxiliary Front Panel circuitry.

System Dac (diagrams 5 and 6)

The System Dac is used in normal operation to set the various analog control voltages throughout the instrument. Such things as preamplifier gain, vertical position and centering, trigger levels, holdoff time, common-mode adjust, scale illumination, intensity of the various crt displays, and CCD positions offsets are all controlled by the System μP via the System Dac. Digital values representing the analog voltage levels required for the various controls are written to the digital-to-analog converter (DAC) input registers where they are converted to analog voltage levels at the inputs to the Sample-and-Hold circuits. The Sample-and-Hold circuits maintain a fixed output voltage to the controlled circuit between updates by the System μP.

For calibration and diagnostic purposes, the System Dac is used to send known voltage levels to various circuits. Those levels may then be adjusted to remove offsets and set gain levels to achieve analog calibration or to test the gains and offsets for diagnostic purposes.

Acquisition Control Registers (diagram 5)

The Acquisition Control Registers are the digital control interface between the System μP and the switchable acquisition circuitry. Switching data is written to the

Registers to control the setup of the Peak Detectors, the A/B Trigger Generator, the Trigger Logic Array, and the Phase Clock Array. Additional decoding circuitry produces clocking signals used to load controlling data into Attenuator Register, the CH1 and CH2 Preamplifiers, and the A/B Trigger Generator.

Triggers and CCD Clocks (diagram 11)

TRIGGERS. The Trigger circuits detect when a trigger meeting the setup conditions occurs. Triggering signals are selectable by the A/B Trigger Generator from a choice of the following sources: CH 1, CH 2, EXT 1, EXT 2, and LINE. The Trigger Logic Array makes possible the further choices of TV Trigger ($\overline{\text{TVTG}}$), WORD Trigger ($\overline{\text{WDTTL}}$), or A and B Trigger. Upon receiving a valid trigger, the acquisition in progress is allowed to complete. Conditions for triggering, such as Level, Slope, Coupling, and Mode, are determined by the A/B Trigger Generator. Other triggering conditions such as delay by time, delay by events, and A and B Trigger are decided by the Trigger Logic Array which produces the output gates signaling a trigger event. The System μP sets up the operating modes for the A/B Trigger Generator and the Trigger Logic Array via the Acquisition Control Registers (diagram 5). Control signals to the Jitter Correction Ramps (RAMP and $\overline{\text{RAMP}}$) are generated by the Trigger Logic Array to start measuring the time between the sample clock and the trigger event. That time difference is used to correctly place the samples when repetitive sampling is used.

CCD CLOCKS. The CCD Clocks (used to move data into and out of the CCDs), the Peak Detector Clocks, the ramp-switching signals to the Jitter Correction Ramp circuits, and the trigger location bits (needed to place the trigger position with respect to the waveform data) are all generated by the Phase Clock Array. A master clock signal of either 200 MHz or 250 MHz is generated by the Phase-Locked Loop circuit and voltage-controlled oscillator. The master clock frequency needed is determined by the sampling rate at a particular SEC/DIV switch setting. Frequency dividers in the Phase Clock Array reduce the master clock frequency to the lower rates of the output clocks as determined by the System μP via the Acquisition Control Registers (diagram 5).

Jitter Correction Ramps (diagram 12)

The Jitter Corrections Ramps work in conjunction with the Jitter Counters to detect and measure the time difference between a trigger event (that occurs randomly) and the sample clock. That time difference is used to correctly place sampled data points into the waveform record when those samples are acquired on different triggers (repetitive sampling). Two ramp generators are used, so two time measurements are made. The System μP will determine which measurement is the one actually used. The RAMP and $\overline{\text{RAMP}}$ signals from the Trigger circuits control the start and stop of the ramp signals while the SLRMP1 and SLRMP2 signals control switching between the fast-charging current source and slow-discharging current source. Since the SLRMP signals are related to the sample clock, the amount of charge stored from the fast-charging current source before switching to the slow ramp occurs is a measure of the time difference between the trigger and the sample clock. The Jitter Counters start counting when the SLRMP signal switches to the slow ramp, and they are stopped when a comparator circuit determines that the ramp level has discharged to a fixed reference level.

Trigger Holdoff and Jitter Counters (diagram 13)

TRIGGER HOLDOFF. The A Trigger Holdoff circuit prevents the A/B Trigger Generator (diagram 11) from recognizing a new trigger event for a certain amount of delay time after an acquisition has been completed. The delay allows all of the data handling of the acquired samples to be completed before starting a new waveform acquisition. Minimum holdoff time is dictated by the SEC/DIV switch setting. A front-panel HOLDOFF control permits the user to increase the holdoff time as an aid in improving triggering stability on certain signals.

JITTER COUNTERS. The Jitter Counters (one for RAMP1 and one for RAMP2) start counting the 8 MHz clock when a START signal is received from the Jitter Counter Ramps switching circuit. That start occurs at the beginning of the slow ramp discharge. When the level of the slow ramp decreases to the fixed reference level, a STOP signal generated by a comparator in the Jitter Counter Ramps circuit halts the count. The 8-bit count bytes held in the Jitter Counters are then read by the System μP via address-selected bus buffers as two measures of the time difference between the trigger point and the sample clock. Since the timing between the two ramps is not identical (but both times are referenced), one measurement may have been made with better slope characteristics than the other (over a more linear portion of the discharge curve). The count producing the least ambiguity is used by the System μP to correctly position the waveform samples in the memory when repetitive sampling is done.

Calibrator (diagram 13)

The Calibrator circuitry shapes the CALCLK signal from the Time Base Controller to produce a signal with a faster rise and fall time and very precise amplitude. Frequency of the Calibrator signals changes (within limits) as the SEC/DIV switch changes. Signal amplitude is 400 mV (starting from zero), and the effective output impedance is 50 Ω.

System Clocks (diagram 7)

The System Clocks circuitry produces the fixed-frequency clock signals used throughout the scope. A 40 MHz crystal-controlled oscillator circuit produces the master clock signal that is divided down to provide the various system clocks that are needed. Some of the special clocks generated are the CCD Data Clocks, used primarily to switch the analog signal samples from the CCDs to the input of the A/D Converter and switch the converted data bytes to the Acquisition Latches. The reference frequency (either 4 MHz or 5 MHz) to the Phase Clock Array in the CCD Clock circuitry (diagram 11) is also selected by the System Clocks circuitry. A Secondary Clock Generator state-machine circuit produces three clocking signals to the Waveform μP to control the activity of that device.

High Voltage and CRT (diagram 19)

The High Voltage and CRT circuitry provides the auxiliary voltages needed by the CRT to produce a display. Focus, intensity, trace rotation, astigmatism, geometry, Y-Axis alignment, heater, and cathode-to-anode accelerating voltage are all provided by the various circuits included. These circuits are: the High Voltage Oscillator, the High Voltage Regulator, the +61 V Supply, the Cathode Supply, the Anode Multiplier, the DC Restorer, the Focus and Z-Axis Amplifiers, the Auto Focus Buffer, and the various crt adjustment potentiometers.

System I/O (diagram 20)

The System I/O circuits provide the interfaces between the scope and external devices that may be connected. Included in the interfaces is a standard general-purpose interface bus (GPIB) that permits two-way communication between the System μP and a GPIB controller or other IEEE 488-1980 compatible GPIB devices. The GPIB interface permits waveforms, front-panel setups, and other commands or messages to be both sent and received by the scope.

A second interface is the Word Trigger circuitry used to control the word recognization patterns of the optional Word Recognizer probe. All firmware and hardware (including connectors) required for use of the Word Recognizer probe is supplied as standard equipment. A trigger produced by the probe ($\overline{\text{WDTTL}}$) may be internally selected to trigger the scope, and it may be supplied to an external device via the WORD TRIG OUT connector on the rear panel.

A standard XY Plotter interface provides X-Axis, Y-Axis, and Pen Lift voltages to drive an analog plotter. The automatic Pen Lift voltage is polarity selectable for matching the requirements of the external XY Plotter. The output data normally plotted is the graticule, the SEC/DIV and VOLTS/DIV scale factors for each plotted waveform, and the actual waveform data being displayed. Both the graticule and the scale factors may be turned off to prevent them from being plotted.

Probe power connectors are an option for supplying the power requirement of active Tektronix probes. The option consists of two probe power connectors installed on the rear panel of the scope.

An audible alarm bell is provided to give the user warning of events that may require attention. GPIB errors are typical events that produce the warning bell so that a user may take notice of the error event. Another instance that causes the warning bell is an attempted call-up of an invalid operating condition from either the front panel or the GPIB. Typically, warning and error messages are also displayed on the crt to aid the user in determining the nature of the problem.

Video Option (diagram 21)

The Video Option (Option 05) consists of additional hardware installed in the base 2430 that enhances triggering on and viewing of composite video signals. Option 05 circuitry contains both Video Processing and Trigger Generation circuitry. Video Processing stabilizes the input signal and separates the video sync signals (horizontal and vertical sync pulses) from the video signal. A wide range of video signal levels are accommodated by using automatic gain control of the amplifier that sets the level into the sync separator. Separated sync pulse are counted to permit the user to select the line number that will produce a trigger event. Back-porch clamping is available for the Channel 2 display, and when used, it removes or reduces the level of power-supply hum that may be accompanying the composite video signal display.

Low Voltage Power Supply (diagram 22)

The majority of the low voltages required to power the 2430 are produced by a high-efficiency, switching power supply. Input ac power of either 115 V or 230 V within the frequency range of 48 Hz to 400 Hz is rectified and used to drive a switching circuit at a frequency of about 50 kHz. A smaller power transformer is possible with the higher frequency switching, and much more efficient power transfer is possible. Regulation of the power to the switching transformer is controlled by a pulse-width modulator (PWM) using feedback from one of the rectifier transformer outputs. The PWM controls the on-time of the switching transistors that deliver energy to the transformer primary winding. If the feedback voltage is too low, more energy is supplied by turning on the switching transistors longer. Automatic overvoltage and overcurrent sensing circuits shut down the switching if either type of overload occurs. The ac input has an interference filter, primary line fusing, and a thermal cutout that shuts down the power supply in the event of overheating.

Low Voltage Regulators (diagram 23)

The Low Voltage Regulators remove ac noise and ripple from the rectified output voltages from the power transformer. Each regulator automatically current limits the output and prevents the current from exceeding the normal power limits. This limiting prevents further possible damage to the power supply or other scope circuitry. Each of the power supply regulators controls its output voltage level by comparing the output to a known voltage reference level. To maintain stable and well-regulated output voltages, highly stable reference voltages are developed for making the comparisons.

DETAILED BLOCK DIAGRAM DESCRIPTION

INTRODUCTION

This description of the Detailed Block Diagram (found in the "Diagrams" section of this manual) provides an overview of the operation of many of the circuits and their functions within the 2430. The emphasis is on the acquisition system, and a "signal flow" approach is used as much as possible. No attempt is made in this discussion to specifically cover all the 2430 circuitry shown on the block diagram, though most is covered in general as it relates to those areas described in detail. The components discussed for each schematic diagram are generally outlined in functional blocks on their corresponding schematic diagram. These "function blocks" also appear on the "Detailed Block Diagram" within outlined areas that correspond to the schematic diagrams. Refer to both the Detailed Block Diagram and the Schematic Diagrams as needed while reading the following description.

INPUT SIGNAL CONDITIONING AND ANALOG SAMPLING

Signals applied to the CH 1 and CH 2 input connectors are coupled to their respective attenuators. The CH 1 and CH 2 attenuators (diagram 9) are settable for 1X, 10X, and 100X attenuation, with input-coupling mode choices of AC, DC, and GND. Input termination resistance of either 1 MΩ or 50 Ω is selectable with the DC input coupling choice. The attenuation factor, input coupling mode, and input termination settings for each input are controlled by the System μP (diagram 1) through the Attenuator Control Register (diagram 9), based on the Front Panel control settings chosen by the user.

The attenuated CH 1 and CH 2 signals are buffered by their respective Preamps (diagram 9) before they are passed on to the Peak Detectors. Preamplifier gain is controlled by the System μP using a serial control-data line via the Miscellaneous Register (diagram 1) and the DAC MUX (digital-to-analog converter multiplexer) Select circuit. Serial data is clocked into the internal register of the Preamps via the Control Register Clock Decoder (diagram 5). As with the attenuator settings, the gain-setting data output by the System μP depends on the user-selected Front Panel control settings. The range of attenuation settings coupled with the gain-control settings of the Preamps allows the complete range of available VOLTS/DIV switch settings (from 2 mV to 5 V) to be obtained.

In addition to signal gain and input signal buffering, the Preamps convert the single-ended input signal to a double-ended differential output signal that improves the common-mode rejection ratio. Input ports used to control the DC Balance, the Variable VOLTS/DIV gain, and the Vertical Position are provided in the Preamp stages. Analog control voltages to these inputs are developed by the System DAC and routed to the Preamps via the DAC MUX/0 Sample-and-Hold circuit (diagram 5). Trigger pickoff circuits in each Preamp provide a sample of the vertical signal that may be selected by the Trigger circuitry as the trigger signal source.

The differential output signals from the Preamps are applied to their corresponding Peak Detector. Input amplifiers within the CH 1 and CH 2 Peak Detectors (diagram 10) buffer the applied signals and provide a constant input resistance of about 75 Ω to those signals. The buffered signals are then either amplified further or "peak detected" and amplified, depending on the acquisition mode setting.

The System μP controls the operating mode of the Peak Detectors via control data writes to the Acquisition Control Registers (diagram 5). Some of the resulting digital outputs drive control inputs on the Peak Detectors, while others control the enabling and disabling of the Peak Detector clock signals from the CCD (charge-coupled device) Phase Clock Generator (diagram 11). The effect of this combined action depends on the acquisition mode selected. For NORMAL and AVG (average) acquisition modes, the peak-detect function of the Peak Detectors is disabled and the input signals are only amplified for application to the CCDs. For ENVELOPE mode, however, the peak-detect portion of the internal circuitry is enabled, and the maximum and minimum signal amplitude levels that occur during a sampling interval are detected. Those maximum and minimum values are then amplified and passed on to the CCDs.

Other inputs to the Peak Detectors control the input amplifier Bandwidth Limit setting (FULL, 50 MHz, or 20 MHz) and provide for the application of the calibration signal used for instrument calibration and self diagnostics. Calibration voltage levels applied to the Peak Detectors are generated by the System μP via the System DAC (diagram 5), DAC MUX 3, and the Cal Ampl circuit (diagram 6). The System μP selects between either the normal signal inputs or the calibration signal inputs using data written to the Acquisition Control Registers. The bandwidth of the input amplifiers of the Peak Detectors is also controlled via the Acquisition Control Registers, based on the user-selected Bandwidth Limit setting.

The signal-sampling process of CCDs (diagram 10) requires that two differential-signal pairs be available from each Peak Detector. Each CCD will use one or both output pairs as input signals, depending on the analog sampling mode. Briefly, the FISO sampling mode (fast-in, slow-out) requires 1056 samples to be shifted into each CCD. Half of the samples for a channel (528) are shifted into one side of one CCD, and the other half are shifted into the second side of the same CCD. The first pair of differential outputs are shifted into a pair of internal registers in one half of the CCD on the same phase of the sample clock. The second pair of differential output signals are identical to the first pair. This second pair is shifted into the two internal registers of the second half of the CCD on the opposite phase of the same sample clock used to shift in the first pair of output signals. This method of sampling produces a maximum sampling rate of 200 megasamples per second using a 100 MHz clock frequency. A second sampling method, called the "Short-Pipeline" mode, uses only half of each CCD and samples only one of the output signal pairs from the Peak Detectors. FISO and Short-Pipeline analog sampling modes are both discussed later in this description and in the "Time Base Controller and Acquisition Memory" portion of the Detailed Circuit Description.

Each differential output signal pair from the Peak Detectors is monitored by a separate Common-Mode Adjust circuit. These Common-Mode Adjust circuits (diagram 10) compare the common-mode voltage against the common-mode adjust voltage output by the System DAC. The common-mode adjust voltage is set by the System μP to control the overall gain of the CCDs based on calibration constants stored in the System μP nonvolatile RAM (diagram 1) as the result of a self calibration.

The common-mode adjusted signal pairs (two per Peak Detector) are applied to their corresponding side of the CCDs. There, they are analog sampled. The process consists of converting the analog voltages into individual, charged "packets" having a charge directly related to the voltage amplitude of the signal sample.

At SEC/DIV settings of 50 μs and faster, the signals are sampled at a faster rate than the maximum conversion rate of the A/D Converter. This mode is the "fast-in, slow-out" (FISO) sampling mode. When enough samples have been stored in the parallel register array of the CCDs to fill a waveform record after a trigger event, sampling stops (fast-in). The stored analog samples are then clocked out of the CCD arrays at a rate that the A/D Converter can handle (hence, slow-out). For SEC/DIV settings slower than 50 μs, the Short-Pipeline sampling mode is used. In Short-Pipeline, the acquisition rates are slower than the maximum digitizing rate of the A/D Converter. Samples are taken at a constant rate in Short-Pipeline mode, but to account for the slower acquisition rates needed for each successively slower SEC/DIV setting (from 100 μs to 5 s), samples that are not needed are ignored. Short-Pipeline mode is so named because the samples do not fill all of the parallel registers within the CCDs, but take a "short" serial path through the CCDs (see the "Detailed Circuit Description" for more information).

Analog samples are continually clocked into the CCDs by the output clocks of the CCD Phase Clock Array until a valid trigger is recognized by the Acquisition System. The Time Base Controller (diagram 8) provides the reference frequency to the CCD Phase Clock Array via the Reference Frequency Selector and the Phase-Locked Loop circuit (diagram 11). Dividers in the CCD Phase Clock Array synthesize the clocking frequencies needed for saving the acquisition at the different SEC/DIV settings. The Time Base Controller also controls the acquisition mode (FISO, Short-Pipeline, or ROLL) and the storing of acquired samples into the Acquisition Memory.

At this point in the sampling process the Time Base Controller is waiting for a triggering gate from the Trigger System to complete the acquisition (see "Acquisition Process and Control"). Extra pretrigger samples acquired while waiting for a trigger will either be flushed out of the output wells of the CCDs (FISO mode) or converted and stored in the circular Acquisition Memory (diagram 8), but not moved to the Save Memory (Short-Pipeline mode). The exception to this is ROLL mode; a trigger event is not required for ROLL acquisitions. Digitized data is moved through the Acquisition System to continually update the display with each waveform data point acquired.

ACQUISITION PROCESS AND CONTROL

To do a waveform acquisition, the System μP addresses the internal instruction registers within the Time Base Controller and then writes the setup data into the registers. The setup data defines the acquisition mode (FISO, Short-Pipeline, or ROLL), the time base clocking rate (for the SEC/DIV setting), the trigger position, and other instructions for how an acquisition is to be made.

Once the setup data is in the Time Base Controller instruction registers, the System μP generates a strobe that starts the acquisition and turns control of the Acquisition System over to the Time Base Controller. The Time Base Controller then begins monitoring the CCD Phase Clocks to determine when an adequate number of analog samples are in the CCDs to fill the pretrigger requirements. When those samples have been obtained, the Time Base Controller enables the Trigger Logic Array (diagram 11) to accept a trigger and begins looking for a triggering gate from the Trigger Logic Array (via the CCD Phase Clock Array). This waiting period is the continuous analog sampling state for the CCDs referred to at the end of the "Input Signal Conditioning and Analog Sampling" discussion.

With the Trigger System enabled, the A/B Trigger Generator (diagram 11) monitors the selected source for a signal that meets the analog triggering criteria. Source selection and triggering criteria are controlled by serial data writes from the System μP (via the Data MUX Select circuit) based on the Front Panel settings selected by the user. When the analog triggering conditions are met, the A/B Trigger Generator gates the Trigger Logic Array. Once enabled, the Trigger Logic Array monitors other triggering criteria (Trigger Mode, Delay Time setting, Hold Off timing, etc.) to determine the actual "Record" trigger point in the waveform data record. The System μP writes data control bits defining the Trigger Logic Array operating mode to the internal registers of the Trigger Logic Array via the Acquisition Control Registers.

When the Trigger Logic Array determines that the additional triggering conditions are also met, the Time Base Controller is gated (via the CCD Phase Clock Array), and the post-trigger samples are taken (if required) to finish the acquisition. How the acquisition is completed after the trigger point is determined, depends on the analog sampling mode in effect.

FISO Mode

For FISO mode, the CH 1 and CH 2 CCDs must each hold 1024 samples (plus some extra samples used in locating the correct trigger point). After the trigger event, the Time Base Controller counts a sampling clock from the CCD Phase Clock Generator to determine when enough post-trigger samples have been shifted into the CCDs to finish the acquisition. When the record is filled, the analog sampling process is stopped by disabling the sampling clocks output by the CCD Phase Clock Generator. Converting the stored analog information into digital data and saving it into the Acquisition Memory is then started. Both the "conversion" and "save" aspects of the acquisition process are discussed in "Analog Data Conditioning and A/D Conversion" and "Acquisition Processing and Display."

Short-Pipeline Mode

For Short-Pipeline acquisitions, each CCD can contain only 37 samples before the "pipe" is full. This means that samples must be continuously shifted through the digitizing process and into Acquisition memory as the samples are being taken. Since the pretrigger and post-trigger distribution of the data in the acquisition record is not defined until a trigger occurs, converted data is continually stored in the Acquisition Memory. If the Acquisition Memory space should become filled before a trigger occurs, newly acquired data will simply displace the old in a circular manner (oldest data replaced first). After a trigger, the Time Base Controller counts another sampling clock to determine when enough samples have been moved into the Acquisition Memory to satisfy the post-trigger requirements and then turns the Acquisition Memory space over to the Waveform μP. The Waveform μP transfers the samples into the Save Memory for eventual display.

DATA CLOCKING TO ACQUISITION MEMORY

FISO Mode

In FISO mode, the Time Base Controller signals the CCD Phase Clock Array (U470, diagram 11) to begin clocking waveform samples out of the CCDs. The Time Base Controller monitors the Trigger Location signals from the CCD Phase Clock Array to determine precisely where in the acquisition the trigger occurred. When the samples not needed to fill the 1024-point waveform record have been clocked out so that only the samples properly positioned around the trigger point remain in the CCD, the Time Base Controller enables the save acquisition clocking to begin moving the digitized samples from the A/D Converter into the Acquisition Memory, thus saving the waveform record. (See "Detailed Circuit Description" for more trigger point location information.)

To do a waveform save, the Time Base Controller is selected to control writing into the Acquisition Memory via the Memory Mode Control circuit (diagram 8). The $\overline{\text{SAVEACQ}}$ clock circuitry is then enabled to pass a 2 MHz clock signal ($D_2$4XPC) from the CCD Data Clock circuit (diagram 7) to do the memory writes at the FISO rate.

The memory write clock also increments the Acquisition Memory Address Counter to provide the address for writing the next data point into the Acquisition Memory. The address is latched into the Record-End Latch during each memory write so that the beginning of the acquisition record can be determined when the Acquisition Memory is accessed later.

As the samples are being moved into the Acquisition Memory, the Time Base Controller monitors clocks from the CCD Data Clock circuit to determine when the 1024 digitized samples (per each channel) are saved. The Time Base Controller then stops writing to the Acquisition Memory by disabling the write clock and switches control of the memory to the Waveform μP (again, via the Memory Mode Control circuit). The Time Base Controller then strobes the Waveform μP (diagram 2) to signal that the acquisition is complete and the waveform data is available for processing and display.

Short-Pipeline Mode

For Short-Pipeline mode, the Time Base Controller generates an enabling clock that controls the 2 MHz write clock to the Acquisition Memory. The correct enabling rate of the $\overline{\text{SAVEACQ}}$ write clock for the selected SEC/DIV setting is synthesized within the Time Base Controller, using a CCD Data Clock input to obtain the base frequency. This enabling clock turns on the controlling gate circuit to pass only two $\overline{\text{SAVEACQ}}$ clocks (via the Mode Control Circuit) to write to the Acquisition Memory, saving one digitized data point per channel (two in Envelope Mode—one max and one min per channel). Then the synthesized clock from the Time Base Controller disables the $\overline{\text{SAVEACQ}}$ clock for a certain number of clock cycles. Specifically, the number of ungated clock cycles equals the SEC/DIV setting divided by 50 μs, i.e., four clock cycles at a SEC/DIV setting of 200 μs. Therefore, the samples saved in the Acquisition Memory in Short-Pipeline mode produce a constant 50 samples per horizontal division when displayed, regardless of the SEC/DIV setting.

The remainder of the Short-Pipeline save operation is similar to a FISO save. The Acquisition Memory Address Counter is incremented by the clock that writes data to the memory as in FISO, but at the synthesized rate rather than at the 2 MHz FISO rate. As in FISO, the Trigger Location information is used to determine the trigger point location. Enough samples are saved into memory after the trigger point is found to fill the post-trigger requirements before turning control over to the Waveform μP.

ANALOG DATA CONDITIONING AND A/D CONVERSION

Both pairs of the differential output signals from the CH 1 and CH 2 CCDs are applied to the inputs of the corresponding pairs of Single-Ending Amplifiers (diagram 14). Each amplifier converts the differential signal clocked to its inputs to a single-ended output signal. That signal is used to drive the input of a corresponding Sample-and-Hold circuit (also shown on diagram 14).

The CCD Data Clocks and the CCD Output Sample Clocks (diagram 7) control the timing between when the signals are coupled to their corresponding Sample-and-Hold circuits and when the Sample-and-Hold circuit outputs are coupled to the single analog input of the A/D Converter (diagram 15). Briefly for FISO mode, the timing is as follows:

1. A CCD Output Sample clock gates the outputs of both CH 1 Single-Ended amplifiers to the input of their associated Sample-and-Hold circuit. There, the input levels are sampled, and the gating is then disabled to hold the sampled level on the Hold capacitors. One of the CH 1 Sample-and-Hold output circuits is then gated on to pass the sample level to the A/D Converter for digitization.

2. While the output level of the first CH 1 Sample-and-Hold is gated to the A/D Converter, a CCD Output Sample clock gates the outputs of the CH 2 Single-Ended Amplifiers to their corresponding CH 2 Sample-and-Hold circuits. Both the first CH 1 Sample-and-Hold outputs and the inputs to the CH 2 Sample-and-Hold circuit are then ungated, and the first CH 2 Sample-and-Hold output circuit is gated on to pass its held signal level to the A/D Converter.

3. The first CH 2 output is then ungated, and the second CH 1 Sample-and-Hold output and the second CH 2 Sample-and-Hold output are gated on in succession to couple their held levels to the A/D Converter. This multiplexing process continues until 512 samples from both sides of the two CCDs have been converted.

NOTE

The samples are clocked through each side of the CCD at a 500 kHz rate, resulting in an output sampling rate of 1 MHz per channel. Also note that the 4-to-1 gating of the two channels and their respective outputs results in a 2 MHz time-multiplexed (4-to-1) signal to the A/D Converter.

For Short-Pipeline sampling mode, the gating for the inputs to the Sample-and-Hold circuits is the same as in FISO mode. However, since only one side of each CCD is used per channel, only one pair of differential outputs (per CCD) and the corresponding Single-Ended Amplifier and Sample-and-Hold circuits transfers valid waveform samples to the A/D Converter. The Short-Pipeline mode save-acquisition clocking ensures that only the valid converted data is saved (see "Short-Pipeline Mode" in "Acquisition Process and Control"). Observe, however, that the signal to the A/D Converter is still a 2 MHz time-multiplexed signal, but with invalid data half of the time. Since the invalid data is, in effect, discarded by the Short-Pipeline Mode save-acquisition clocking, the A/D Converter continues to operate at a constant 2 MHz conversion rate as in FISO mode.

The time-multiplexed signal is applied to the input of the A/D Converter circuit for digitization. The System Clocks circuit (diagram 7) provides a 2 MHz clock to the converter, for a 2 MHz data-conversion rate of the input signal. The resulting digital output byte is applied in four 8-bit bytes to the Acquisition Latches (diagram 15).

For Normal and Average Acquisition Modes, data is clocked into the Acquisition Latches by the same 2 MHz clock used by the A/D Converter. Enabling of the outputs of the Acquisition Latches is controlled by the CCD Data clocks in a sequence that ensures that the data clocked out from the enabled latch corresponds to the CCD side and Sample-and-Hold circuit that provided it. The 8-bit sample bytes are then saved in Acquisition memory in the same order they were obtained. This "structured" method for saving acquisitions keeps the data in the correct time sequence for display.

For Envelope Mode, the Time Base Controller disables continuous gating of the 2 MHz clock to the Acquisition Latches. This action turns over the gating of that clock to the Envelope Min-Max Comparators (diagram 15). With the 2 MHz clock ungated, the CCD Data Clocks will continue to control the enabling of the outputs of the acquisition latches as described, but the new data bytes are not continually clocked into the latches. The result is that only the data bytes clocked in by the Envelope Min-Max Comparators are sequentially clocked to the Envelope Data bus in the following manner: CH 1 max, CH 2 max, CH 1 min, CH 2 min. This is the same order in which the analog samples are clocked into the A/D Converter.

The output of the A/D Converter is fed to the Envelope Min-Max Comparators (diagram 15). The outputs of the Acquisition Latches are also fed back to those comparators. Due to the previously described timing action of the CCD Data Clocks, the newly digitized minimum or maximum value from the Peak Detectors (see "Input Signal Conditioning and Analog Sampling") is compared to the last value latched into the Acquisition Latch that corresponds to the new point. If the newly acquired point is outside the previous min or max value, the appropriate Envelope Min-Max Comparator gates the 2 MHz clock, and the new data byte is latched into the corresponding acquisition latch.

ACQUISITION PROCESSING AND DISPLAY

Data Transfer to SAVE Memory

Once the 1024 digitized signal bytes per channel are in Acquisition Memory, the Time Base Controller ungates the $\overline{\text{SAVEACQ}}$ clock and switches the the Memory Mode Control circuit to the Waveform μP. It also signals the Waveform μP, via the Display Status Buffer (diagram 2), that the acquisition is complete. The Waveform μP can then access the Acquisition Memory.

When the Waveform μP reads the acquisition done (ACQDN) signal from the Time Base Controller, it writes an address (via the Address Latch) which is decoded by the Register Address Decoding circuit (diagram 2). The decoded address signals the Record-End Latch (diagram 8) to enable its contents (the last addressed memory location for the stored acquisition) to the Waveform μP data bus to be read to determine the location of the last record byte stored. The Waveform μP then uses that location to determine the location of any byte in Acquisition Memory.

The Waveform μP outputs (via its Address Latch) addresses to the Address Counter for Acquisition Memory. The Address Counter is held in its load mode by the Waveform μP (via the Memory Mode Control circuit), passing the address through to Acquisition Memory. The Waveform μP enables the Acquisition Memory and provides the clocks (via the Memory Mode Control circuit) to move stored data out to the Waveform Data bus via the Data Bus buffer. This data is written either into the

Waveform Save Memory or into an internal register of the Waveform μP for processing, depending on the display requirements.

Most transfers from Acquisition Memory are straight out of Acquisition Memory, through the Waveform Data Buffer, and into a corresponding memory location in Waveform Save Memory. However, the Waveform μP sometimes disables the Waveform Data Buffer and reads the data directly into its own internal register via the Data Bus Buffer. The Waveform μP then processes it according to tasks assigned by the System μP, using routines stored in its own ROM. For instance, in Envelope mode the Waveform μP will read (into a second internal register) the corresponding byte stored in Waveform Save Memory from the previous acquisition. If the new byte, stored in the first internal register, is determined to be a new max or min value, the Waveform μP uses it to replace the previous value in Waveform Save Memory.

It should be noted that the Waveform Save Memory is a paged RAM memory. The Waveform μP uses a paged address scheme to load waveform data into one of six possible sections, depending on the source (CH 1 or CH 2) or the destination (REF1, REF2, etc) of the waveform. Observe also that the Waveform Save Memory RAMs are supplied power by the Standby Circuit when instrument power is off, allowing for preservation of the waveform data stored in each of the six sections. See the "Detailed Circuit Description" for more information concerning the structuring of the Waveform Save Memory and operation of the Standby Power circuit.

Data Transfer to Display Memory

Once an acquisition is stored in the Waveform Save Memory, it must be moved to the proper locations in Display Memory, from where it is converted back to an analog signal for display. The Waveform μP updates each section of Display Memory at the proper time, based on internal routines stored in Waveform Processor ROM and timing supplied by the Secondary Clocks via the Waveform Processor Clock and Bus Grant Decoding circuit. The Waveform μP also writes attribute changes (such as changes in horizontal position) to the Display Memory (when assigned the task by the System μP).

The Waveform μP addresses (in parallel) both the Waveform Save Memory and the Display RAMs via the Address Multiplexer (diagram 17). The System μP gates the address through to the Display Memory (the Vertical, Horizontal, and Attribute RAMs on diagram 16) via the Display Control Register (diagram 17). The Waveform μP then clocks the data out of its memory into the appropriate Display RAM.

Data Transfer to Display DACs

When the System μP initiates the display of the data stored in Display Memory, it writes (via its data bus) the starting address of that data to the Display Counter (diagram 17). It also outputs an address that latches, via the Register Select Circuit, the starting address into the Display Counter. Simultaneously, data from the System μP initiates, via the Display Control Register (diagram 17), a strobe to the Display State Machine. The Display State Machine then signals the Address Multiplexer, gating the address(es) output by the Display Counter through to Display Memory (diagram 16), and begins to gate a clock from the Display Clocks circuit to the Display Counter. The Display Counter increments for each (display) clock cycle, accessing successive addresses in Display Memory as the System μP clocks the data out of Display Memory.

The System μP uses data writes to the Mode-Control Register (diagram 17) to select which portion of the Display Memory (Vertical, Horizontal, or Attribute) or which register (Volts Cursors or Time Cursors) is selected for output to the Vertical or Horizontal DACs. The System μP also uses the Mode-Control Register to select, via the Horizontal Data Buffers, whether the waveform data in the Horizontal Ram is applied to the Horizontal or Vertical DAC, allowing either YT or XY displays.

It should be noted that the incrementing addresses supplied via the address latch are also applied to the Ramp Buffer. Since each incremental address corresponds directly to the data byte it addresses, and since the output of the Ramp Buffer (diagram 16) will be converted to a staircase waveform by the Horizontal DAC, the addresses can provide the horizontal deflection (or "ramp") necessary for YT displays.

Data Display

Data, waveform or other, is converted to two complementary output currents by each Display DAC. These currents are analog in nature, but reflect the ±256-bit resolution of the DACs. Therefore, the current outputs are a series of discrete analog levels (or steps, if the current is varying), each level corresponding to the 8-bit byte applied to the DAC.

The differential current outputs from the Horizontal and Vertical DACs are converted to single-ended voltages at the input to the Display Output circuitry. Those voltages then drive either the corresponding Horizontal and Vertical Vector Generators (diagram 18) for vector displays or the Horizontal and Vertical Output Amplifiers directly for dot displays.

The Vector Generators consist of a High-Current Difference Amplifier, a Sample-and-Hold circuit, and a Integrator to produce the vectors that connect the sample points in the display. Signals for vectored displays are continuously sampled and held, and integrated. The input voltage integrated is the difference between the voltage level of the sample presently being held and the intergrated level of the sample immediately preceding it. This action allows a smooth transition between the individual steps for a continuous display.

A Display Mode Switcher selects between the Vector Generator signals, a dots-only signal or an envelope display signal. With Envelope mode selected, the signal is passed through an rc integrator that produces vectors between the min-max data points of the Envelope Mode display.

The System μP, based on Front Panel settings, selects the display mode for the Vertical and Horizontal Vector Generators. The selected input, either Vector, Dot, Envelope, or Readout inputs, from each Vector Generator is coupled through to its corresponding Vertical or Horizontal Output circuit (diagram 18). There they are amplified and converted from single-ended to double-ended, to drive the Vertical or Horizontal plates of the crt (diagram 19). Both Vertical and Horizontal Output circuits have voltage offset and gain adjustments and are compensated for "spot wobble" (variations in beam placement on the crt screen with variations in beam intensity) by the Intensity circuit (diagram 6) via the Spot-Wobble Correction circuit.

DETAILED CIRCUIT DESCRIPTION

SYSTEM PROCESSOR

The System Processor (diagram 1) is the control center of all operations in the 2430. It consists of an 8-bit microprocessor (μP), an 8-bit data bus, a 16-bit address bus, a prioritizing interrupt system, hardware address decoding, "nonvolatile" and volatile RAM space, and 144K bytes of bank-switched ROM.

The System Processor circuitry also coordinates the functions of the two other microprocessors in the 2430, the Waveform Processor and the Front Panel Processor.

System μP

System μP U640 executes instructions stored in the System ROM in order to initiate and control the various functions of the 2430. Internally, the microprocessor has 16-bit data paths; externally it has an 8-bit data bus for communication and a separate 16-bit address bus. No address/data bus demultiplexing is necessary. The μP is driven by an external 8 MHz clock that is divided by four internally for a 2 MHz cycle rate. The number of cycles per instruction varies from a minimum of 2 to a maximum of 20, with the average being about 4 cycles per instruction. The μP executes, on the average, 1/2 MIP (Million Instructions Per second).

System μP U640 generates three signals used to control the communication activities of external circuitry. Of these signals, E and Q are for timing purposes. The rising edge of Q signals that the address on the bus is valid; data to the μP is latched on the falling edge of E. The third signal generated is the R/W signal. It is valid the same time the address is valid, and its state (LO or HI) determines whether an addressed device is written to or read from.

The E signal (U640 pin 34) and the Q signal (U640 pin 35) are ORed together by U840D to generate the HVMA (Host Valid Memory Address) signal. When HVMA at U840D pin 11 is HI, the address on the bus is valid. Once the external circuitry receives a valid address signal, it proceeds with the specified memory access. The signals used throughout the 2430 to enable and time these accesses are $\overline{\text{RD}}$ (read) and $\overline{\text{WR}}$ (write).

The $\overline{\text{RD}}$ signal is derived from U844A, which NANDs the HVMA signal with the μP R/$\overline{\text{W}}$ signal. Inverting buffer U572C provides added driving power to the R/$\overline{\text{W}}$ signal, and inverting buffer U884B reinverts it back to its original polarity before it is applied to NAND-gate U844A. The output of U844A is the $\overline{\text{RD}}$ signal, whose falling edge indicates the start of a read cycle. The rising edge of $\overline{\text{RD}}$ is coincident with the latching of the data read into μP U640.

The $\overline{\text{WR}}$ signal is derived from an inverted version of the μP R/$\overline{\text{W}}$ signal (via U572C) with a buffered μP Q signal (via U880D) NANDed by U844B. The output of this NAND-gate is a signal with a falling edge that indicates the start of a write cycle to the addressed device and a rising edge that latches data from the μP into the addressed device. The Q signal is used here instead of HVMA (as was used to generate $\overline{\text{RD}}$ to produce a data hold time of more than 100 ns as needed by the oscilloscope Time Base Controller circuitry.

Data Bus Buffer

Data Bus Buffer U650 provides buffering of the data bus lines. It is bidirectional to enable two-way communication between the System μP and the data bus. In normal operation, jumper J126 will connect the chip-enable pin to ground, and the buffer is enabled to transfer data. The direction of the transfer is controlled by the R/$\overline{\text{W}}$ signal from the System μP via inverting buffer U572C.

Moving test jumper J126 to its "KERNEL" position disables buffer U650 and forces it to its tri-state (high-impedance output) mode. The pull-up and pull-down resistors on the data bus lines, R742, R746, and R744, place an instruction byte on the μP data bus that causes the μP to repeatedly increment the addresses placed on its address bus lines through their entire range. This procedure is a troubleshooting aid that exercises a good portion of the address-decoding and chip-select circuitry.

Address Buffers

Address Buffers U632 and U730 provide buffering of the System μP address lines to the various addressable devices. The buffer chips are permanently enabled and provide both current buffering and electrical isolation for the address lines. Test point TP840 is provided as a source of an oscilloscope trigger signal when checking the incrementing address lines in the forced "KERNEL" troubleshooting mode described in the "Data Bus Buffer" description.

System ROM

The System ROM (read-only memory) stores the commands and data used by System μP U640 to execute its control functions. The System ROM is made up of one 16K byte x 8-bit memory device, U670, that contains the System μP operating system, and four page-switched, 32K byte x 8-bit memory devices, U680, U682, U690, and U692 used for storage of all the additional operating routines. This gives a total of 144K bytes of ROM space. Each ROM is individually enabled by the ROM Select circuitry, and the addressed data will only appear on the system data bus when the $\overline{RD}$ (read) signal goes LO. Since μP U640 has the capability to address only 64K locations and has to address other things besides ROM, the System ROM is split into nine pages. Address decoders U890A, U890B, and part of PC Register U860, select the page of ROM to be read from to allow the System μP to access the entire 144K byte ROM space.

Immediately after the power-up reset ends, μP U640 automatically tries to fetch the reset vector (the location of the first program instruction) from locations FFFE(hex) and FFFF(hex) in its address space. Anytime the System μP tries to access memory, the HVMA (host valid memory address) signal from U840D will be HI during the time the address is guaranteed to be valid. Addresses FFFE and FFFF have bits AE and AF (the two MSBs of the address bus) set HI; therefore, with the HVMA signal HI, NAND-gate U870D outputs a LO that enables U890A, and a $\overline{ROM1}$ select output is obtained from U890A for both addresses. The $\overline{ROM1}$ applied to the chip-enable input of ROM U670, along with the LO $\overline{RD}$ applied to its output enable, outputs the two 8-bit data bytes from location FFFE and location FFFF onto the system data bus via bus transceiver U660. The address contained in these bytes directs the μP to the start of its program, and the program is started.

When the μP needs information from one of the other System ROMs, it writes three bits of select data into register U860. Of these bits, PAGE-BIT0 and PAGE-BIT1, applied to 1-of-4 Decoder U890B, select which ROM chip of ROM0 is enabled. PAGE-BIT2 is the most significant bit of the ROM addresses and determines which page of the enabled ROM is addressed. The applied bit levels produce a ROM select for one of the 32K ROM chips when data selector U890B is enabled by U890A. This enabling occurs when an address between 8000h and BFFFh is output by μP U640, causing U890A to produce its $\overline{ROM0.X}$ output to U890B. Page switching in this way permits eight 16K-byte pages of ROM to reside between addresses 8000h and BFFFh. The ROM selected depends on the states of the three PAGE-BITS written to PC register U860. These ROM select bits are initialized LO by the RESET signal from the Power-Up Reset circuit when the oscilloscope is turned on.

Power-Up Reset

The Power-Up Reset circuit keeps the System μP reset until all instrument power supplies are sure to be operating properly and for the 100 ms delay needed by μP U640. This delay time is enough that the processor will begin the operating program with all electrical components in valid (defined) states after the instrument is turned on.

The Power-Up Reset circuit consists of an RC-integrator formed by R936 and C938 and a comparator circuit formed by U940B and associated components. Capacitor C938 begins charging when the PWRUP (power-up) signal goes HI, and the comparator detects when this charging level crosses a predefined threshold voltage (set by R944, R943, and R942). Positive feedback through R942 separates the turn-on and turn-off thresholds of comparator U940B to ensure that switching of the comparator is positive when the threshold level is reached. The turn-on circuit delay of approximately 100 ms allows all electrical components to stabilize before attempting any circuit operations.

On power-down, the PWRUP line is immediately pulled LO, and capacitor C938 begins discharging via R938 and diode CR936. At the time this discharge is initiated, the $\overline{NMI}$ (nonmaskable interrupt) is asserted, and the processor branches to the power-down routine. In the power-down period before the power supplies are discharged, the μP does the housekeeping activities that ensure the data stored in Nonvolatile (NV) RAM is correct and turns off any asserted 50-ohm input coupling. After approximately 10 ms of discharging, the $\overline{RESET}$ line is asserted to hold the μP reset while the power supplies finish their discharge. If power to the System μP is not lost but merely reduced, approximately 260 ms after $\overline{NMI}$ goes LO, the System μP will fetch its reset vector and restart as though the power was actually cycled off and then back on.

Interrupt Logic

The Interrupt Logic circuit provides a means by which other sub-systems may interrupt the normal program execution being done by the μP to request service. Three levels of interrupts are available in μP U640. The $\overline{NMI}$ (nonmaskable interrupt) that occurs at power-down has priority over the other two interrupt levels. If either of the other interrupts is present at the same time as the NMI, the μP gives preference to the NMI and immediately branches to the power-down routine. The power-down routine performs the operations necessary for an orderly shut-down of the scope. A cyclical-redundancy checksum of the data stored in Nonvolatile RAM is calculated and stored back into that RAM. On power-up, that checksum is used to verify the validity of the parameters and settings stored in the Nonvolatile RAM. To prevent a possible 50-ohm overload of the Channel 1 or Channel 2 input circuitry during times that the instrument is off, part of the power-down routine is to make certain that input coupling is set to a high-impedance state.

The next interrupt in priority after the NMI is the FIRQ (fast-interrupt request). It is produced by flip-flop U894A in response to a 2 ms clock signal from the Time Base circuit (diagram 8). The 2 ms clock sets the FIRQ line LO every 2 ms to signal μP U640 that it is time to do the time-critical tasks like updating the DAC System. When the fast-interrupt request has been serviced, the μP clears the FIRQ latched into U894A by outputting address 6012h. This address is decoded by 1-of-8 Decoder U884 to generate a CLRFIRQ (clear fast-interrupt request) signal that resets flip-flop U894A. Servicing of a fast-interrupt request differs from other interrupt requests in that the contents of only two μP registers are pushed to an internal stack (instead of all the μP registers), allowing the μP to respond faster.

The lowest priority is given to the combined signal forming the IRQ (interrupt request). This interrupt allows various sub-systems to get attention from the System μP. NOR-gate U850B outputs a LO when any of the five conditions occur. Inputs to NOR-gate U850B are from: the GPIB (General Purpose Interface Bus), the Display circuitry, the Front Panel, the Waveform μP, and the Trigger System. Of these, the latter three interrupts may be masked off (disabled) by the μP by writing LO mask bits into register U760 which are then applied to AND-gates U880A, U880B, and U880C. A LO input to one input of an AND-gate holds the associated output pin LO and prevents an interrupt signal from being gated through to NOR-gate U850B. The Waveform μP may mask the Display System interrupt (DISDN) from the System μP by placing a LO on pin 5 (MDISDN) of AND-gate U580B from register U550 (diagram 2). The Waveform μP thereby can gain first access to the Display System if it needs to do display updates before the System μP sees that the Display System is finished with its last task. When the Waveform μP is done, it writes the MDISDN interrupt HI to let the System μP know that it is finished with the Display System and the Display System is ready to be restarted.

When an IRQ interrupt is detected, the μP executes a read of location 6010h which is the address of Interrupt Register U654 (an octal buffer). That address is decoded by 1-of-8 Decoder U884 to set INTREG LO and enable U654. The enabled buffer passes the status of the various interrupt lines at its inputs to the data bus for the μP to read. From the status bits read, the μP determines which circuit caused the interrupt and branches to the called for interrupt service routine. If more than one interrupt is pending, the System μP IRQ interrupt handling routine decides which one needs to be (or can be) handled first. The order in which it handles these interrupts depends on the current activity of the System μP.

Besides interrupt status, three other status bits are read from the Interrupt Register. These are the DCOK (dc ok) signal from the power supply (check during the calibration routine register checks), BUSGRANT from the Waveform μP, and FPDNRD. DCOK signifies that the various power supply voltages are within proper limits; BUSGRANT indicates that the Waveform μP has relinquished bus control in its operating space and that those addresses are now mapped into the System μP address space. FPDNRD indicates that the Front Panel μP has read the data sent to it from the System μP.

System Address Decode

The System Address Decode circuit generates specific enables and clocks when certain addresses (or blocks of addresses) appear on the μP address bus. Figure 3-2, a simplified memory map, illustrates the areas addressed by blocks.

To permit the System μP to control the hardware functions of the 2430, several control registers have been assigned to unique addresses within the μP address space (memory-mapped). These registers appear as blocks of read-only, write-only, or read-write memory to the System μP. The data bits handled by these registers control specific hardware functions, and the commands written will not violate any hardware restrictions.

A block of addresses from 6000h to 6FFFh corresponds to the host memory-mapped input/output (HMMIO) block. Addresses within this block are decoded to produce a LO HMMIO signal to 1-of-8 Decoder U884 and Octal buffer U830. The three MSBs of the I/O address block and the HVMA (host valid memory address) are decoded by AND-gate U862 and inverter U866C to output a HI level for addresses between 6000h and 7FFFh. This output is NANDed by U870B with the inverted AC (address bit C) line from U866A to decode the I/O addresses between 6000h and 6FFFh.

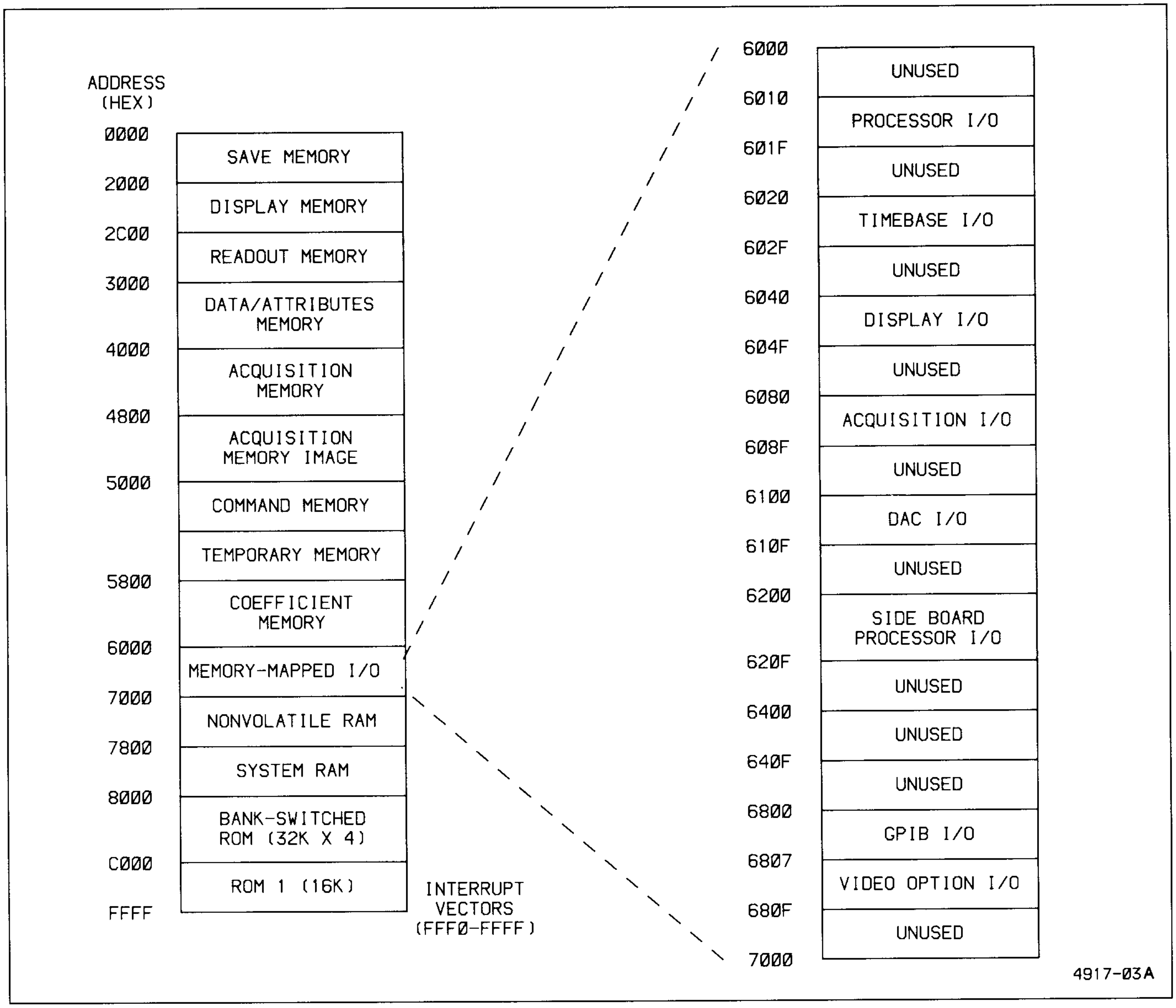


Figure 3-2. Simplified Memory Map of the 2430.

One-of-eight Decoder U884 uses the $\overline{HMMIO}$ line and address bits A3 and A4 as enabling signals. Address lines A0 and A1 and the $\overline{R}$/W line from the processor (via inverter U572C), select one of the eight outputs of U884 to go LO when the Decoder is enabled. Table 3-1 shows the registers accessed by this decoding.

Inverting buffer U830, enabled by $\overline{HMMIO}$ for I/O operations, applies the inverted middle bits of the address bus to various functional modules as selects. The firmware routines will allow only one of these select bits to be set LO at a time. In the selected circuit, further address decoding is enabled. Figure 3-2 illustrates the System μP address memory map and shows the blocks assigned for memory-mapped I/O. Each of the memory-mapped I/O blocks consists of 16 consecutive addresses from 6000h to 7000h with various functions assigned to specific addresses. These functions include clocks, chip enables, and circuit enables. Each is explained in the descriptions of the circuits they affect.

Address line AC and the output from AND-gate U862 are decoded by NAND-gate U870A to produce the host RAM enable ($\overline{HRAM}$) for addresses between 7000h and 7FFFh. This address block is split into two ranges by the further decoding done by gates U840A, U840B and inverter U254C. Address bit AB is decoded to enable Nonvolatile RAM U664 in the lower half of the range; the normal system RAM, U668, is enabled in the top part of the range.

AND-gate U580A (performing a negative-logic OR output function—a LO out is the enabling signal) detects when either the host RAM or system ROM is being addressed. A LO from gate U580A turns on the Memory Buffer U660 via OR-gate U332A (performing a negative-logic AND function—two LOs in give a LO enabling signal out). This connects the selected memory device to the system data bus.

System RAM

The System RAM provides temporary storage of data used in execution of the various control functions of the System μP. In addition, long-term power-off storage of system-calibration constants and front-panel settings is provided, allowing the instrument to power on in the same state it was in when it was turned off.

The System RAM consists of two memory devices, one being a low-power, Nonvolatile RAM that uses a battery-supply circuit to maintain the calibration constants and setup information during periods when normal instrument power is off. Both RAM devices are addressed in parallel, with the chip-select logic determining which one is enabled (see "System Address Decode" description). The addressed memory location will be read from or written to under control of the $\overline{WR}$ (write) and $\overline{RD}$ (read) control lines from μP U640.

The chip-select circuit for Nonvolatile RAM U664 consists of Q842, Q960, CR944, and associated components. With instrument power off, no bias current for Q960 will be

Table 3-1

Host Memory-Mapped I/O

W/$\overline{R}$	A1	A0	Output Signal
LO	LO	LO	INTREG (read Interrupt Register)
LO	LO	HI	PMISCIN (Processor miscellaneous inputs)
LO	HI	LO	CLRFIRQ (clears FIRQ flip-flop)[a]
LO	HI	HI	NC
HI	LO	LO	PCREG (write Processsor Control Register)
HI	LO	HI	PMISCOUT (write Misc Register)
HI	HI	LO	TVREG (write Video Option Register)
HI	HI	HI	WDREG (write Word Probe and GPIB LED Register)

[a]To clear the Fast-Interrupt Request, the μP does a read of the assigned address even through an actual register does not exist. The decoded output performs the reset function and no data is transferred.

available, and the transistor will be off. Power for maintaining the stored contents of the Nonvolatile RAM is applied to U664 from the Battery circuit; and with Q960 off, the chip enable input of U664 is also pulled HI via R764 to switch the I/O pins to their high-impedance state. This is the "low-power standby mode," and the contents of U664 are maintained as long as the V_{CC} supply and CE (chip enable) pins are held above +2 volts.

When instrument power is applied, a switching circuit in the Battery stage supplies power for the RAM, and the normal power supplies provide bias currents for the chip-select string between U840B and U664. As the power supplies are coming up, operations on the address bus are undefined, which could cause U840B to try to enable U664. To prevent this, the RESET signal from the Power-Up Reset stage is applied to the base circuit of Q960 through diode CR944. This LO keeps the transistor biased off until the power-up RESET signal returns HI; at which time the data on the address bus is stable.

With normal power on, when OR-gate U840B decodes an enable to access RAM U664, the output of the gate will go LO to turn off Q842. Current from R956 then supplies base current for Q960, turning that transistor on and pulling the chip-enable pin of U664 LO to enable the RAM. The Nonvolatile RAM enable is removed when the output of U840B goes HI, turning Q842 back on. Current from R956 is shunted to ground through Q842 and no base current for Q960 is provided. With Q960 off, the chip-enable input of U664 is pulled HI by R764 to disable the RAM.

Memory Buffer

Memory Buffer U660 transfers data between the System μP and the System ROM or System RAM stages. The buffer is enabled when either the System ROM or System RAM are addressed (see System Address Decode description). The direction of data transfer through the buffer is controlled by the WR (write) line from the System μP, depending on whether data is being written to RAM or read from either memory. When devices other than System ROM or System RAM are addressed, the buffer outputs are switched to a high-impedance state to isolate the memory devices from the data bus.

Miscellaneous Registers

The Miscellaneous Registers allow the System μP to initiate and control various processes by writing control words to two address-decoded locations. The Miscellaneous Registers also contain an address-decoded buffer used to read certain bits of instrument status.

The RESET line holds all of the outputs of Processor Control Register U860 LO until the Power-Up Reset goes HI, ensuring that the functions controlled by the PC register outputs start in known states. To load U860 the System μP writes data to location 6014h, generating an address-decoded PCREG clock. This rising edge of the PCREG clock when the clock returns HI causes the data on the data bus to be written into the register. Table 3-2 illustrates the select functions of the PC Register output bits.

Operation of U760, the Processor Miscellaneous Register (PMREG), is similar to U860 just described. Data is written into the register with the PMISCOUT (processor miscellaneous outputs) clock when address 6015h is decoded by U884. Table 3-3 explains register functions.

The Processor Miscellaneous buffer (PMBUF), U854, at address 6011h, allows the System μP to monitor the activities of various other circuits. By reading the data byte from location 6011h, the System μP can check for the presence of a Word-Trigger probe and for Waveform μP and Front Panel μP interrupts. For diagnostic routines and self-check, correct operation of registers U760, U860, and U754 is verified by writing known values to the diagnostic bits (DIAG0, DIAG1, and DIAG2) then reading them back.

Table 3-2

Processor Control Register Functions

Bit	Output Name	Output Function
0 1	PAGE-BIT0 PAGE-BIT1	ROM enable selection signals for Bank-Switched System ROM
2	PAGE-BIT2	Selects a page in Bank-Switched System ROM
3	WPRESET	Resets Waveform μP
4	WPKERNEL	Places the Waveform μP in "Kernel" mode for diagnostics
5	BUSREQ	System μP requests to take control of the Waveform μP busses
6	BUSTAKE	System μP takes control of the Waveform μP address and data busses
7	DIAGO	Diagnostic bit 0—verifies that data can be written to the PC register

Table 3-3

Processor Miscellaneous Register (PMREG) Output Functions

Bit	Output Name	Output Function
0	MWPDN	Masks off (disables) Waveform Processor Done interrupt
1	MSYNTRIG	Masks off Synchronous Trigger interrupt
2	MFPINT	Masks off Front-Panel interrupt
3	PENLIFT	Lifts pen of the X-Y Plotter
4	$\overline{\text{XYSAMP}}$	Indicates present data is for the X-Y Plotter (enables it)
5	$\overline{\text{XYHOME}}$	Forces the X-Y Plotter pen to the "HOME" position
7	DIAG1	Diagnostic bit 1—verifies data can be written to the PMISCOUT register

If both HIs and LOs can be written to and read from these diagnostic locations, fairly high confidence may be placed in the addressing and selection of the registers and their data paths.

Battery

The Battery circuit supplies standby power to the Nonvolatile RAM that allows instrument calibration constants and front-panel settings to remain stored for long periods of time (greater than three years) when instrument power is turned off. A switching circuit turns off the battery (BT800) current source while normal instrument power is applied. A battery monitor circuit warns the Front Panel μP (and thereby the user) of a low-voltage condition (indicating that it is time to change the battery) or an over-voltage condition (indicating that reverse current is attempting to charge the lithium battery).

With normal instrument power applied, transistor Q806 will be turned on by the base-bias voltage-divider circuit formed by R812 and R815. Base current is then supplied through Q806 and R800 to turn on Q804. This is the normal operating mode, and operating current for Nonvolatile RAM U664 is supplied via Q804 from the +5 V_D supply. During normal operation, capacitor C904 is held charged through CR902 but isolated from the RAM power source by reverse-biased diode CR900.

With instrument power turned off, transistors Q806 and Q804 are both turned off. The positive charge potential stored by capacitor C904 forward biases CR900 and pulls the chip-enable pin of U664 HI through R764. This disables RAM U664 and switches its I/O ports to high-impedance states. Operation in this state is the "standby" mode in which data in U664 is maintained using minimal supply current.

The eventual charge loss from capacitor C904 causes its output voltage to drop below that of Backup Battery BT800 (a lithium battery), and diode CR900 again becomes reverse biased. The standby current for U664 is then supplied from the battery via CR802 (and R900 in the return path). Diode CR802 acts as the current switch and prevents reverse current through the lithium battery during normal power-on operation. Resistor R900 provides reverse-current limiting in the event that CR802 becomes shorted.

BATTERY WARNING CIRCUIT. Operational amplifier U940A is a very high impedance buffer to limit current drain of the battery. Its buffered output voltage is applied to the Front Panel μP (diagram 3) to monitor for both low-voltage and over-voltage conditions of the lithium backup battery. A battery-error condition found at power-on or with the Extended Diagnostics will cause the BATT-STATUS test to fail. That test may then be selected to run at the next lower level in the test hierarchy to determine if the battery is undervoltage or overvoltage. The warning circuit is operational only when normal instrument power is applied. Resistor R802 provides additional circuit impedance that prevents any appreciable discharging of the battery by the voltage-sensing circuit.

WAVEFORM PROCESSOR SYSTEM

The Waveform Processor System (diagram 2) performs the high-speed data-handling operations needed to produce and update displays of acquired data points on the crt including averaging, enveloping, adding, multiplying, and interpolation of the waveform data. It accepts task information from the System μP and then carries out the assigned tasks without further need of the System μP. When that task list has been completed, it sends an interrupt to the System μP to inform it that another list of tasks can be accepted.

The Waveform μP memory space is accessible by the System μP, allowing the System μP to send commands to the Waveform μP and to read any desired result or data location especially for the GPIB I/O functions.

Waveform μP

Waveform μP U470 is a specially designed, high-speed microprocessor with a 16-bit multiplexed data and address bus and separate 12-bit instruction-address and 16-bit instruction-data busses. The Waveform μP is clocked at 2.5 MHz and executes one instruction each clock cycle. Internally the Waveform μP uses a 32-bit wide instruction word. Therefore, to enable it to obtain a complete instruction for execution with each μP cycle, instructions are "double-prefetched." Two 16-bit halves of the instruction are fetched from the instruction bus with each cycle at a 5 MHz rate, so that the instruction words are 32 bits wide.

Initially, with power-on, $\overline{\text{WPRESET}}$ (Waveform μP reset) from Processor Controlled Register U860 (diagram 1) will be LO, holding the processor reset via U270C. This reset remains in effect until the System μP writes a HI bit to the $\overline{\text{WPRESET}}$ output of U860 to remove the reset and enable the Waveform μP. The System μP also holds the Waveform μP reset while it is updating the command list in RAM of the next task that the Waveform μP is to perform. This reset occurs at the completion of each set of tasks given to the Waveform μP and is released when the new task list is in place in the Waveform μP Command RAM, U440.

Upon release of $\overline{\text{WPRESET}}$, the Waveform μP fetches the first two 16-bit words from its instruction ROMs, U480 and U490, at a 5 MHz rate and forms them into a 32-bit instruction word. Waveform μP U470 then executes the first instruction and at the same time it "prefetches" the next 32-bit word from the instruction ROM (the next instruction). The Waveform μP continues fetching instructions to carry out its internal initialization routine until that is completed, and it then looks in Command RAM at a vectored location to find the first task in the task list.

The first instruction in the task list tells the Waveform μP what is to be done. The μP then switches to the routine in ROM to get the instructions that do that job. Part of that routine might be to get the arguments for the task. When the arguments are in place, the Waveform μP then finishes the task routine. When done with the first task, the Waveform μP looks at the task list for the next task. It keeps doing the commands and arguments for each task until the entire task list is done. The last task of every task list is the WPDN task (Waveform Processor Done). Upon receiving that task, the Waveform μP sets the WPDN bit to the System μP Interrupt circuit HI, informing the System μP that it is finished. It then enters a "loop forever" state to wait for its next set of instructions. When the System μP checks the interrupt register and finds WPDN HI, it resets the Waveform μP and writes a new list of tasks to the Waveform μP Command RAM.

WAVEFORM μP OPERATION. When the Waveform μP gains control of the waveform bus, it sequentially moves the 1024 data points for each channel (512 min/max pairs in envelope) from the Acquisition Memory (diagram 8) to the Save Memory (U350). When the Waveform μP does a display update, it selects the required data points needed for each waveform display requested (according to the mode selected) from Save Memory and moves them to the Display Memory (diagram 16). At the end of the display update, DISDN (display done) from the Display Control (diagram 17) goes HI to interrupt the Waveform μP (and the System μP if the Waveform μP is also done and permits the signal to be gated to the System μP via AND-gate U580B, diagram 1). This tells the Waveform μP that the current display cycle has completed and the next update to Display Memory may be started.

When in ENVELOPE acquisition mode with more than a one acquisition accumulation to be displayed, the data bytes stored in Save Memory are not automatically overwritten with each acquisition. As the data bytes are being transferred from Acquisition Memory to Save Memory, they are compared by the Waveform μP. If the new data byte does not exceed the current maximum or minimum value in Save Memory location that it is being compared with, that Save Memory location is not overwritten (until the envelope acquisition is reset to start a new accumulation).

In AVG acquisition mode, data from the Acquisition Memory is averaged with the waveform data in the Save Memory, and the Save Memory is then rewritten with the averaged waveform data. Waveform adds, multiplies, expansions, and interpolations are performed by the Waveform μP on the Save Memory data prior to transfer to the Display Memory for display.

WAVEFORM μP ADDRESS ENABLING. The 2.5 MHz System Clock signal CLK1 from the Clock Divider U710 (diagram 7) is inverted by U866E and ORed with the skewed 2.5 MHz CLK3 signal by OR-gate U264B. The timing of this ORed signal is such that the output of U264B goes HI when the address on the input pins of Waveform Address Registers U562 and U364 is guaranteed to be valid. Inverter U270B inverts the output from the OR-gate (WVMA—waveform valid-memory address), and when that output again goes LO, the rising edge of the inverted WVMA signal on the clock input of the Waveform Address Registers latches the 16-bit address from the Waveform μP into the registers.

ADDRESS LATCH. Address Latches U364 and U562 hold the 16-bit address output by the Waveform μP. The latched address then remains on the address bus for the rest of the Waveform μP cycle to access that memory location for reads or writes.

Test point TP562 on address line WAA provides a trigger source for an external test oscilloscope when examining address waveforms in the Waveform μP "KERNEL" mode. As the KERNEL mode exercises address lines WA0-WAA, WAA is used as the trigger point.

WAVEFORM μP READ/WRITE ENABLING. Once latched, the address is removed from the bus and, depending on whether μP U470 is supposed to be reading or writing, data will be read into the processor from data bus buffers U360 and U560 or written to the WD (waveform data) bus via U360, a bidirectional data bus buffer. To read data into the processor, the HI R/$\overline{\text{W}}$ (read-write) signal is applied to NAND-gate U870C where it is NANDed with $\overline{\text{CLK1}}$. During the half period that $\overline{\text{CLK1}}$ is HI (CLK1 is LO), the gated output from U870C is the $\overline{\text{WRD}}$ (waveform processor read) in its LO (asserted) state. The LO is applied to the direction-enabling input of bidirectional buffer U360 via U542B. This LO enables U360 for a read from the WD (waveform data) bus, and the addressed 8-bit word on the WD bus is applied to the center eight lines of the processor 16-bit address/data bus.

The four least significant bits (LSB) and the four most significant bits (MSB) of the data applied to the WD bus come from buffer U560, which is enabled via U250B and U250A for processor reads. The four LSBs are always LO (guard bits), while the four MSBs will be set to the same level as the WD7 bit (sign-extended) of the center eight bits. This placement of the 8-bit data in the center of the 16-bit bus provides a reasonable tradeoff between dynamic range (12 bits) and guard bits (4 bits).

To write data out of the Waveform μP to the WD bus, the $\overline{\text{WRD}}$ level applied to the direction-enabling pin of U360 will be HI. The center eight bits of the Waveform μP data bus will then be buffered onto the WD (waveform data) bus by U360 and written to the currently addressed location. During writes to the WD bus, the HI level of $\overline{\text{WRD}}$ disables buffer U560, via U250B and U250A, to isolate it from the Waveform μP address/data bus.

SYSTEM μP ACCESS. When the System μP needs to do an access in the Waveform μP address space, it checks its software copy of PCREG to see if the Waveform μP is reset. If it is not reset, the System μP asserts BUSREQ (bus request) to the Waveform μP and waits until the Waveform μP outputs a BUSACK (bus acknowledge) to OR-gate U332D. The output of U332D is the BUSGRANT signal that, when HI, disables the Waveform μP data buffers, address registers, and memory control lines.

When Waveform μP U470 is being held reset (inactive) and cannot possibly respond to a BUSREQ, the System μP instead asserts BUSTAKE to OR-gate U332D when it needs to take control of the Waveform μP address space. The System μP can also assert BUSTAKE during diagnostics in the event of a Waveform μP failure to release the bus after a BUSREQ is given.

From inverter U254B, $\overline{\text{BUSGRANT}}$ turns on Bus Connect Address Buffers U262, U260, and U564 to connect the System μP address bus and control signal lines to their counterparts from the Waveform μP. Bus Connect Data Buffer U552, a bidirectional device, is then enabled and directed by control signals from the System μP for data transfers to and from the Waveform μP data bus.

NOR-gate U850, performing a negative-logic NAND function, is used to check for proper addressing to connect the System μP and Waveform μP data busses together. When all of the addressing conditions are met, Bus Connect Data Buffer U552 is enabled by the output of U850 via inverter U254D, and the two busses are connected together. The direction of the transfer through the buffer is controlled by the $\overline{\text{WR}}$ (write) line from the System μP, depending on whether a write access ($\overline{\text{WR}}$ is LO) or a read access ($\overline{\text{WR}}$ is HI) is being done.

The conditions that must be present for NOR-gate U850 to produce an enable to the Bus Connect Data Buffer are:

1. $\overline{\text{BUSGRANT}}$ LO—Waveform μP has relinquished the busses.

2. $\overline{\text{MAIN}}$ HI—This is not a "system RAM" access.

3. Address bit AF is LO—This is not a "system ROM" access; and either:

   a. HMMIO is LO—The address is not a System μP memory-mapped I/O location, or

   b. It is a memory-mapped I/O location and address bits A3 and A4 are HI (the address is within the top eight I/O addresses of the System μP).

Addresses residing in the System μP memory space should not access the Waveform μP memory space, and are thus excluded from access by U850 and the associated input logic gates. Addresses not excluded will cause a System μP access into the Waveform μP memory space.

Waveform μP ROM

The Waveform μP ROM consists of two, 4K-x-8-bit ROM devices connected in parallel to form a 4K-x-16-bit storage memory for Waveform μP waveform data handling commands. The Waveform μP "double-fetches" data from this ROM space by reading in two 16-bit bytes of command data during each Waveform μP clock cycle. This method of reading the commands makes the Waveform μP command memory space look like a 2K-x-32-bit ROM. The 32-bit instruction word formed by the two fetches adequately defines any Waveform μP operation and allows the Waveform μP to execute one instruction for each 2.5 MHz clock cycle.

Waveform μP ROMs, U480 and U490, are enabled by three chip selects each. During normal operation, WFM KERNEL jumper (P128) is installed, and the CS1 chip selects of both ROMs are enabled. Chip select CS2 of both ROMs are addressed by the Waveform μP IAA bit to access the memory locations, and chip select CS3 of both ROMs is permanently enabled by +5 V via W380. When the ROMs are enabled by the IAA address line from the Waveform μP, data from the addressed location is output to the 16-bit instruction data bus of the Waveform μP. In this implementation, jumper W378 is left out, but it can be added for future expansion of the addressing by using the IAB bit to control the CS3 line. In that case, jumper W380 would be removed from the circuit to disconnect the +5 V supply from the CS3 input pins.

The addresses of instructions to be read are determined by the 12 instruction-address bits output from the Waveform μP and by the state of the 5 MHz clock. The 12 address bits from U470 are the most significant address bits for any given instruction. The 5 MHz clock applied to ROM address inputs A0 through delay line DL580 and associated components provides the least significant address bit with sufficient delay to provide the needed data-hold time. The state of the 5 MHz clock will be LO to access the first 16 bits of an instruction word. The state of the A0 address line then goes HI, and the second half of the 32-bit instruction is obtained from the next higher memory location. This manner of address selection is the "double-fetch" of instruction data mentioned previously in the Waveform μP description.

Manually removing jumper P128 disables the Waveform ROMs and places their outputs into the high-impedance state. The pull-up and pull-down resistors within resistor packs R474 and R590 place a "NOP" (no-operation) instruction byte on the instruction bus. A NOP command causes the Waveform μP to increment through the first 12 bits of its address range on the 16-bit DAD bus and through all the addresses of its IA bus. This "KERNEL" mode allows the Waveform μP address bus and address decoding to be exercised for troubleshooting and diagnostic purposes.

Address Decode

The Address Decode circuit monitors the Waveform μP address bus to develop the appropriate enabling signals to the memory or I/O device that is to be accessed.

Block decoding is done by one-of-eight decoder U570, which uses address lines WAC-WAF to separate the addresses below 32K into eight, 4K blocks. Decoder U570 is enabled when a valid address (WVMA HI) below 32K (address bit WAF LO) is placed on the memory address bus by either the Waveform μP or the System μP. The next three lower address lines (WAE, WAD, and WAC) determine which one of the eight outputs of the Decoder will be selected. Table 3-4 illustrates this address decoding.

A LO output selection to either Y0 or Y1 of Decoder U570 will cause AND-gate U580C (functioning as a negative-logic OR gate) to output a LO $\overline{SAVE}$ enable to "Save" RAM U350 via Q244 and Q332. The Save RAM resides in the first 8K of address space, 0000h to 1FFFh. This storage space is where waveform data is placed for saving while the oscilloscope is turned off. The chip-select circuit between the $\overline{SAVE}$ output of U580C and the low-power RAM chip U350 is identical to that for the System μP nonvolatile RAM (U664, diagram 1). The circuit provides for chip selection during normal operation and high-impedance isolation of the Save RAM chip-select input when power is off. The chip-select circuit is explained more fully in the "Save Memory Keep-Alive" description. Writing to or reading from any of the Waveform μP RAM space is done via bidirectional bus buffer U352. When Save RAM U350 is selected by the $\overline{SAVE}$ line going LO, U352 is also enabled via AND-gate U580D. The direction of the data transfer is determined by the state of the $\overline{WWR}$ (waveform write) control line.

The next three outputs from U570, $\overline{DISP}$, $\overline{DATT}$, and $\overline{ACQ}$, are used to select the Display and Display Attribute Memories (diagram 16) and the Acquisition Memory (diagram 8) respectively.

The 4K block of addresses from 5000h to 5FFFh, when selected, is further decoded into two, 2K blocks by U250C, U254E, and U250D. In this block of memory, address line WAB is used to select either Command Memory U440 via OR-gate U250C or Coefficient Memory U432 via OR-gate U250D and inverter U254E. Bidirectional bus buffer U352 (RAM Buffer) is enabled via AND-gate U580D for data transfers to or from either RAM for this entire address block.

Table 3-4

Waveform μP Address Decoding

ADDRESS BITS			OUTPUT SIGNAL (Active LO)
WAE	WAD	WAC	
LO LO	LO LO	LO HI	(Y0 or Y1) SAVE from NAND-gate U580C to enable the SAVE memory.
LO	HI	LO	(Y2) DISP—Selects display memory.
LO	HI	HI	(Y3) DATT—Selects attribute memory.
HI	LO	LO	(Y4) ACQ—Selects acquisition memory.
HI	LO	HI	(Y5) WPCMDN/COEFF—Selects either the command or the coefficient memory.
HI	HI	LO	(Y6) WMMIO—Enables Waveform μP memory-mapped I/O Decoder U540.
HI	HI	HI	(Y7) Unused.

The waveform memory-mapped I/O locations fall into the next 4K block decoded by U570 (WMMIO). Addresses falling within this block produce a LO on the WMMIO signal line and enable U540. Decoder U540 operates similarly to U570 and uses address lines WA0-WA4 to produce its various I/O enabling outputs. Address bits WA3 and WA4 are used as chip selects and cause the output of U540 to fall into the eight locations immediately above those of Decoder U884 (diagram 1) for System μP memory-mapped I/O.

The outputs of U540 allow the accessing processor to read the display status (SSREG), to read the two-byte address of the last-acquired point (RDMAR0 and RDMAR1), or to latch the present interrupt status (COMREG). (See the "Display Status Register" and "Interrupt Latch" descriptions for further explanation.)

Waveform μP RAM

The Waveform μP RAM resides in the Waveform μP address space and is used for storage and manipulation of waveform-display data. The RAM consists of three memories; the 8K-x-8-bit "Save Memory" RAM, the 2K-x-8-bit "Command-temp" RAM, and the 2K-x-8-bit "Coefficient" RAM.

The 8K-x-8-bit Save Memory, U350, is where the Waveform μP places acquired waveform data that should be retained with power off. Waveforms stored is the Save RAM are retained for at least five days at room temperature with the power off.

The "command-temp" RAM, U440, provides temporary scratch-pad storage of display calculations in process and storage of commands to the Waveform μP from the System μP.

The "coefficient" RAM, U432, provides further scratch-pad storage.

Reading from and writing to the Waveform μP RAM selected by the Address Decode circuit are controlled by the WRD (waveform read) and WWR (waveform write) signals respectively.

RAM Buffer

The RAM Buffer U352 allows data transfers to and from the Waveform μP RAM to take place. The buffer is enabled by U580D when any of the Waveform μP RAM locations are addressed. Buffer direction is determined by the WWR level.

Save Memory Keep-Alive Supply

The Save Memory Keep-Alive circuit maintains the contents of the waveform "save" memory, RAM U350, during periods that the oscilloscope power is turned off. A portion of the circuit controls the chip-select input of the Save RAM during normal operation. The keep-alive current to RAM U350 is supplied by the charge stored in capacitor C896. The large capacity value of C896 (one farad) provides sufficient energy to maintain the saved data in RAM

U350 for three to five days at room temperature with a 10 μA standby current demand. The save time decreases with increasing temperature as the standby current demand increases and the charge storage capability of the capacitor decreases.

During normal operation, the $\overline{PWR}$ (power) signal from Q806 in the Backup Battery circuit (diagram 1) will be LO and the V_{CC} source for Save RAM is via transistor Q782. With the power on, capacitor C896 is charged up through CR792 to store energy for the power-off keep-alive function. Chip selection for the Save RAM is done through transistors Q244, Q332, and their associated components. Initially, when the oscilloscope is turned on, the $\overline{RESET}$ signal applied to the base of Q332 via CR244 keeps the Save RAM deselected. When the power supplies are up to normal operating levels, $\overline{RESET}$ goes HI, and chip selection is controlled by the output signal from AND-gate U580C.

When the oscilloscope is turned off, the secondary supply voltages drop off slowly enough to allow an orderly shutdown of the digital circuitry. The $\overline{RESET}$ signal from the Power-Up circuit (diagram 1) goes LO when the output of +5 V_D supply drops to about +4.3 volts. The LO $\overline{RESET}$ signal switches off Q332 to produce a high-impedance path from its collector to ground, and CR784 becomes forward biased by the voltage level of the charge on C896. The $\overline{PWR}$ bias supply to Q782 is removed when the +5 V_D supply drops below about +3 V (Q806 in the Backup Battery circuit becomes biased off at that voltage level), and that transistor is also turned off. The positive voltage level on the RAM chip-select input keeps the outputs in their the high-impedance state, and the current needed to maintain RAM contents is then supplied from the charge on C896 through forward-biased diode CR784.

Display Status Register

Display Status Register U542A allows the controlling processor (System μP or Waveform μP) to read the status of the Display System operations. The address-decoded $\overline{SSREG}$ (sub-system status register) line from Decoder U540 enables buffer U542A to place the DISDN (display done) and ACQDN (acquisition done) signals on the WD bus where they may be read. These status bits are used by the reading μP to determine when to execute the next phase of a display or acquisition sequence.

Interrupt Latch

The Interrupt Latch (U550) allows the Waveform μP operations to interrupt the System μP for servicing and, when servicing is completed, allows the System μP to reset the interrupt.

To write data into the latch, the controlling μP addresses location 6019h, causing the $\overline{COMREG}$ line from U540 to enable U550. Data from the WD bus is written into the latch on the rising edge of the $\overline{WWR}$ pulse. The Q output from pin 2 (MDISDN) of the latch is applied to AND-gate U580B (diagram 1) where it either masks the DISDN (display done) interrupt from the System μP when it occurs or lets the interrupt pass. Masking the DISDN interrupt from the System μP permits the Waveform μP to have first access to the Display System for display updates before the System μP sees that the Display System is finished with its last task. The next bit is unused. The Q output bit on pin 10 is the WPDN (waveform processor done) interrupt and provides the Waveform μP with a way of telling the System μP that it is done with its assigned task and is ready to accept another. The output bit on pin 10 is applied to Display Status Register U542A and is used for write-readback verification of U550 and U542A during the self-check and other diagnostic routines.

FRONT PANEL PROCESSOR

The Front Panel Processor (diagram 3) monitors the settings of the pots and switches of the Front Panel (diagram 4) and the Auxiliary Front Panel (diagram 6). The Front Panel μP allows quick system response to changes in front-panel settings without excessive use of time by the System μP. The Front Panel Processor system consists of the microprocessor integrated circuit with a built-in RAM, ROM, and A/D converter (for digitizing the potentiometer wiper voltages); the handshake logic between the System μP and the Front Panel μP (to synchronize data transfer between processors); and the data bus interface to provide the actual data transfers between busses.

Front Panel μP

Front Panel μP U700 does the reading of the front-panel pots and switches. It continuously scans the front-panel control settings and compares them against the values stored in its internal RAM. When a change is detected, the Front Panel μP issues an interrupt to the System μP. The System μP then handles the interrupt and reads the changed data from the Front Panel μP to update its control-setting values. The Front Panel μP also updates the current value list stored in its RAM for further use.

Front Panel μP U700 is externally clocked by the 4 MHz system clock applied to the external clock input (EXTAL). Initially, the LO state of $\overline{FPRESET}$ on the INT_2 input (pin 18) will clear all the internal registers of the Front Panel μP. When $\overline{FPRESET}$ goes HI, the μP executes the power-up self-test instructions stored in ROM space within the μP integrated circuit. When the self test has completed, the Front Panel μP sends the diagnostic result byte to the System μP and branches to its main program. The main program routine sets up the data direction for the various port lines, sets the AN0-AN3 (analog inputs 0-3) to their analog input mode, and receives the eight front-panel configuration bytes from the System μP that define the manner in which the various front-panel switches and pots operate. It then begins scanning the front-panel pots and switches for their initial settings. After the initial values are determined and stored, the Front Panel μP sends those coded values back to the System μP in an 11-byte message (10 data bytes plus an end-of-message byte) to update the front-panel information held by the System μP. It then begins scanning the front-panel controls for changes from the currently stored front-panel values.

To read front-panel pot settings, the internal A/D converter of the Front Panel μP performs an 8-bit, successive-approximation conversion of the analog levels applied to the AN0 and AN2 inputs by a selected potentiometer. These analog input signals come from 8-input analog multiplexers U902 on the Front Panel (diagram 4) and U600 on the Auxiliary Front Panel (diagram 6). A specific pot to be read is selected by the multiplexer under control of the MUXSEL0, MUXSEL1, MUXSEL2, and MUXINH (multiplexer inhibit) output lines from the Front Panel μP. These select signals, in combination with the selected A/D (AN0 or AN2) input, define the pot being read. The voltages monitored on the AN1 and AN3 analog inputs are also digitized by the internal A/D converter to detect Main board temperature (MBTEMP) changes (not used at this time) and if lithium backup battery BT800 (diagram 1) is either low (needing replacement) or being charged (not allowed).

To read the front-panel switches, the Front Panel μP first sets one of the front-panel switch-matrix rows LO, using the MUXSEL0-MUXSEL2 outputs. It then sets its S/$\overline{\text{L}}$ (shift/load) output on pin 29 LO. The LO does a parallel load of the switch-closure data into shift registers U904 (diagram 4) and U700 (diagram 6). The shift/load line is then set HI (shift mode), and eight shift clocks (SHCLK) are generated to move the switch-closure data serially onto the SW OUT (front-panel switch data out) or the SW OUT A (auxiliary front-panel switch data out) lines, where it is read by the Front Panel μP. This cycle is then repeated for the seven remaining rows of the matrix to read all the switches.

When the Front Panel μP detects a change in either a switch or a pot setting from its currently stored values, it places a code identifying which control setting changed on its PA0-PA7 outputs, and it then sets the WRTOHOST (write to host) signal HI to clock Handshake Logic flip-flop U861B. The resulting HI on the Q output of the flip-flop is the front-panel interrupt (FPINT) to the System μP, telling it that the front-panel settings have been changed.

The System μP handles the interrupt by reading the byte from the Front Panel μP; and then, via the Handshake Logic, it resets flip-flop U861B to remove the interrupt and set HOSTDNRD (host done reading) HI. This signals the Front Panel μP that the System μP has read the code identifying the changed control. The Front Panel μP then places the new control-setting value on its output bus and reasserts the front-panel interrupt using the WRTOHOST line to again clock flip-flop U861B.

The System μP then reads the changed-data bytes for the identified control(s) (either three bytes or five bytes depending on whether one or two control changes are being sent) and reasserts HOSTDNRD. Changes of up to two controls are remembered by Front Panel μP U700 so that if the System μP is busy, the control changes are not lost while the Front Panel μP is waiting to make the transfers. If more than two controls are changed before the System μP has time to read the changes, the oldest change is written over and lost.

The $\overline{\text{WRTOFP}}$ (write to front-panel processor) input to U700 at pin 3 is set LO (via the Handshake Logic) when the System μP wants to input data to the Front Panel μP. The Front Panel μP then reads one byte of data from the System μP in a manner similar to that just described for transfers from the Front Panel μP to the System μP. This mode allows the System μP to change the current control configuration list stored in the limited RAM space of the Front Panel μP. This list defines how the operation of pots and switches is to be interpreted (for example, momentary contact or toggle switches).

Jumper J155, connected to the PC_7 and PD_7 inputs, is used to enable diagnostic test routines that verify functionality of U700. The test routines may also be used to troubleshoot the Front Panel Processor system. These tests are explained in the Diagnostics portion of the "Maintenance" section of this manual.

Handshake Logic

The Handshake Logic circuit, formed by NOR-gates U862A, B, C, and D and flip-flops U861A and B, controls and synchronizes data transfers between the System μP and the Front Panel μP.

Data transfers between the two processors are initiated by interrupts that signal the destination processor that service is requested. When the Front Panel μP has changed-value data to give to the System μP, it will place the data bytes to be given to the System μP on its PA_0-PA_7 (port A—bits 0 through 7) outputs. It then asserts WRTOHOST (write to host) HI, clocking the FPINT (front-panel interrupt) at the Q output of U861B HI.

Depending on what the System μP is doing, it may either service the interrupt request immediately, or it may wait for time to be available. When it responds to the interrupt, it does a read of the Front Panel "register" at address 6209h. The decoded $\overline{\text{FPREG}}$ signal from Trigger Holdoff Decoder U781 (diagram 12) allows OR-gates U862B and U862C to pass the $\overline{\text{WR}}$ or $\overline{\text{RD}}$ signals. For a read, both input pins to U862B are LO, causing the output of U862A to go LO. This enables buffer U751, placing the data from the Front Panel μP on the System μP data bus (FP0-FP7) and, at the same time, resets flip-flop U861B. Resetting U861B removes the front-panel interrupt and sets HOSTDNRD (host done reading) to U700 HI.

When the System μP needs to write to the Front Panel μP, it writes data to address 6209h. This latches data from the System μP data bus into register U742. The enable to U742 is via U862C. The latch enable also resets the Q output of flip-flop U861A LO via U862D to produce the $\overline{\text{WRTOFP}}$ (write to front-panel) interrupt to U700. Latching data into U742 immediately frees the System μP to resume other tasks, since it doesn't have to wait for the Front Panel μP to service the interrupt.

When U700 services the interrupt by the System μP, it sets $\overline{\text{FPRD}}$ (front-panel reading) LO and enables the latched data in register U742 onto the Front Panel data bus. It then reads the data into its internal registers and asserts FPDNRD (front-panel done reading). FPDNRD going HI clocks the $\overline{\text{FPDNRD}}$ status bit from flip-flop U861A pin 6 HI to signal the System μP that it is done reading the byte and removes the $\overline{\text{WRTOFP}}$ interrupt present on U861A pin 5. Each data byte transfer from the System μP to the Front Panel μP and vice versa is done using the two handshake routines just described.

Trigger Status Indicators

The Front Panel Trigger Status Indicators provide visual information regarding trigger slope and trigger status to the user. Data written to LED Register U741 from the System μP turns on the LED that reflects the current trigger status. A LO output from U741 turns on the associated LED. The LED Register is enabled by a System μP write to address 6208h. Trigger Holdoff Decoder U781 (diagram 12) produces the decoded $\overline{\text{LEDREG}}$ signal that enables data at the input pins to be latched when the $\overline{\text{WR}}$ clock goes HI.

FRONT PANEL CONTROLS

The Front Panel is the operator's interface for controlling the user-selectable oscilloscope functions.

All of the Front Panel controls (diagram 4) are "soft" controls in that they are not connected directly into the signal path. Therefore, associated circuits are not influenced by the physical parameters (such as capacitance, resistance, and inductance) of the controls. In addition, converting the analog output levels of the potentiometers to digital equivalent values allows the System μP and the Front Panel μP to handle the data in ways that enhance control operation.

The variables defining the current settings of the control pots and the front-panel switches are stored and continually updated in Nonvolatile RAM U664 (diagram 1) by the System μP. The data remains stored when the oscilloscope is turned off so that when the scope is turned on again the System μP returns to the same front-panel setup that was present when the scope was turned off.

Front-Panel Switch Scanner

The Front Panel switches are arranged in an electrical array of eight rows and six columns. Switches are placed at row-column intersections, and when a switch is closed, one of the row lines is connected to one of the column lines through an isolation diode. Checking for switch conditions (open or closed) is done by setting a single row line LO and then sequentially checking the six columns to determine if a LO is present on any of the column lines. After each column line in a row is checked, the current row line is reset HI and the next row line is set LO to check the next six columns. A complete check of the front-panel switches consists of setting all eight row lines LO in order and performing a six-column scan for each column to check for a LO.

A row is selected for checking by the Front Panel μP (U700, diagram 3) when it switches the MUXSEL lines (0-2) applied to multiplexer U903 to set a row line LO. To check the columns, the processor pulses its S/$\overline{\text{L}}$ (shift/load) select line to shift register U904 first LO and then HI. This causes a parallel load of the six column-line bits (plus the seventh and eighth bits tied HI by R934) into the shift register. The processor then generates eight shift clocks (SHCLK) to U904, serially shifting the switch data out on the SWOUT (switch data out) line. The serial data bits are applied to the PB0 input (pin 25) of the Front Panel μP to be checked. Any LO bits in the column-line data tell the μP that a switch is closed. Since the Front Panel μP knows which row line it set LO, it can determine from the position of the LO bits in the serial data string which of the switches are closed.

In addition to the front-panel push-button and continuous-rotation switches connected in the switch array, there is a rate switch associated with the Horizontal Position, the CH 1 Vertical Position, the CH 2 Vertical Position, and the Cursor Position potentiometers. These switches are normally closed in the center positioning range of the associated pot. When the pot is rotated in either direction out of this range, the rate switch opens. The open switch signals the Front Panel μP that the associated control function has changed from normal (absolute) positioning to a faster, rate-change positioning mode. Rotating the pot still further into the rate region causes the associated on-screen display position to change at a still faster rate. When the pot position is returned to its center range (rate switch closed), further positioning of the associated display occurs from where the rate function positioning left off.

Pot Scanning

The Pot Scanning circuitry, working together with the A/D converter internal to Front Panel μP U700, produces digital values for the wiper voltages of the front-panel potentiometers and for the voltages monitored by the auxiliary front-panel circuitry. Analog multiplexer U902 selects which of the eight front-panel pots are read. (Trigger Level control R902 and Holdoff control R901 are continuous-rotation potentiometers made up of two separate resistive elements each.) Analog multiplexer U600 (diagram 6) selects the auxiliary front-panel value to be read.

Three MUXSEL control lines to multiplexers U902 and U600 select the pot or value to be read. The analog voltage level at the wiper of the pot selected by U902 is output at pin 3 (AOUT0) and is applied to the Front Panel μP at pin 21 (analog input AN0). Analog voltages selected by multiplexer U600 are applied to analog input AN2. The voltage levels at these inputs are digitized, and the amount and direction of changes from the previously stored values are calculated. Changed values are stored in the internal RAM of U700 for comparison during future scans, and the change data is then relayed to the System μP. That change data is used by the System μP to update its current control settings and pot values list and to update the front-panel variables in Nonvolatile RAM U664.

SYSTEM DAC AND ACQUISITION CONTROL REGISTERS

The System DAC and Acquisition Control Registers circuitry (diagram 5) is used to set various analog reference voltages throughout the instrument and controls such things as preamplifier gain, vertical position and centering, trigger levels, holdoff time, common-mode rejection, graticule illumination, and CCD offsets.

The System DAC portion of the circuitry consists of a data latch that stores the digital value to be converted, a D/A converter that does the actual conversion, a multiplexer system to route the resulting analog voltage to the proper control circuit, and a sample-and-hold system that stores the analog levels between updates. Much of the multiplexing and sample-and-hold circuitry is shown in diagram 6, System DAC (cont) and Auxiliary Front Panel.

The other portion of diagram 5 is the Acquisition Control Registers circuitry, used by the System μP to set up the acquisition and triggering modes. The System DAC portion is described first.

D/A Converter

The D/A Converter stage, U860, converts the digital value written into registers U850 and U851 by the System μP into two complementary output currents. (Complementary in this case means that the sum of the two currents equals a predefined value.) The digital data bits to be converted are serially clocked into the shift register from data bus line D7 (via U280). Sixteen data bits are sequentially placed on data bus line D7 and clocked into the shift register on the rising edges of 16 $\overline{\text{WR}}$ pulses (clock is via U280A and U280B). As the bits are being loaded into the registers, the DAC output current does not correspond to any useful value, but the multiplexers used to direct that output to the following stages are not enabled during loading. After all 16 bits have been clocked into the register, the inputs to DAC U860 will be at their proper levels and the DAC outputs will be valid levels. One of the multiplexers may then be enabled by the System μP using the DAC MUX enables via register U272.

Only the first 12 bits (DAC0 through DAC11) of the 16 bits loaded into the registers for are used for conversion data. The next three higher bits are used as 1-of-8 select bits to the four analog multiplexers that route the DAC output voltage to the proper Sample-and-Hold circuit. And finally, the MSB of shift register U851 is used in a write-readback operation that allows the operation of registers U850 and U851 to be checked by the System μP during self checks and diagnostics.

The magnitude (range) of the DAC output currents is set by the voltages applied to pins 14 and 15 of U860. Pin 15 V_{REF-} is tied to ground through R761. The reference voltage to pin 14 is applied via a voltage divider (R760 and R860) between the $+10\ V_{REF}$ supply and the output of the DAC Gain Sample-and-Hold, U660. The System μP enables self-calibration of the gain of U860 via this Sample-and-Hold circuit. Gain changes are explained in the discussion of the DAC Gain Self-Calibration circuit.

DAC I-TO-E CONVERTER. This circuit changes the differential output currents from DAC U860 into a single-ended output voltage that is routed to a selected Sample-and-Hold circuit via one of the analog multiplexers.

The output currents from DAC U860 develop a voltage drop across the resistive networks at the inputs to operational amplifier U661C. The equivalent input impedance at both inputs is approximately 200 ohms; so, when both currents are equal (middle range of the DAC), the output voltage of operational amplifier U661C will be close to zero volts. An offset current is added to the non-inverting input node via R666 to precisely set the midrange value to zero volts. The gain of U661C is set by the ratio of R663 to R664, and the (calibrated) output voltage ranges from −1.36 V to +1.36 V.

DAC OFFSET. The DAC Offset level is self-adjusting and is updated via DAC Offset Sample-and-Hold U650 each time the DAC System cycles through its DAC channels to update its control levels.

At the beginning of each DAC-update cycle, the System μP writes 0800h to DAC input shift registers U850 and U851; this corresponds to zero volts (center of the DAC range). The DAC output currents representing zero volts are converted by the DAC I-to-E Converter U661C to a voltage that is applied to U650 via multiplexer U651. Any deviation from the desired zero-volt level causes the output of U650 (configured as an inverting integrator) to shift slightly. This applies an offsetting voltage to DAC I-to-E Converter U661C via R666 and R665 to bring its output level back to precisely zero volts.

Capacitor C655 holds the offset level constant between update cycles (every 64 ms) to keep the proper offset for the entire DAC cycle. By updating the offset every 64 milliseconds, offset variations that would otherwise occur over time and temperature changes are eliminated.

DAC GAIN. The DAC Gain is set during each DAC-update cycle immediately after DAC Offset is set and keeps DAC gain constant with time and temperature changes.

To set the DAC Gain, the System μP loads 0F59h into DAC input registers U850 and U851 and routes the resulting output voltage to DAC Gain Sample-and-Hold U660 via multiplexer U651 pin 2. A digital input of 0F59h to the DAC is supposed to produce an output of +1.25 V from U661C. The resulting DAC output is compared to a +1.25 volt reference by operational amplifier U660. Any deviation from the correct +1.25 V level produces a gain-correction voltage applied to the DAC via R760. Capacitor C662 maintains the correction voltage between DAC update cycles.

Multiplexer Select

The Multiplexer Select circuit, composed of addressable latch U272 and the associated decoding gates, provides the enabling signal that selects one of the four 1-of-8 multiplexers to route the DAC output voltage to the Sample-and-Hold circuits. Data applied to the D input of U272 from data bus bit $\overline{D7}$ (via U280D) is latched to the addressed output pin as determined by the logic levels on the A, B, and C select lines (A0 through A2). The input data is written to the addressed output on the falling edge of the enable signal at pin 14 (via U280A and U280C). The logic state written to the output remains latched when the enable signal returns HI. The states of the unaddressed outputs remain unchanged. To enable the latch, NOR-gate U280A (functioning as a negative-logic NAND-gate) needs the $\overline{DACSEL}$ (DAC select) line LO to produce a HI output. That HI is inverted by U280C to enable the Multiplexer Select register to be written into. That same LO $\overline{DACSEL}$ is applied to NOR-gate U280D to enable it to pass the data on the D7 line to the D input of U272 and to the DAC input register, formed by U850 and U851.

Multiplexer U651, when enabled by Multiplexer Select Latch U272, routes the analog output voltage from DAC I-to-E Converter U661C to one of eight Sample-and-Hold circuits, depending on the output specified by the logic states on the its select inputs. Selection is determined by three bits clocked into DAC Register U851 as described in the preceding D/A Converter discussion. One of three other multiplexers, shown in diagram 6, may be enabled instead of U651 to pass the DAC output to one of the Sample-and-Hold circuits on their outputs (also shown in diagram 6).

Sample-and-Hold

The eight Sample-and-Hold circuits shown on diagram 5 (formed by U641A through U641D, U650, U660, U661A, U661B and their associated components) store and buffer the analog voltage levels directed to them by multiplexer U651. Each of the operational-amplifier circuits selectable by U651 (except the DAC Offset and DAC Gain operational amplifiers, U650 and U660 respectively) has a hold capacitor on one input that is charged up to the DAC output voltage level through the selected multiplexer channel. When the multiplexer channel is then deselected, the capacitor holds the voltage at a fixed level so that the associated Sample-and-Hold circuit provides a steady voltage level to the circuit it controls. Voltage gain of the Sample-and-Hold operational amplifiers range from more than 4.5 in the CH 1 and CH 2 Gain-Cal circuits down to 2 in the

Jit 1 Gain and Jit 2 Gain amplifiers and down to about 1 for the CH 1 and CH 2-BAL voltage followers. The Jitter Gain circuits (formed by U661A and U661B) produce a negative 5 V dc offset voltage at their output pins as their gain-setting resistors are referenced to the +5 V supply. The DAC Offset and DAC Gain Sample-and-Hold circuit operations are described in the previous D/A Converter discussion.

Acquisition Control Registers

Mode control of the analog acquisition system and trigger circuitry is controlled by the System μP via shift registers and a decoder. The System μP, through its address decoding circuitry, enables Decoder U271 to produce a shift register clock at one of its eight outputs. These clock signals are used to move serial data from the ACD (acquisition control data) line, U272 pin 5, into one of the various Acquisition Control Registers, of which three are shown in diagram 5. They are Peak Detector Control Register U530, Gate Array Control Register U270, and Trigger Source Control Register U140. Other registers clocked are the Channel 1 and Channel 2 Control Registers (U510 and U220 on diagram 9), the internal control registers of the CH 1 and CH 2 Preamplifiers (U420 and U320 on diagram 9), and the internal control registers in the A/B Trigger Generator (U150, diagram 11).

The ACD line is shared by all the Acquisition Control Registers; the selected clock determines which register will be loaded with the data being written by the System μP. Decoder U271 is enabled when the $\overline{\text{ACQSEL}}$ and $\overline{\text{WR}}$ lines are LO and address line A3 is HI. Address lines A0, A1, A2 determine which of the output lines produces the clock signal. A data bit present on the ACD line (previously written to latch U272 in a DAC write cycle) is loaded into the clocked register on the rising edge of the $\overline{\text{WR}}$ signal as U271 becomes unenabled and its selected LO output goes HI. Each bit to be loaded must be successively written to U272 then moved into a register by the output clock from U271.

SYSTEM DAC (cont) AND AUXILIARY FRONT PANEL

The DAC multiplexing and sample-and-hold circuits included in diagram 6 operate similarly to those described in the DAC System (diagram 5) discussion. The analog voltage output from the DAC I-to-E Converter is routed through one of the three additional multiplexers (shown in diagram 6) to several types of hold circuits.

DAC Multiplexers

DAC Multiplexers U821, U830, and U831 route the analog output voltage from DAC I-to-E Converter U661C (diagram 5) to the various Sample-and-Hold circuits. Operation of each multiplexer is identical to that of Multiplexer U651, previously described in the System DAC circuit discussion. Each multiplexer is individually enabled by a bit from Multiplexer Select Latch U272, and signal routing through the enabled device is controlled by the three select bits applied to it from the three most significant bit outputs of DAC Register U851.

Sample-and-Hold

A separate Sample-and-Hold circuit is associated with each of the multiplexer outputs. An analog voltage routed from the DAC I-to-E Converter through the selected multiplexer channel charges up the hold capacitor at the input of an operational amplifier in the selected Sample-and-Hold circuit. When that multiplexer channel is deselected, the voltage level is held on the capacitor because of the high-impedance discharge paths presented by the multiplexer output and the operational amplifier input. The individual operational amplifiers are configured as buffers with voltage gains varying from −0.47 to +10, depending on the requirements of the function that is being controlled. The CH 1 and CH 2 Position Sample-and-Hold circuits also provide a dc offset of their output levels to properly bias the inputs they drive.

Cal Signal Amplifier

The Cal Signal Amplifier (U610) operates in a manner similar to the Sample-and-Hold circuits just described. It is used to supply test signals to the CAL inputs of the CH 1 and CH 2 Peak Detectors (U440 and U340, diagram 10) for Self Calibration of the acquisition system. The test signal level, stored on capacitor C733, is applied to the input of an amplifier internal to U610 which has dual-differential outputs. The complementary-current outputs for each channel are approximately 6 mA ±1.25 mA.

Z-Axis Control

The Z-Axis Control stage consists of Q810, U811, U810A, U810B, five-transistor array U812, and associated components. Multiplexer U811 selects one of three intensity-control voltages—normal, intensified, or readout (output from Sample-and-Hold buffers U820B, U820C, or U820D) and routes it to a current source composed of U810A, U810B, and Q810. The amount of current passed by Q810 controls the display intensity. The transistors in array U812 form an automatic gain compensation circuit for Z-Axis Amplifier U227 (diagram 19).

Selecting an input to pass through multiplexer U811 is done by two active input signals, BRIGHTZ and RO. (The third select input is a permanent LO, so one of the first four inputs only can be selected.) For normal-intensity waveform displays, all select bits will be LO to select input 0 to switch through U811. If the waveform display should be intensified at any time, the BRIGHTZ input will go HI, selecting input 1. When readout is to be displayed, the RO input will go HI, selecting either input 3 or input 4, depending on the setting of the BRIGHTZ bit. Since inputs 3 and 4 are both connected to the INT-RO (readout intensity) control voltage level, the readout displays are not intensified.

The selected intensity control voltage is applied to U810B, configured as an inverting buffer with a gain of −1. The output voltage is offset −4.06 V by the voltage divider at pins 3 and 5 of U810 (R814 and R815) and resistor R816 at pin 6. The resulting inverted and shifted output is converted to a current by R812 and applied to the emitter of Q810.

The circuitry of operational amplifier U810A and transistor Q810 is arranged so that the transistor is on with its emitter held at −2.7 V. The −2.7 V level at the emitter is set by the bias on input pin 3 of operational amplifier U810A. The voltage developed at the output of U810B causes a current to flow in R812 and sets the current drive level for the Z-Axis circuit (diagram 19). This Z-INT drive current supplied via U812E from pin 14 may vary from 0 mA to 4 mA (−1.36 V to +1.36 V respectively at the output pin of multiplexer U811).

When the intensity of the selected display is at minimum, the output control voltage from multiplexer U811 will be below −1.36 V. This causes the output of U810B to go to approximately −2.7 V, reducing the emitter current to Q810 to approximately zero. Diode CR810 limits the reverse-bias voltage across the base-emitter junction of Q810 to about 0.6 volts and protects the base-emitter junction from excessive voltage.

Automatic compensation of the Z-Axis Amplifier gain is carried out in five-transistor array U812. Transistors U812B and U812C form the bias network for U812D, one-half of the Z-Drive compensation amplifier. Biasing for the other transistor of the differential pair is supplied by U812A, R817, and a resistor internal to the Z-Axis Amplifier that is tied to the +5 V_D supply. The differential amplifier pair is biased so that the total current is divided between the two sides. The resistance value of the internal resistor in the Z-Axis Amplifier is an indication of the gain of that device. Changes in that value that occur between different Z-Axis Amplifiers shift the biasing level of U812E to either increase or decrease the share of the total current through that transistor by a small amount. The change in current is in the appropriate direction to make the display intensity of different instruments comparable with exactly the same Intensity control settings. Capacitor C817 bypasses high-frequency noise present on the ZGAIN signal line.

The SPOTWOB (spot wobble) signal line, at the output of Operational Amplifier U810B, picks off the various intensity levels. Those levels are used in the Horizontal and Vertical Output Amplifiers (diagram 18) to dynamically correct intensity-related position shifts on the crt (described in the Display Output circuitry discussion).

Graticule Illumination

The Graticule Illumination circuit, composed of U820A, U520G, and associated components, sets the brightness of the three lamps used to light up the graticule lines etched on the crt faceplate.

Operational amplifier U820A is configured as an inverting integrator. Inverting buffer U520G may be thought of simply as an open-collector transistor following operational amplifier U820. The circuit appears this way because the negative feedback around the loop via U820 and voltage divider R824-R825 keeps U520G in its linear operating range. Gain around the loop (11) is set by the ratio of R822 to R823 plus 1. The DAC control voltage applied to pin 2 of U820A causes the integrator output to slowly ramp in the opposite direction. This output is inverted by U520G, and it sets the current in the graticule lamps. Between DAC-updates no integration takes place, and the charge held on C822 holds the output of the inverting buffer, and thereby the graticule lighting, constant.

Auxiliary Front Panel

The Auxiliary Front Panel circuitry provides a means of reading the front-panel bezel push buttons, located directly below the crt, as well as several analog voltages associated with the front-panel BNC input connectors. The circuit consist of analog multiplexer U600 (used to route the various analog voltages to the A/D converter), parallel-loading shift register U700 (used to relay switch-closure data to the Front Panel μP, shown in diagram 3), and associated components.

Analog multiplexer U600 routes one of the eight input levels to the A/D converter internal to Front Panel μP U700 (diagram 3), depending on the three-bit code applied to its select inputs. The selected signal may be one of the four probe-coding voltages (developed by the voltage divider formed by the encoding resistance of the probe attached to the input connectors and the associated pull-up resistor within R601), the CH1 OVL (overload) or CH2

OVL levels (used to indicate when an excessive voltage is applied to the input connector), or one of the two, 180 degree out-of-phase wipers on the Intensity control (a continuous-rotation pot).

Auxiliary Switch Register U700 performs a parallel load of the status of all of its input bits whenever the Front Panel μP puts out a SHCLK (shift clock) with the S/$\overline{L}$ (shift/load) select input of the register set LO. Once loaded, the S/$\overline{L}$ input is set HI, and the eight bits of switch-closure data are clocked out to the Front Panel μP on the SWOUTA (switch data out-auxiliary Front Panel) line with eight more clocks applied to the clock input of the Auxiliary Switch Register. Switches read include the five menu select switches on the lower edge of the crt bezel, the Intensity Control SELECT switch, the STATUS switch, and the MENU OFF/EXTENDED MENU switch.

SYSTEM CLOCKS

The System Clocks circuitry (diagram 7) produces the fixed-frequency System clocks signals used throughout the oscilloscope. These clocks are developed from a 40 MHz master clock frequency, and they are used to drive state machines that produce other special-purpose clocks that control the waveform acquisition processes.

Master Clock

The Master Clock circuit produces 20 MHz and 8 MHz clocks ($\overline{\text{C20M}}$ and C8M) by dividing down the output from the 40 MHz crystal oscillator circuit, Y611. The oscillator circuit drives both the divide-by-two flip-flop (U612A) and the divide-by-five circuit (flip-flops U612B, U615A, and U615B) in parallel via inverter U513A. The 20 MHz clock is obtained from flip-flop U612A. With its Set, Clear, J, and K inputs all held permanently HI, the flip-flop toggles on each negative-going 40 MHz clock edge to divide the input clock frequency by two.

The divide-by-five circuit is a state machine formed by J-K flip-flops U612B, U615A, and U615B. With the two feedback signals to the J and K inputs of U612B, the flip-flop chain sets logic level on the J and K inputs of U615B that allows its Q output to change states only every five 40 MHz input clocks to produce the 8 MHz clock.

Jumper J132 allows an external clock signal to be substituted for the 40 MHz clock signal to aid in testing and troubleshooting.

Secondary Clocks

The Secondary Clocks circuit further divides the 20 MHz clock to produce other system clock rates. The flip-flops within U710, along with logic gates U711A, U711B, U711C, and U712B, produce 10 MHz, 5 MHz, and 2.5 MHz clocks.

Flip-flop U710D and exclusive-OR gate U711C generate the 2.5 MHz clock (CLK3A) that is delayed 3/8 of a cycle (150 ns) with respect to the 2.5 MHz clock at the 3Q output (CLK1A). CLK1A, CLK2A, and CLK3A are used for control-clock generation in the Waveform Processor system (diagram 2). The 10 MHz clock output at J133 is provided as a trigger signal when troubleshooting the Waveform Processor system with a logic analyzer or test oscilloscope.

The CLK1A, CLK2A, and CLK3A clocks are buffered by U712A, U712C, and U712D to the Waveform μP. Buffering these clocks ensures that a fault on the buffered side will not halt operation of the Secondary Clock Generator circuit. Series-damping resistors R713, R715, and R716 reduce ringing in the interconnection cable. The 5 MHz clock is applied to multiplexer U722A, where it is available for selection (along with the $\overline{\text{4MHz}}$ clock) as the reference signal to Phase Clock Array phase-locked loop circuit (U381, diagram 11). The 5 MHz clock is also used in the Display Control circuitry, diagram 17.

Minimum-Delay 1 MHz Clock

The Minimum-Delay 1 MHz Clock circuit produces a 1 MHz clock (2XPC) whose transitions very nearly coincide with those of the 20 MHz clock. The requirements of the clock timing dictate that the delay between a rising edge of the 20 MHz clock (C20M2 on U720A pin 3) and the 2 MHz $\overline{\text{TTL4C}}$ (TTL-compatible phase 4 clock, originating from Phase Clock Array U470—diagram 11) transitions be less than 50 ns. Since the propagation delay (2XPC-to-$\overline{\text{TTL4C}}$ delay) through the Phase-Clock Array is a significant portion of the 50 ns allowed, the phase of the 2XPC (two-times CCD "C" register clock rate) clock relative to the 20 MHz clock must be optimized for minimum delay.

To obtain minimum delay, U622, U523B, and their associated logic gating are configured as a divide-by-20 counter whose output is synchronized to the 20 MHz clock (plus propagation delay through U523B). Counter U622 and NAND-gate U620C provide division by ten, producing a 2 MHz clock (4XPC) at pin 11 of U622. This clock is inverted by U513F and is used in the A/D Converter and Acquisition Latches circuit (diagram 15). The uninverted 4XPC clock is used as the SR (shift right) data input for shift register U642 to produce two delayed 4XPC clocks ($D_1$4XPC and $D_2$4XPC).

After one run through the counting cycle at power-on, any unknown counter states in divide-by-ten counter U622 are resolved, and the circuit counts in the following manner: If the circuit does not start in the Load condition, it will be in the Count mode (a HI on pin 9 from the output of NAND-gate U620C) and the 20 MHz clocks cause the counter output to increment until it reaches 1100 (binary). At this point the output of U620C will go LO, causing the counter to load the count 0011 (binary) from its inputs with the next clock. Once the counter is loaded, the output of U620C will return HI, and normal counting from a known state commences. When the counter reaches 1100 again, the load-count sequence will be repeated, requiring ten 20 MHz clocks to complete the cycle.

AND-gate U623C watches the three lowest bits of the counter outputs (Q_A, Q_B, and Q_C). The output of U623C (pin 8) will be HI during the "7" state (0111 binary) of each 10-count cycle and will stay HI for one 20 MHz clock cycle (50 ns). This HI is applied to the K input and the J input (via OR-gate U522B) of flip-flop U523B. With the K and J inputs both HI, the flip-flop toggles when the next 20 MHz clock arrives. Assuming the Q output of the flip-flop was LO, toggling to a HI applies a HI to the J input via OR-gate U522B. When the output of U623C returns LO (next 20 MHz clock), the J and K input states of the flip-flop will keep the Q output HI with subsequent 20 MHz clocks.

The Q output of U523B will stay HI until the next seven (0111) state from AND-gate U623C arrives, at which time the J and K inputs are again set HI. On the rising edge of the next 20 MHz clock the Q output of flip-flop U523B toggles LO. When the 50 ns pulse from U623C returns LO, the J and K input states will both be LO, and further 20 MHz clocks are prevented from changing the Q output state of the flip-flop. The output remains LO until the next HI state from U623C starts the divide sequence over again. Note that transitions of the 1 MHz signal (2XPC) at pin 9 of U523B are delayed from the $\overline{\text{C20M}}$ (20 MHz clock) clock rising-edge transitions by only the propagation delay through the flip-flop (about 7 ns).

CCD Output-Sample Clocks

The CCD (charge-couple devices) Output-Sample Clocks stage controls signal transfers from the Acquisition CCD-Clock Drivers (diagram 10) to the external CCD Output circuitry (diagram 14). It consists of a state machine synchronized to the 20 MHz clock (and thus the CCD events) and produces clocks to: (1) move sampled data out of the CH1 CCD array, (2) move sampled data out of the CH2 CCD array, (3) reset both the CH1 and CH2 CCD array output-charge wells in preparation for the next transfer, and (4) phase-lock the CCD-Data Clock stage. Figure 3-3 illustrates the timing of these clocks and other clocks in the System Clock Generator; it may be of use in following the discussion of circuit operation.

When acquired samples are to be shifted out of the CH1 and CH2 CCD array, the TTL version of the Phase-Clock 04 output ($\overline{\text{TTL4C}}$ from Phase Clock Array U470) will be toggling at 500 kHz. Transitions of the $\overline{\text{TTL4C}}$ clock are resynchronized to the 20 MHz clock (C20M2) by flip-flop U720A to correct the phase between the $\overline{\text{TTL4C}}$ clock and the state machine outputs. This correction closely synchronizes charge transfers within the CCD (relative to the 2XPC clock) with the signal transfers out of the CCD.

When the $\overline{\text{SYNC4C}}$ (synchronized phase-4 clock) is LO (pin 5 of flip-flop U720A), the LOAD signal applied to shift registers U730 and U830 (via AND-gate U623B and inverter U513E) will be HI. This HI, along with the HI SYNC4C signal from pin 6 of flip-flop U720A, causes both shift registers to do a parallel load of the fixed logic levels applied to their D input pins. The levels loaded set the $\overline{\text{OS1}}$ (sample CH1-CCD outputs), $\overline{\text{OS2}}$ (sample CH2-CCD outputs), and the $\overline{\text{RST}}$ (reset CCD output wells) outputs from U730, and the $\overline{\text{SYNC}}$ (sync data clocks) output from U830 all HI. The HI $\overline{\text{RST}}$ level applied back to U621 and the HI output from NAND-gate U620B will be loaded into counter U621 as 0101 binary because of the LO $\overline{\text{LOAD}}$ output of U623B applied to the CT/$\overline{\text{LD}}$ input pin. This state then stays as is for the remainder of the LO state of the $\overline{\text{SYNC4C}}$ signal.

When the $\overline{\text{SYNC4C}}$ output of flip-flop U720A returns HI, counter U621 is enabled by the HI from AND-gate U623B to count for three, 20 MHz clock cycles (150 ns), reaching the count of 0111 binary. The next clock toggles the Q_C output of U621 LO (count goes to 1000 binary), and the $\overline{\text{LOAD}}$ output from AND-gate U623B is forced LO. The HI LOAD signal output obtained from inverter U513E, along with the LO SYNC4C from flip-flop U720A pin 6, sets up shift registers U730 and U830 to shift right. The next 20 MHz clock (250 ns after the 2XPC clock toggled) shifts a LO to the $\overline{\text{OS1}}$ output of U730 (pin 14) and loads a binary 0100 into counter U621 (since the output of NAND-gate U620B is now LO). The fixed HI applied to the SR data input of U730 is shifted to the Q_A output.

After 0100 is loaded into counter U621, the $\overline{\text{LOAD}}$ output of U623B returns HI (since pin 12 of U621 has been set HI by the inputs loaded into the counter). This once again produces a LO LOAD output from inverter U513E and prevents U730 and U830 from shifting. Counter U621 counts four cycles of the 20 MHz clock (200 ns), reaching count 0111. The next 20 MHz clock toggles the Q_C output of U621 LO and sets the $\overline{\text{LOAD}}$ line LO once again, enabling shift registers U730 and U830. The next clock (250 ns) shifts the previously loaded LO from the $\overline{\text{OS1}}$ output right to the $\overline{\text{OS2}}$ output of U730 and moves a HI from the SR data input into the $\overline{\text{OS1}}$ output. At the same time, counter U621 is reloaded to 0100 binary to again restart its count.

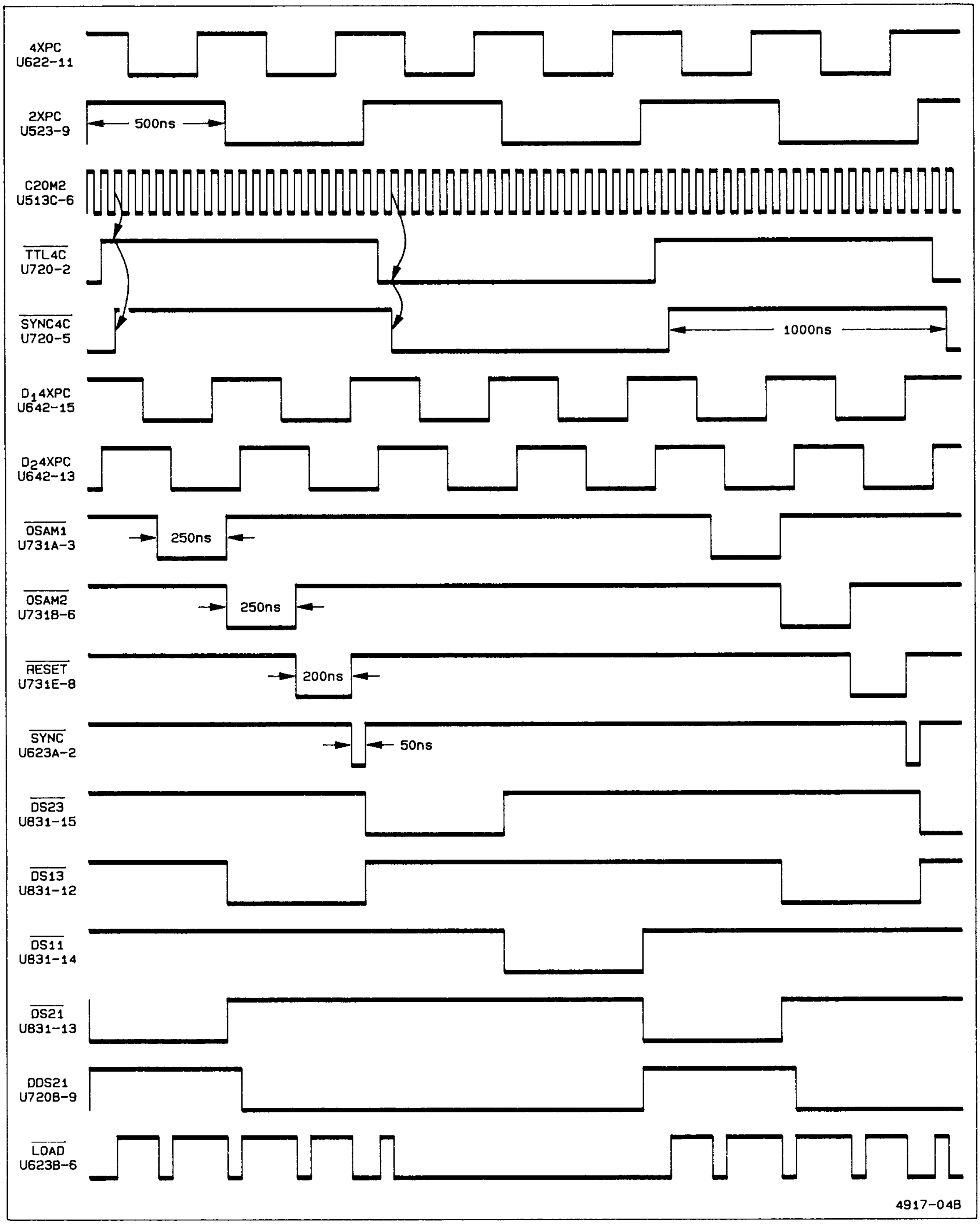


Figure 3-3. System Clock waveforms.

A similar 250 ns cycle occurs for the $\overline{\text{OS2}}$ LO state, ending with the LO being shifted to the Q_D output of U730. However, when the load is done to U621 this time, the $\overline{\text{OS2}}$ output to NAND-gate U620B is LO, and counter U621 is loaded with 0101 binary (the D_A) input from U620B is HI).

Since U621 now needs one less clock to count to 0111, $\overline{\text{RST}}$ (and thus $\overline{\text{RESET}}$ remains LO for 200 ns (rather than 250 ns as for $\overline{\text{OS1}}$ and $\overline{\text{OS2}}$), after which time the next load of U621 will occur. At the end of the reset time, both $\overline{\text{RST}}$ and the DA output of U620B are both LO, so counter U621 loads to 0000 binary. On the same 20 MHz clock, the LO $\overline{\text{RST}}$ level present on the SR data input of U830 is shifted right to the Q_A ($\overline{\text{SYNC}}$) output. This state (with $\overline{\text{SYNC}}$ LO) lasts one clock cycle (50 ns) only, because Q_C is still LO, causing LOAD to go HI and, therefore, causing the shift register to again shift right, resulting in $\overline{\text{SYNC}}$ going HI. On the next 20 MHz clock pulse, the $\overline{\text{TTL4C}}$ input is LO, causing $\overline{\text{SYNC4C}}$ to go LO on the clock edge. This starts the whole process over, and it is repeated until all samples have been moved out of the CCD arrays.

AND-gates U731A, U731B, and U731C buffer the outputs of counter U730 and ensure that the counter and the clock circuit will keep running even if a short occurs on the buffered $\overline{\text{OSAM1}}$, $\overline{\text{OSAM2}}$, or $\overline{\text{RESET}}$ lines.

CCD Data Clocks

The CCD Data Clocks ($\overline{\text{DS11}}$, $\overline{\text{DS13}}$, $\overline{\text{DS21}}$, and $\overline{\text{DS23}}$), generated by counter U721, shift register U831, and the associated logic gating, are responsible for multiplexing the four CCD array output levels (CH 1-1, CH 1-3, CH 2-1, and CH 2-3) onto the CCD DATA line for digitization by the A/D Converter. Figure 3-3 (shown previously) illustrates timing of the stage.

When the $\overline{\text{SYNC}}$ output from U830 pin 15 goes LO (for 50 ns at the end of the $\overline{\text{TTL4C}}$ cycle), the outputs of NAND-gate U620A and inverter U513D go HI, and the output of AND-gate U623A goes LO. This places counter U721 and shift register U831 in their parallel load mode, and the next 20 MHz clock rising edge (start of next $\overline{\text{TTL4C}}$) loads in the fixed logic levels at their D inputs. The data bits (1000 binary) loaded into shift register U831 set the DS23 (data select CH2 phase-3) output bit (pin 15) HI, with all other output bits LO. The LO $\overline{\text{DS23}}$ output from inverter U832D is applied to Q880 (diagram 14) to switch the CCD output data from the CH2 CCD array phase-3 output onto the CCD DATA line, where it is applied to A/D Converter U560 (diagram 15).

That same 20 MHz clock loads counter U721 with 0111 binary and clocks $\overline{\text{SYNC}}$ from pin 15 of U830 HI. With $\overline{\text{SYNC}}$ HI, shift register U831 is in hold mode, and counter U721 is enabled to count via AND-gate U623A. Counter U721 increments from the beginning count of 0111 to 0000 (nine, 20 MHz clocks—450 ns), at which time the $\overline{\text{SHIFT}}$ output from OR-gate U522A goes LO. This sets up shift register U831 (via U620A) to shift and via U623A places U721 in load mode. The next 20 MHz clock (at 500 ns) shifts a new LO from the SR data input of U831 into the Q_A output and shifts the HI from the Q_A output to the Q_B output (DS11). Counter U721 is also reloaded with 0111 binary for the next count cycle.

Similar 500 ns count cycles shift the HI bit to each output of shift register U831 in succession until, during the last 50 ns of the HI state of the DS13 signal (U831 pin 15), $\overline{\text{SYNC}}$ goes LO again. The LO sets up U721 and U831 to load on the next 20 MHz clock. The next clock (concurrent with $\overline{\text{TTL4C}}$ going LO) loads both U721 and U831 and starts the cycle over again. The arrival of the $\overline{\text{SYNC}}$ signal ensures that the presetting load of U721 and U831 always occurs concurrently with $\overline{\text{TTL4C}}$ going LO. The four data-select clocks (and their inverted outputs) are thereby synchronized to CCD array output cycles.

The DS21 signal is also applied to a circuit formed by flip-flop U720B and exclusive-OR gate U711D. One input of U711D is held permanently HI so the gate acts as an inverter for the DS21 signal on the other input. When the DS21 logic level goes HI, the output of U711D goes LO and flip-flop U720B become set with the Q output (pin 9) HI. At the end of the HI logic level, the DS21 signal goes LO, but the Q output remains HI until the next rising edge of the $D_1$4XPC clock (4XPC delayed by one 20 MHz clock cycle) clocks the LO on the D input through the flip-flop. This circuit action has the effect of stretching the DS21 signal by 50 ns. The resulting DDS21 signal is applied to Time Base Controller U670 (diagram 8).

The delayed $D_1$4XPC and $D_2$4XPC clocks are produced by using the 4XPC clock as the data source for the shift-right input to register U162 and clocking that data right to the shift register outputs with the 20 MHz clock (C20M1). The first output signal (Q_A) is delayed from the input clock by 50 ns and the second (Q_C) by 150 ns. $D_2$4XPC is applied to NAND-gate U650B (diagram 8) for use is controlling the timing of the $\overline{\text{SAVEACQ}}$ signal to the Acquisition Memory. The time delay ensures that the data written to Memory has stabilized at the output of the A/D Converter.

Reference Frequency Selector

The PLL (phase-locked loop) Reference Frequency Selector, U722A, selects either a 4 MHz or a 5 MHz clock signal as the reference frequency to the Phase-Locked Loop (PLL) circuit (U381, diagram 11). The Phase-Clock Oscillator in the PLL circuit runs at 50 times the selected reference frequency, so sampling clocks to Phase Clock Array U470 are generated at a rate of either 200 MHz or 250 MHz. The two choices of signal frequencies provide the correct input frequency to the internal dividers of the Phase Clock Array needed to generate the clocks for each SEC/DIV setting sample rate.

Flip-flop U523A is configured as a divide-by-two circuit that divides the 8 MHz (C8M) clock to produce a $\overline{4MHz}$ clock at its $\overline{Q}$ output (pin 6). The SEL4/5 (select 4 MHz/5 MHz) signal on pin 14 of U722A selects whether this 4 MHz clock or the 5 MHz clock from U710 will appear at the REF4/5 output pin. The signal inputs to the multiplexer are connected so that when SEL4/5 is HI, the 5 MHz clock is selected (no matter what state the other select input, shown with U722B, is in); when it is LO, the 4 MHz clock is selected. The $\overline{4MHz}$ signal is inverted by U832F and applied to the Front-Panel μP (U700, diagram 3) as the clocking frequency.

TIME BASE CONTROLLER AND ACQUISITION MEMORY

Time Base Controller (U670, diagram 8) and its associated gating circuitry generates the control signals and clocks to cause acquisitions in the various modes to occur. It keeps track of how the acquisition is progressing, starts the digitization of the samples by the A/D Converter when the correct number of data points have been acquired, and moves the digitized samples to Acquisition Memory (U600). The Acquisition Memory provides temporary storage of the converted data to permit the Waveform μP to access the data as it is needed to update the display.

Time Base Controller

Time Base Controller U670 monitors and controls the various acquisition functions. Two different operating modes of the CCD (charge-coupled devices) arrays must be controlled by U670; these are the FISO mode (fast-in, slow-out) and the Short-Pipe mode (slow-in, slow-out). FISO mode is used at sweep speeds faster than 100 μs/div when the analog sampling must occur at the fastest possible rate. The Short-Pipe mode is used for lower frequency signals when the A/D conversion rate is much faster than the signals being sampled.

The major Time Base Controller functions in FISO (fast-in, slow-out) mode are:

- Ensure that enough samples are in the CCD array "B" register to fill the "pretrigger" requirements.
- Ensure that the proper number of "post-trigger" samples are moved into the "B" register after triggering occurs.
- Discard the proper number of unneeded samples at the start of "slow-out" conversion.
- Ensure that exactly 1024 samples are moved to the Acquisition Memory during the "slow-out" conversion process.

Major functions in Short-Pipe mode are:

- Ensure that valid data has made it through the "short-pipe" path of the CCD arrays.
- Synthesize the proper sample rate called for by the SEC/DIV setting.
- Ensure that enough samples have been saved in the Acquisition Memory to fill pretrigger requirements before enabling the Triggers.
- Ensure that the proper number of post-trigger samples are stored into the Acquisition Memory after the trigger event.

The instruction registers within Time Base Controller U670 are enabled when $\overline{TBSEL}$ from the System μP is LO. A register is selected for writing to or reading from by address lines A0, A1, and A2. Setup data from the System μP data bus is buffered to the selected register via bidirectional buffer U641 and written into the selected internal register by the $\overline{WR}$ (write) signal applied to pin 14. Acquisition mode, SEC/DIV setting, trigger position, and several other functions are controlled by the System μP via the commands written to the instruction registers within U670. Status data and register contents may be read out of the Time Base Controller registers by the System μP in a similar manner using the $\overline{RD}$ (read) signal to reverse the data paths in buffer U641 and the internal circuitry of U670.

The FISO (fast-in, slow-out, pin 36), ROLL (pin 2), SEL4/5 (select reference—4 MHz/5 MHz, pin 28), and ENVL (envelope, pin 39) outputs are set indirectly by System μP writes to the internal control registers at the start of each acquisition cycle. Control signals are then output by an internal state machine of the Time Base Controller to dynamically control the acquisition circuitry in the required mode and signal acquisition rate (set by a combination of FISO and SEL4/5). Writing to these "register" locations also allows the System μP to generate several strobes for internal latching and control functions.

A state machine internal to Time Base Controller U670 runs the acquisition process from start to finish. When all internal registers are properly loaded, the System μP writes to location 6022(h), generating a strobe that switches acquisition control to the Time Base Controller. This starts the acquisition system, and samples are taken in the defined mode. For FISO operations, the following occurs.

A counter internal to U670 begins counting $\overline{\text{TTL1B}}$ (TTL version—Phase 1B) clocks to determine when at least enough samples have been transferred into the "B" register of the CCD arrays to fill "pretrigger" requirements. Samples will then continue to be placed in the B register, but no output samples will be saved until the record trigger occurs. (All 1054 locations in the two sides of 16 × 33 B register will fill if a record trigger does not occur before that many samples have been taken.) Each $\overline{\text{TTL1B}}$ clock represents 32 analog samples (two, 16-sample sides) transferred into the CCD array B register. When the proper number of pretrigger samples have been loaded, U670 will set its EPTHO (end of pretrigger holdoff) line HI. This signal enables Trigger Logic Array U370 (diagram 11), and the state machine in Time Base Controller U670 starts watching the SYNTRIG (synchronized trigger) input (pin 30) from the Phase Clock Array (U470, diagram 11) for the "record" trigger. In the meantime, the Trigger Logic Array will be counting delay clocks (DELCLK) to fulfill any specified delay requirements before a record trigger is permitted to be generated.

When the delay requirements are met, the SYNTRIG is allowed to occur when a trigger event occurs. The counter then watches $\overline{\text{TTL1B}}$ to determine when the proper number of post-trigger samples have been moved to the B register to fill the post-trigger requirements, then it sets SO (slow-out, pin 38) HI. This stops the sampling process and starts A/D conversion of the analog samples stored in the CCD array B register.

Since the trigger event can occur at any one of the 32 analog samples that are taken between each TTL1B clock, and since the Time Base Controller only keeps track of the number of pretrigger and post-trigger samples in terms of these 32-sample records, there are usually some samples at the beginning of those in the CCD array B register that are extra. When the analog samples are serially moved out of the CCD array for digitization, these extra samples must be ignored in order to maintain proper trigger location within the complete record. The CCD Phase Clock Array (U470) knows where the record trigger occurred relative to the $\overline{\text{TTL1B}}$ pulse (1-of-32 position) and sends this information to U670 on the TL0-TL4 (trigger location bits 0 through 4) lines. This trigger-location number is loaded into the counter and, as the samples are moved out of the CCD array, that number of samples is essentially discarded. Those samples are A/D converted but will not be stored because U650B is not yet enabled to gate the $\overline{\text{SAVEACQ}}$ signal used to write the data into the Acquisition Memory.

Once the extra samples have been counted, the ACQUIRE output is set HI, enabling U650B. Since the instrument is in FISO mode, the output of U512C will be HI and the $\overline{\text{SAVEACQ}}$ signal used to save waveform data into the Acquisition Memory (via U501) is controlled by the output of U642 (diagram 7). This input to NAND-gate U650B is a delayed version of the 4XPC (2 MHz) clock ($D_2$4XPC). The 150 ns delay provided ensures that the A/D Converter output byte has settled before being written to the Acquisition Memory.

When the Time Base Controller is in control of writing data to the Acquisition Memory, the $\overline{\text{SAVEACQ}}$ clock is routed through U501 of the Mode Control Logic and becomes the $\overline{\text{WE}}$ (write enable) clock used to write waveform data into Acquisition Memory U600. That data is obtained from the Acquisition Latches (diagram 15) via buffer U613. The $\overline{\text{WE}}$ signal is also used to increment the Memory Address Counter (U300, U400, and U401) the result being that digitized samples from the Acquisition Latches are saved interleaved in consecutive memory locations. Each address is latched into the Record-Start Address Latches (U502 and U601) as the data-write ends, so that the address of the last-stored sample is always available. This information is used as a pointer when generating waveform displays.

As the digitized samples are moved to Acquisition Memory, an internal counter in Time Base Controller U670 watches the DS21 and DS23 clocks (pins 6 and 17) to determine when 1024 points (or 512 max/min pairs in Envelope mode) from each CCD array (CH 1 and CH 2) have been stored. When 2048 samples have been saved, the Time Base Controller will set ACQUIRE (pin 24) LO, disabling memory saves, and it will set its ACQDN (acquisition done) status line (pin 25) HI. The Waveform μP (U470, diagram 2) then takes over for transfer of the acquired waveforms to the Waveform μP Save Memory.

When the Waveform μP (U470, diagram 2) reads the HI ACQDN status via U542 (diagram 2), it reads the address of the last-saved point from the Record-End Latch (U502 and U601). Since the Acquisition Memory addresses are circular (incrementing the Address Counter from its last address goes back to the first address), it knows the record begins at the next address. With TB2MEM LO, the $\overline{\text{ACQ}}$ signal is routed through Mode Logic Switch U501 to become the $\overline{\text{WP2MEM}}$ signal. The $\overline{\text{ACQ}}$ signal going LO from the Waveform μP via address decoder U570 enables data buffer U610 to permit the Waveform μP to access the waveform data stored in the Acquisition Memory (see "Waveform Processor System" description).

SHORT-PIPE OPERATION. Short-Pipe operation is similar to FISO in the way mode and setup data is loaded and the way the internal counter is used to keep track of various events. The major differences are: Short-Pipe mode moves input samples directly from the CCD array "A" register input, down the first "B" register channel and out of the CCD array through the "C" register. Short-Pipe mode must also synthesize the sample clock rate.

To synthesize the sample rate for the Short-Pipe mode, FISO (from U670 pin 36) is set LO by the System μP, thereby enabling the CE2B/N (clock enable 2B divided by N) input to U512C. The CE2B/N clock (along with the $D_2$4XPC clock) then controls saving the waveform data into the Acquisition Memory. In Short-Pipe mode, CCD sampling occurs at a continuous 1 MHz rate, but due to SEC/DIV setting data written to an internal counter in U670, the synthesized $\overline{\text{CE2B/N}}$ clock will only allow every "Nth" point to be saved in Acquisition memory to produce only 50 data points per division in the display. Samples between the saved Nth points are ignored. The synthesized $\overline{\text{CE2B/N}}$ clock will only enable U650B long enough to save either two or four points and is dependent on the sweep-rate division factor written to the internal counter. This allows effective sample rates down to 1 sample every 2 μs (100 μs/div) to be achieved. The SDC (slow-delay clock, U670—pin 29) runs at this effective sample rate and allows the Trigger circuits to count delay periods in terms of sample intervals.

Since CCD array samples are moved directly from the input to the output via the first B register and since stored samples may occur at a rate different than the sample rate, pretrigger and post-trigger counting is done relative to samples actually stored into the Acquisition Memory. When enough valid pretrigger points have been saved, EPTHO enables the Triggers. Data is saved in bursts of two points (four points in ENVELOPE acquisition mode), one for CH 1 and one for CH 2, at the synthesized rate. When the trigger event occurs, the Trigger location bits are set relative to the synthesized clock and allow a data correction algorithm to correct already-acquired data points relative to the trigger event. Post-trigger sampling occurs at the defined rate, and since A/D converted data already is stored in Acquisition Memory, ACQDN is set. Waveform data bytes are moved to the Save Memory by the Waveform μP and control is given back to the System μP.

LOAD LATCHES FLIP-FLOP. In Envelope Mode, Load Latches flip-flop U651A puts out a signal at the beginning of each envelope sampling interval that is HI for four acquisition cycles. That HI LOAD LATCHES signal loads the first four acquired data points (two min-max pairs) into the Acquisition Latches to be used for min-max comparison to the following waveform samples in that Envelope sampling interval.

The Set input of U651A is HI during Envelope, the output of the flip-flop is controlled by the DS23 clock and the CE2B/N clock (on the D input). The CE2B/N clock is a divided down DS23 clock, with the division factor depending on the SEC/DIV setting. The division factor determines how many waveform samples will be compared for new max and new min during each envelope sampling interval. Only the maximum and minimum waveform data point values that occur during the envelope sampling interval are transferred to the Acquisition Memory.

For non-envelope acquisitions, ENVL is LO. The Set input of flip-flop U651A is therefore asserted, and U651A will be held in the Set state with the Q output (LOAD LATCHES) held HI. That constant HI signal applied to the Acquisition Latch Switching circuitry causes each data point acquired to be loaded into the Acquisition Latches and transferred into Acquisition Memory.

ROLL LOGIC. In ROLL mode the display is constantly being updated as new data points are available. A means is provided to tell the Waveform μP when new data points are available. An interrupt to the Waveform μP is generated by the Roll Logic flip-flop, U651B. When the ACQUIRE signal from Time Base Controller U670 goes HI, new waveform data points are acquired. The HI state of that signal is clocked to the Q output of flip-flop U651B on the rising edge of the $\overline{\text{CE2B/N}}$ signal; the same signal that causes the sample data to be saved into the Acquisition Memory in Short-Pipe mode. The PTAVAIL signal at the Q output is an interrupt to the Waveform μP. When the Waveform μP services the interrupt request, it sets $\overline{\text{PTACK}}$ (point acknowledge) LO via U500B and U500C to reset the flip-flop in preparation for the next new data points. The saved points are also moved to the Save Memory and then to the Display Memory for a display update.

In NORMAL mode, the ROLL signal is LO, and NAND-gate U500B outputs a continuous logic HI that holds the Roll Logic flip-flop in the Reset state (with the Q output LO).

Memory Mode Control

The Memory Mode Control circuit is made up primarily of Mode Selector Switch U501, a quad 2-to-1 multiplexer that switches control signals between those of Time Base Controller U670 and those of the Waveform μP. Selection is done by the TB2MEM signal from AND-gate U731D pin 11.

The $\overline{\text{WE}}$ (write enable) output from Mode Selector Switch U501, pin 12, controls both writing into the Acquisition Memory and incrementing of the Address Counter. With TB2MEM set LO, the $\overline{\text{WWR}}$ (Waveform μP write) signal gated through OR-gate U512D to the 4A input (pin 13) of U501 controls writing to the Acquisition Memory. The $\overline{\text{OE}}$ (output enable) derived from the Waveform μP $\overline{\text{WRD}}$ (Waveform μP read signal), controls the output of Acquisition Memory data. It is asserted LO only when the Waveform μP is trying to read Acquisition Memory locations.

With TB2MEM HI, the $\overline{\text{SAVEACQ}}$ signal from NAND-gate U650B, is selected as the $\overline{\text{WE}}$ signal, and the $\overline{\text{OE}}$ is set HI to disable the Acquisition Memory from outputting data. Data buffer U613 is enabled by the LO level of the $\overline{\text{EOE}}$ signal from pin 7 of the Mode Select Switch to connect the the Envelope Logic Latch bus to the input bus of the Acquisition Memory.

When the Waveform μP wants to access the Acquisition Memory, it will set the $\overline{\text{ACQ}}$ line LO to enable its control signals to the inputs of Mode Logic Switch U501 and wait for the ACQUIRE signal from Time Base Controller U670 (diagram 8) to go LO (indicating that the Time Base Controller is finished acquiring). When ACQUIRE goes LO, the output of AND-gate U731D (TB2MEM) goes LO and the Mode Logic Switch select the Waveform μP signals to control the Acquisition Memory. The LO TB2MEM signal also sets the Address Counters to their Load state, and the counter outputs then follow the WA0-WAA (Waveform μP address bits 0-A) lines, giving direct access to Acquisition Memory data locations by the Waveform μP.

Address Counter

The Address Counter increments the Acquisition Memory address as each point is saved. Each write into Acquisition Memory ends with the $\overline{\text{WE}}$ (write enable) signal going HI, clocking the counter to address the next sequential Acquisition Memory location.

The TB2MEM signal from AND-gate U731D controls the mode of the Acquisition Memory Address Counter (composed of binary counters U300, U400, and U401). When the the TB2MEM signal goes LO, the counters become "transparent." This connects the Waveform μP address bus to the address inputs of the Acquisition Memory so that the Address Counter output follows the WA0-WAA (Waveform μP address bits 0-A) lines. When the TB2MEM signal is HI, the Time Base Controller is in control of the Acquisition Memory, and counter will be in its count mode as the acquired signals are being stored into the Acquisition Memory.

Acquisition Memory

Acquisition Memory U600 is a random-access memory device (RAM) that provides temporary storage of acquired data points before they are moved into Save Memory. Analog waveform samples from the CH 1 and CH 2 CCD arrays are digitized and moved into Acquisition Memory under control of the Time Base Controller (diagram 8), alternating CH 1 data with CH 2 data. The Waveform μP reads the data out of Acquisition Memory via buffer U610, unscrambles it, and moves it to proper Save Memory locations.

MEMORY INPUT BUFFER. Memory Input Buffer U613 applies the time-multiplexed waveform data bytes from the Acquisition Latches (diagram 15) to the data inputs of the Acquisition Memory inputs at all times except when the Waveform μP is accessing the Memory. Inverter U620D inverts the most-significant bit of the sample data so that range center of the A/D Converter output corresponds to 00 hex (center screen value), thereby creating bipolar data referenced to center screen.

Record-End Latch

The Record End Latch composed of U502 and U601 continually latches the address of the last Acquisition memory location that was written. The latch is clocked on the rising edge of the $\overline{\text{WE}}$ clock (from the $\overline{\text{SAVEACQ}}$ signal or the Waveform μP $\overline{\text{WWR}}$ signal via Mode Logic Switch U501) and provides the Waveform μP with the last address written (the end of the record for a full acquisition) by the Time Base Controller or read by the Waveform μP. Since the Acquisition Memory addresses are circular, the start of a FISO record will always be the Record End address plus one. In Short-Pipe mode, the Waveform μP will read those (two for normal, four for envelope) points immediately preceding (and including) the Record End address. The latched address (plus the trigger location data) is placed on the Waveform μP data bus by asserting $\overline{\text{RDMAR0}}$ and $\overline{\text{RDMAR1}}$ (read memory address) lines.

Two-to-one multiplexer U722B applies either trigger-location bit 4 (TL4) or the Time Base Controller TBTRIG (time base triggered) status bit to latch U502, depending on whether FISO or Short-Pipe mode is called for. The TBTRIG bit used in Short-Pipe mode tells the Waveform μP when the Time Base Controller detected Record Triggering.

ATTENUATORS AND PREAMPLIFIERS

The Attenuator and Preamplifier circuitry (diagram 9) allows the operator to select the vertical deflection factors. The Front Panel μP monitors the Channel VOLTS/DIV switches and VOLTS/DIV VAR controls and passes changes to the settings to the System μP which then digitally switches the attenuators and sets the Preamplifier gains accordingly. Vertical Couplings are similarly controlled.

Channel 1 and Channel 2 Attenuators

The Channel 1 and Channel 2 Attenuators are identical in operation, with corresponding circuitry in each channel performing the same function. Therefore, only the Channel 1 circuitry is described.

An input signal from the Channel 1 input connector is routed through an attenuator network by four pairs of magnetic-latch relay contacts. The position of the relays is set by data placed into Attenuator Control Register U511 by the System μP. Relay buffers U510 and U520A and ATTEN CLK circuitry, U520D, Q620, and Q621 provide the necessary drive current to the relay coils.

Four input coupling modes (1 MΩ AC, GND, 1 MΩ DC, and 50 Ω DC) and three attenuation factors (1X, 10X, and 100X) may be selected by closing different combinations of relay contacts. The relay contacts are magnetically latched and, once set, remain in position until new attenuator settings are loaded into the Attenuator Control Register and clocked by the ATTEN CLK circuitry. (See the "Attenuator Control Register" description for a discussion of the relay-latching procedure.) The three attenuation factors, along with the programmable and variable gain factors of the Vertical Preamplifier, are used to the obtain complete range of vertical deflection factors.

The 50 Ω termination resistor has a thermal sensor associated with it that produces a dc voltage (CH 1 OVL) proportional to the input power. Should the input power exceed the normal safe operating level for the 50 Ω DC input, the output voltage from the thermal sensor will exceed the normal operating limit. The amplitude of this dc level is periodically checked by the Front Panel μP to detect if an overload condition is present. If an overload occurs, the System μP switches the input coupling to the 1 MΩ position to prevent damage to the attenuator, and the error message "50 Ω OVERLOAD" is displayed on the crt. At power-off, the input coupling is automatically switched to the 1 MΩ position to prevent an unmonitored overload condition from accidently occurring.

Compensating capacitor C414 is manually adjusted at the time of calibration to normalize input capacitance of the preamplifier to the attenuator.

A probe-coding ring around the BNC input connector passes probe-coding information (a resistance value to ground) to the Front Panel μP for detection of probe attenuation factors. The readout scale factors are then set to reflect the attenuation factor of the attached probe.

Attenuator Control Register and Attenuator Clock

The Attenuator Control Register, composed of shift registers U511 and U221, allows the System μP to control the settings of the input coupling and attenuation factors. To set the input coupling mode and attenuation factors for Channel 1 and Channel 2, a series of eight 16-bit control words are serially clocked into U221 and U511 (eight bits in each register). Each control word is used to set the position of one of the eight attenuator and coupling relays (four relays are in each attenuator assembly). Each control word will have only the bit corresponding to the specific relay contact to be closed set HI. Relay buffers U510 and U520A (for Channel 1) and U220 and U520B (for Channel 2) are open-collector drivers that invert the polarities of all bits. This results in a LO being applied to only the coil lead associated with the contact to be closed; all other coil leads are held HI.

ATTENUATOR CLK CIRCUIT. To set a relay once the control word is loaded, the System μP generates an ATTN CLK (attenuator clock) to U520D pin 4 via R530 and C530. The strobe pulses the output of U520D LO for a short time. This output pulse attempts to turn on both Q620 and Q621 (relay drivers) via their identical base-bias networks. Due to the lower level from the turned on Darlington relay buffer (coupled through the associated coil diode and either CR610 or CR622 to one of the bias networks), one transistor will turn on harder as the ATTN CLK pulse begins to forward bias the transistors. The more positive collector voltage of the transistor turning on harder is fed through the bias diode (again either CR610 or CR622) to further turn off the opposite transistor. This action results in one transistor being fully on and the other one being fully off. The saturated transistor supplies a current path through the two stacked relay coils to the LO output of either U221 or U511 to close the selected contacts. Once set, the magnetic-latch feature will hold the relay set to this position until opposing data is clocked into the Attenuator Control Register and strobed into the relay. All coil leads for the remaining relays are set HI, and only the selected relay will be set.

To set the seven remaining Attenuator and coupling relays, the sequence just described is repeated seven more times. Whenever the System μP is informed by the Front Panel μP that the attenuation factor or input coupling has changed, the entire relay-setting procedure is repeated for all eight relays.

The MSB (most-significant bit) of the Attenuator Control Register, ATD15, is routed back to the System μP via CR287 and U380A (diagram 5), allowing diagnostic readback of the register contents.

Channel 1 Preamplifier

Preamplifier U420 converts the single-ended input signal from the Channel 1 Attenuator to a differential output signal used to drive the Channel 1 Peak Detector (U440, diagram 10). The device provides amplification in predefined increments, depending on the control data written to it from the System μP. The Preamplifier also has provisions for signal inversion, variable gain, vertical positioning, trigger signal pickoff, and balance control.

The Channel 1 vertical input signal is applied to pin A of Channel 1 Preamplifier U420 via C1005, R1005, and R1015. Resistor R1015 is a damping resistor, and the two series diodes to the −8 V supply, CR410 and CR411, protect the Preamplifier input from excessive negative voltages. The differential Preamplifier signal outputs (+OUT and −OUT) sink 12 mA of common-mode current from the Channel 1 Peak Detector inputs and drive those 75 Ω inputs with a 0.25 mA per division output signal.

Control data from the System μP is clocked into the internal control register of U420 via pin 22 (CD) by the clock signal applied to pin 23 ($\overline{CC}$). This data causes the Preamplifier either to multiply the normalized gain (5 mV/div) by 2.5 or 1 or to divide the normalized gain by 2, 4, or 10. The resulting sensitivities are 2 mV/div, 5 mV/div, 10 mV/div, 20 mV/div, and 50 mV/div respectively.

Three analog control voltages set by the DAC System circuitry (diagrams 5 and 6) modify the differential output signal at pins 9 and 10 of the Preamplifier. CH1-BAL (Channel 1 Balance) is applied to U420 pin 2 from the sample-and-hold circuit formed by U641B and C648 (diagram 5). This signal is a dc-offset level determined during the auto-calibration procedure. The offset value is stored as a calibration constant in nonvolatile memory and, like the other DAC System outputs, is updated approximately every 64 ms, holding the Preamplifier in a dc-balanced condition.

The voltage level of the CH1-PA-POS (Channel 1 Preamplifier Position) signal, from the circuit which includes U630A and U630B (diagram 6), vertically positions the channel 1 trace. When the CH1 VERT POS control on the Front Panel is turned, the Front Panel μP detects the change and reports it to the System μP. The System μP incorporates the change and causes subsequent DAC System updates to reflect the new value in the analog voltage level of the CH1-PA-POS signal.

A user may change the Channel 1 variable gain by pressing the CH1 VARIABLE button and pressing the appropriate menu choice buttons. The Front Panel μP detects these switch closures and reports them to the System μP. The System μP modifies the memory value that is sent to the DAC System to reflect the user-defined variable gain factor in the CH1-GAIN-CAL signal. The memory value that is modified is the calibrated value derived at the time of instrument self-calibration and stored in nonvolatile memory. Selecting the CAL menu choice, removes the variable gain modification and returns the calibrated gain setting.

A pickoff amplifier internal to U420 conditions the trigger signal and provides the proper signal level at pin 15 to drive the A/B Trigger Generator (U150, diagram 11). The pickoff point for the trigger signal is prior to the addition of the vertical-position offset, so the position of the signal on the crt has no effect on the trigger operation. However, the pickoff point is after the Preamplifier balance and variable gain have been added to the signal, so both of these functions affect trigger operation.

Common-mode signals are rejected from the trigger signal by the circuitry composed of operational amplifier U230B and associated components. The inverting input of U230B (pin 6) is connected to the common-mode point between +PICK (pin 12) and −PICK (pin 15) of U420. Any common-mode signals present are inverted and applied to a common-mode point between R133 and R235 to cancel the signals from the differential output. A filter network composed of LR421 and a built-in circuit board capacitor reduces trigger noise susceptibility.

The drain voltage for the input FET of the Preamplifier is provided by the circuit composed of VR420, R512, R515, and R516. Resistors R516 and R515 are part of the self-calibration circuitry and are used to match the gain of the CH1-BAL signal (pin 2) with that of the output of the attenuator.

Channel 2 Preamplifier

Operation of Channel 2 Preamplifier U320 is nearly identical to that of the Channel 1 Preamplifier just described. The exceptions are that the signal obtained from the pickoff reverse-termination return (pin 11) is used to drive the rear-panel CH 2 OUT connector and that the signal from the positive trigger pickoff (pin 12) is used to drive the Video Option Back-Porch Clamp circuit (diagram 21). The output of that clamp circuit is an offset signal, applied to the Channel 2 Preamplifier at pin 3, that is used to remove ac power-supply hum from the display of a video signal applied to the Channel 2 input when the Video option is in use.

The amplified Channel 2 +PRTR signal from U320 pin 11 provides an accurate representation of the Channel 2 signal at the rear-panel CH 2 OUT connector. The +PRTR pickoff signal is applied to the emitter of Q240B via a voltage divider formed by R234, R241, and R240. Transistor Q240B, configured as a diode, provides thermal compensation for the bias voltage of Q240A and reduces dc level shifts with varying temperature. Emitter-follower Q240A provides the drive and impedance matching to the CH 2 OUT connector and removes the diode drop added by Q240B. Clamp diodes CR140 and CR141 protect Q240A should a drive signal be accidentally applied to the CH 2 OUT connector.

External Trigger Preamplifier

The functions provided by External Trigger Preamplifier U100 are similar to those provided by the Channel 1 and Channel 2 Preamplifiers. The single-ended EXT TRIG 1 and EXT TRIG 2 input signals are buffered by U100 and routed to A/B Trigger Generator U150 (diagram 11) where they are available for selection as the trigger source for either the A or B trigger signal.

External trigger signal sensitivities may be set by the user to allow triggering ranges of either ±0.9 volts (EXT ÷ 1) or ±4.5 volts (EXT ÷ 5). Larger applied voltages on the external trigger inputs will exceed the control ranges of the Trigger System. The logic levels of control bits applied to U100 pin 30 (GA3) and pin 31 (GA4) from Source Select Control Register U140 (diagram 5) set the gain of the EXT 1 and EXT 2 Preamplifiers respectively.

Dc offsets in the output signal due to any tracking differences between the +5 V and the −5 V supply to U100 are reduced by the Tracking-Regulator circuit composed of U120, Q110, and associated components. Operational amplifier U120 and Q110 is configured so that the output voltage at the emitter of Q110 follows the −5 V supply applied to R210. This tracking arrangement ensures that the supply voltages are of equal magnitude to minimize dc offsets in the output signals.

PEAK DETECTORS AND CCD/CLOCK DRIVERS

The Peak Detectors and CCD/Clock Driver arrays (diagram 10) form what is essentially a very fast analog shift register. Waveform samples from each Preamplifier (U320 and U420, diagram 9) are loaded into the shift register array at a selected sample rate up to 10 ns per division and clocked out of the array at a slower fixed rate for digitization by the A/D Converter (diagram 15).

Peak Detectors U340 and U440 are hybrid devices having two modes of operation: "track" and "peak detect." For NORMAL and AVG (average) acquisition modes, the Peak Detectors track the input signal and provide signal gain from the Preamplifiers to the CCD arrays. In the peak detect mode used for ENVELOPE acquisitions, the Peak Detectors detect and hold the most positive and the most negative amplitude value of the input signal that occurs during each sampling interval. The peak values are amplified as in the NORMAL and AVG modes and applied to the input registers of the CCD arrays in such a manner as to produce a composite waveform of the most positive and most negative waveform amplitudes.

CCD/Clock Drivers U350 and U450 are hybrid devices containing a charge-coupled device (CCD) integrated circuit and a Clock Driver integrated circuit. The charge-coupled devices are very fast analog shift registers. Differential signal level applied to the inputs of the CCD from the Peak Detectors are sequentially clocked into the CCD registers at the processor-selected sample rate as determined by the SEC/DIV switch setting. Movement of the analog samples through the CCD arrays is controlled by the Clock Driver circuitry of the devices. Shifting the samples out of the CCD to be digitized in done with the combined clocking action of the internal Clock Drivers and the clock signals supplied externally to the CCD via Q450, Q460, Q550, Q551, and Q560. All control logic for the CCD/Clock Drivers, with the exception of the $\overline{\text{RESET}}$ signal from the System Clock circuitry (diagram 7), is derived from Phase Clock Array U470 (diagram 11).

Signal samples from both vertical channels are continuously loaded into and shifted through the CCD arrays until a trigger event occurs. The Time Base Controller (U670, diagram 8) then allows a specific number of further analog samples to be shifted into the arrays depending on the number of post-trigger samples needed to fill the waveform record. That number is determined by the TRIG POSITION setting for the acquisition. When the necessary samples have been loaded into the arrays, sampling is halted. The differential analog samples stored in the CCD arrays are then shifted out of the CCD to the CCD Output circuitry (diagram 14) where they are conditioned and multiplexed to the A/D Converter to be digitized.

Peak Detectors

The Peak Detectors provide peak detection, gain, and buffering of the CH 1 and CH 2 signals. Peak detect is enabled for ENVELOPE mode acquisitions only, but signal buffering is provided for all modes. Operation of both Peak Detectors is the same; therefore, the description is limited to the CH 1 circuitry. A simplified block diagram of the Peak Detector is shown in Figure 3-4.

Two user-selectable bandwidth limiters provide bandwidth reductions to either 20 MHz or 50 MHz for the signal through the Peak Detectors. With the Video Option installed, one of the 20 MHz limiter coils (L531 for CH 1) is adjustable to optimize the 20 MHz response for video signal operation. Without the option, both 20 MHz bandwidth limit coils for each Peak Detector are fixed values. Fifty megahertz bandwidth is adjusted by C431 for CH 1. The input stage of the Peak Detector is where bandwidth limiting is switched. Three bandwidth-select bits (FULL, BW50, and BW20) applied from the Peak Detector Control register (U530, diagram 5) control the bandwidth. Only one control bit at a time is set HI, and that bit controls the input amplifier bandwidth accordingly.

The differential signal from the CH 1 Preamplifier is applied to the CH 1 Peak Detector (U440) on input pins 4 and 6. In ENVELOPE acquisition mode, two sets of two fast-peak detectors following the input stage are used to permit continuous peak detection of negative and positive peaks of the input signal. While the PDA fast-peak detector is peak detecting the positive peak, the PDB peak detector is holding the last peak or resetting and vice versa (see table in Figure 3-4). Each of fast-peak detectors is followed by a slow-peak detector to increase the peak-hold time to the CCD input register. The outputs of the positive peak detectors are multiplexed to the differential OUT1 pins (pins 26 and 28) while the outputs of the negative peak detectors are multiplexed to the differential OUT3 pins (pins 33 and 35).

For NORMAL and AVERAGE acquisition modes, the Peak Detector operates in the track mode. To track the input signal and supply buffering only to the input signal, pin 21 ($\overline{\text{PD}}$) is set HI and pin 22 (SLOW/$\overline{\text{FAST}}$ is set LO, and the differential peak-detector clock signals (PD1 and PD2) are held at fixed levels (PD1 LO and PD2 HI). These control state levels set up one of the fast-peak detectors in the positive- and negative-peak detectors to follow the input signal in the track mode. The differential outputs at OUT1 and OUT3 follow the input signal at a signal level of 400 mV/division with a dc common-mode voltage of about 9 V. The CCD/Clock Driver SIG1 and SIG3 inputs are high impedance, so output loading of the Peak Detectors is provided by the Common-Mode Adjust circuits (discussed later).

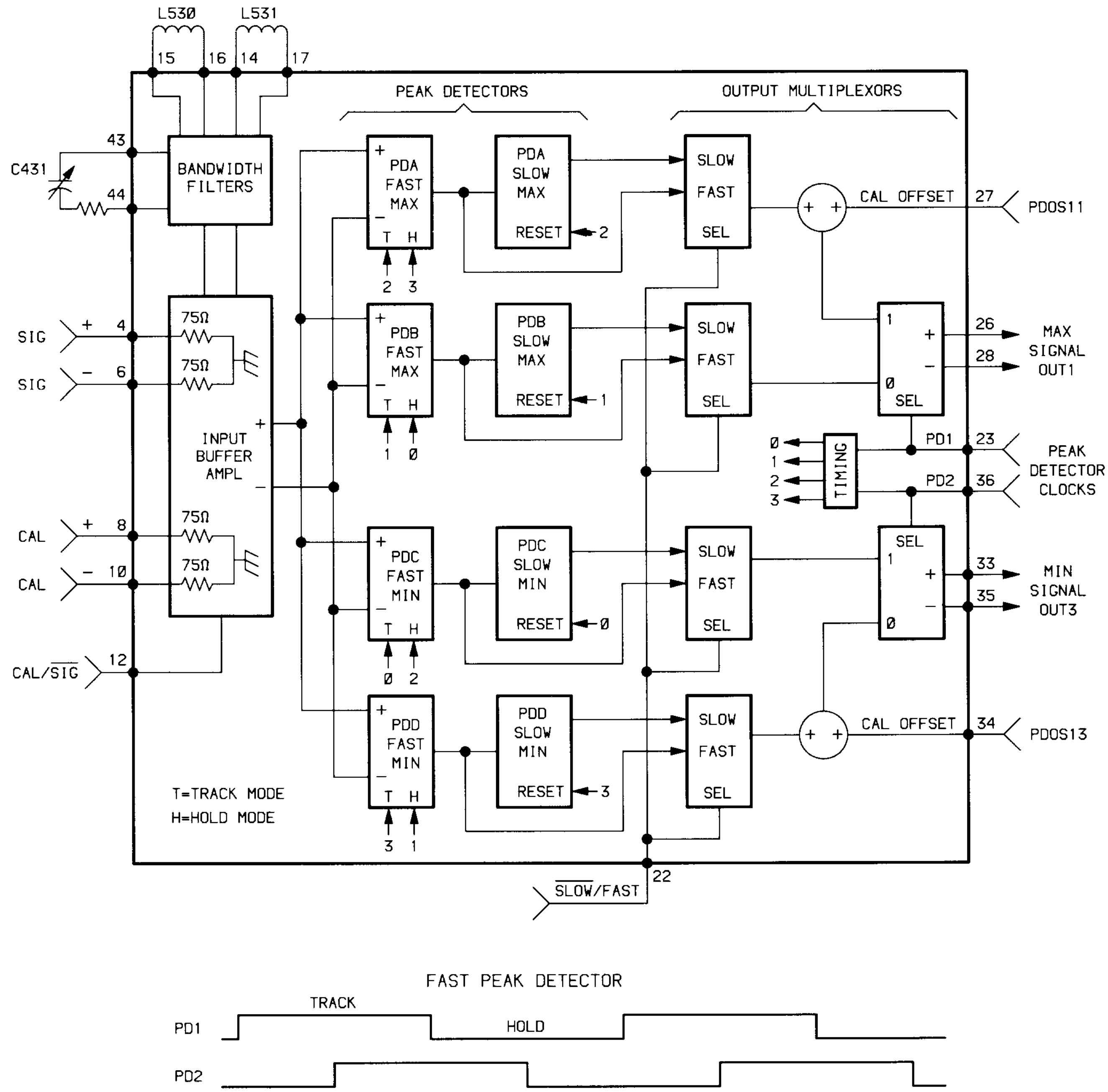
Peak detect mode for ENVELOPE acquisitions is turned on by setting $\overline{\text{PD}}$ LO at pin 21 and SLOW/$\overline{\text{FAST}}$ HI at pin 22 of Peak Detector U440. The differential ECL peak-detector clock signals (PD1 and PD2) toggle under control of the Phase Clock Array (U470, diagram 11) to control the internal peak detector switching and multiplexing of the positive and negative peaks to the OUT1 and OUT3 stages. The table in Figure 3-4 shows timing of the peak detector clocks and illustrates how alternate peaks are applied to the SIG1 and SIG3 inputs of the CCD.

DC offsets between the internal peak detectors of U440 are nulled out by voltage levels applied from the DAC System (diagram 6) to pins 27 and 34. Bias current for the input stage of U440 is set by R430 on pin 47, and output stage bias is set by R440 on pin 32.

The +CAL and −CAL inputs at pins 8 and 10 are identical to the signal inputs, but they are used only for the application of test signals during calibration or diagnostic testing. Selection of the inputs is controlled by the CAL/$\overline{\text{SIG}}$ signal. The test signals applied to pins 8 and 10 from the DAC System are used for testing and calibrating the Peak Detectors, the CCD/Clock Drivers, the CCD Output circuits, and the A/D Converter.

Common-Mode Adjust

The Common-Mode Adjust circuits (U540A and B, Q540, Q640, and associated components) allow varying, under control of the System μP, the common-mode voltage levels at the output of the CH 1 Peak Detector. (Similar circuitry performs the same task for the CH 2 Peak Detector.) Adjusting these dc levels changes the gain of the CCD and is done during self-calibration to control the overall gain of the Peak Detector-CCD subsystem. The CH 1—OUT1 Common-Mode Adjust circuit is described; the remaining Common-Mode Adjust circuits operate identically.



MAX	A	PD DISPLAY	HOLD DISPLAY	TRACK	PD	PD DISPLAY	HOLD DISPLAY	TRACK
MAX	B	TRACK	PD	PD DISPLAY	HOLD DISPLAY	TRACK	PD	PD DISPLAY
MIN	C	PD	PD DISPLAY	HOLD DISPLAY	TRACK	PD	PD DISPLAY	HOLD DISPLAY
MIN	D	HOLD DISPLAY	TRACK	PD	PD DISPLAY	HOLD DISPLAY	TRACK	PD

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Figure 3-4. Simplified Peak Detector block diagram.

The OUT1+ and OUT1− common voltage is level shifted and attenuated, then applied to U540A pin 3. Operational amplifier U540A compares the common-mode level with the attenuated CM11 level from the DAC System. The output of U540A drives Q640 to supply more or less current to the collector circuit thus raising or lowering the voltage on pin 25 of U440. Common-mode current is drawn by pins 26 and 28 via R540C and R450D to complete the feedback loop to the operational amplifier. Additional current is drawn by VCC1 (pin 25), part of which is supplied via R651 to reduce the stress on Q640. Emitter resistor R647 provides protection to Q640 against excessive current demand in the event of a short or overload. Resistors R647 and R651 also limit the voltage gain of Q640 to stabilize the feedback loop of the Common-Mode Adjust circuit.

Charge-Coupled Devices (CCD)

The CCD portion of the CCD/Clock Driver hybrid is a MOS-type integrated circuit that functions as a very fast analog shift register. A signal applied to the input is sampled by being converted to charge packets. These charge packets are then shifted through the CCD registers by MOS-circuit gating at intervals determined by the clock rates applied by the Clock Driver integrated circuit portion of the hybrid. The internal arrangement of the CCD analog shift registers and the total amount of storage space permits the input signal to be sampled at a high clock rate when necessary for the higher frequency signals. The charge packet samples are temporarily stored and then shifted out of the CCD at a much slower rate than the sampling rate. An inexpensive A/D Converter can be used to digitize the signal and slower memory circuits used to store the digitized samples. This type of operation is called Fast-In-Slow-Out (FISO) and is used at SEC/DIV settings of 50 μs and faster. At SEC/DIV settings of 100 μs and slower, the CCD runs with a constant clock rate of 500 kHz in a mode called Short Pipeline (discussed later).

A simplified diagram of one-half of one CCD is shown in Figure 3-5. The half shown, the SIG1 side or Side 1, is nearly identical to the SIG3 side (Side 3) of the CCD. Each side provides temporary storage of 528 analog samples for a total storage of 1056 samples of a single channel. The extra samples above that needed for the 1024-byte waveform record are needed for proper clock switching between the Fast-In and Slow-Out portions of the FISO cycle. The CCD has a Serial-Parallel-Serial (S-P-S) architecture. Each side has a 16 sample serial input "A" register, a 16 × 33 sample parallel storage "B" register, and a 16 sample serial output "C" register. Two such SPS sections are shown in Figure 3-5.

All the registers require four-phase gate clocking to move the sample charge packets through the CCD. Hence, there are four "A" register clocks, four "B" register clocks, and four "C" register clocks. There is also a Transfer In (TI) clock to shift samples from the serial A register into the B register and a Transfer Out (TO) clock to move them from the B register to the C register. The $\overline{\text{RESET}}$ clock discharges the output wells between output sample intervals so that charge does not accumulate at the input to the source-follower output amplifier. The S1 Sample clock samples the analog input signal at the side one inputs. Sampling occurs on the falling edge of S1, and the charge packet representing the instantaneous analog signal value is initially formed under the first "1A" gate (the first gate that is driven by the A register Phase 1 clock).

An extra input gate is added to Side 3, the other side of the CH 1 CCD array (not shown in Figure 3-5) to accept the Side 3 charge packets and permit their movement through the CCD to be synchronized with the Side 1 samples. The S3 Sample clock (opposite in polarity to the S1 Sample clock) performs the sampling function of the SIG3 signal. This sampling scheme doubles the effective sample rate of the CCD. Thus, the 100 megasample per second sampling rate is achieved with 50 MHz "A" register clocks. All register gates are driven with bipolar square-wave signals of +5 V to −5 V. The $\overline{\text{RESET}}$ clock signal also switches between +5 V and −5 V, but it is HI for only 200 ns of the total 2 μs period.

In FISO mode, 16 samples are shifted down the serial input A register at a clock period equal to 0.04 times the SEC/DIV setting. On every sixteenth clock cycle, the positive 2A clock pulse is replaced by a single positive pulse that moves all the charge packets into a transfer-in register at the head of the B register array. The A register is then empty and ready to accept new serial-in samples. The B register clocks run at 1/16 the speed of the A register clock rate so that the A register will be filled prior to each B register clock. In this way, the B register is filled with samples that are moved in parallel through the array. During this Fast-In portion of the input cycle, unneeded charges that arrive at the output C register due to the way that the input signal is continually sampled (until a trigger occurs) are emptied from the CCD through the output diffusion (OD1). When the Time Base Controller determines that the proper number of samples have been stored in the CCD after the trigger occurs, the mode changes to Slow-Out. The C register and RESET clocks then toggle at a constant 500 kHz rate to shift samples out of the CCD to be digitized.

The Short Pipe mode of the CCD is in effect at SEC/DIV settings of 100 μs and slower. The CCD is operated at a continuous 500 kHz rate. Samples are

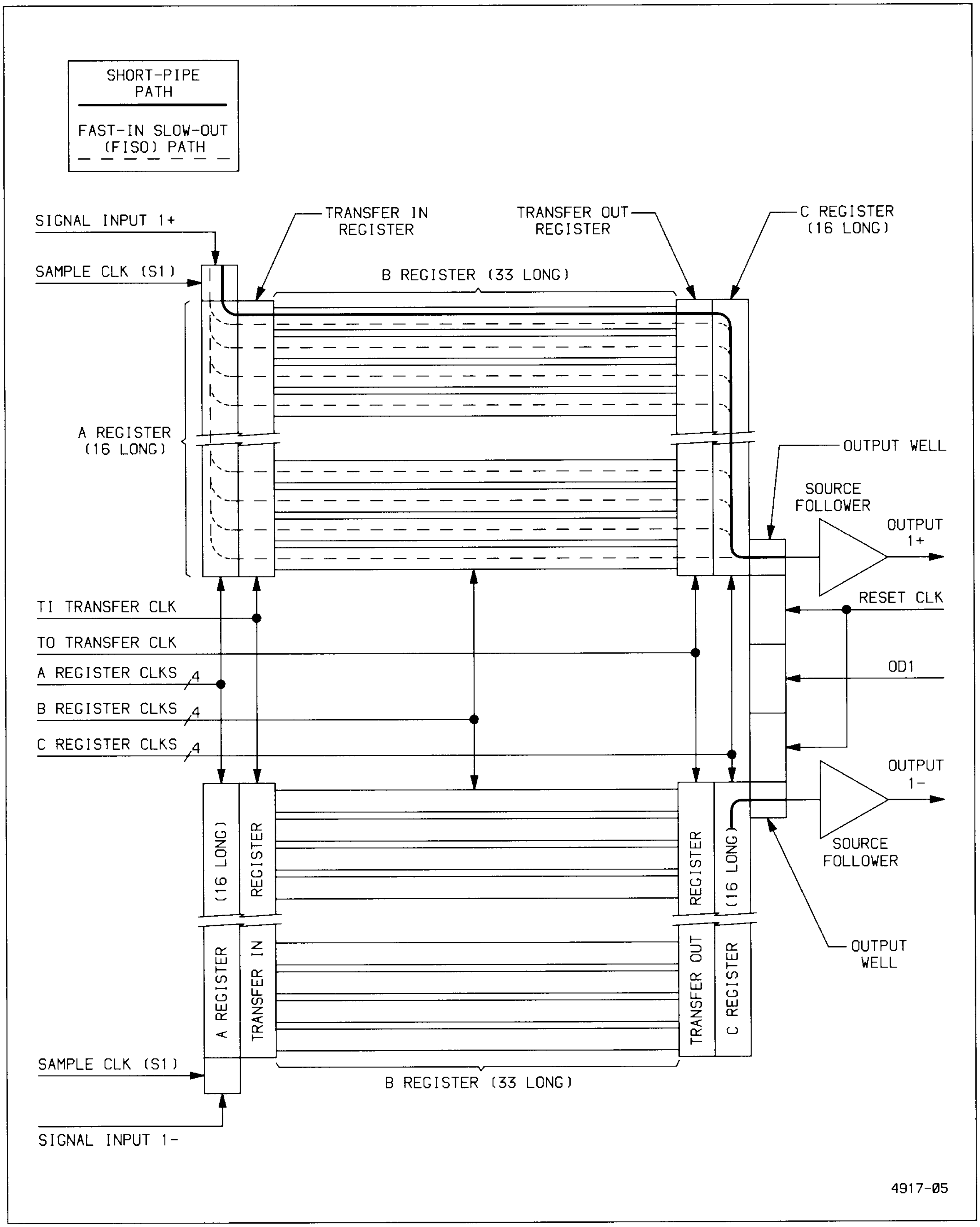

Figure 3-5. Simplified CCD architecture.

shifted serially through the CCD via one B register channel only. The TI clock toggles continuously to move the sample charge packets from the first A register position into the active B register channel, shown in Figure 3-5 as the Short-Pipe (slow-in, slow-out) path.

The output diffusions for sides 1 and 3 (OD1 and OD3) are independently driven from the DAC system. Varying the voltages on these nodes varies the gain of the CCD. These adjustments are used in conjunction with the Common-Mode Adjustments to calibrate the gains of the Peak Detector and CCD/Clock Driver subsystem. Gain increases with increasing OD voltage and decreasing Common-mode voltage; therefore, the calibration firmware moves these voltages in opposite directions to effect calibration.

Clock Drivers

The Clock Driver integrated circuits internal to the CCD/Clock Driver hybrids develop the four "A" register clocks, the four "B" register clocks, the two sample clocks, and the transfer input (TI) clock for the CCD. The high-speed Sample A Register and TI drivers are differential class A drivers through thick-film load resistors on the hybrid. The B Register drivers are slower with active pull-up and pull-down totem-pole outputs similar to conventional TTL driver outputs.

The 1A and 3A high-speed clocks are accessible at probe pins 21 and 20 of the hybrid devices. These pins (P1A and P3A) are isolated from the actual CCD gates by internal 875-ohm series resistors. Terminate the signals into 50 ohms to view them. Using the standard 10 MΩ probe will cause the signals to have a displayed rise time of about 30 ns; the actual rise time internally is about 2 ns.

Channel 1 CCD bias current for the high-speed drivers is set by the feedback circuit of U360A and Q375. The drivers are biased by injecting current into the IS input (pin 29). Increasing the current makes the LO level of the high-speed clocks more negative; decreasing the current raises the LO level. The HI level of the clocks is always within a few hundred millivolts of the +5 V supply to the hybrid. For controlling the negative clock level, the common-mode level of the 1A and 3A clocks at the P1A and P3A outputs is applied to the input of U360A. This level is compared to the midpoint between the +5 V and −5 V supplies. Operational amplifier U360A drives the base of Q375 to a level such that the current injected into IS sets the common-mode level of P1A and P3A equal to the voltage at pin 3 of U360A (the voltage supply midpoint value). Since the HI clock levels at P1A and P3A are approximately at the +5 V supply level, the LO levels of the clocks then are set to approximately the −5 V supply level. Bias stability is thereby maintained over temperature and component variations.

Each Clock Driver integrated circuit has only two B register drivers. Therefore, the B register drive task is shared between the two CCD/Clock Driver hybrids. The Clock Drivers in U450 drive the 1B and 3B gates of both CCD arrays, and the ones in U350 drive the 2B and 4B gates of both CCD arrays (see diagram 10). The Transfer Out (TO) gate timing has to match the 4B gate timing; therefore, the TO gate inputs of each CCD are tied to the 4B gate signal through R345.

Since the B register drivers have totem-pole outputs with emitter-followers for pull-ups, their HI state outputs are reduced from the +5 V supply by approximately 1 V. Resistors R466, R465, R366, and R365 reduce the transient current flow into the B register gates when the B drivers change state.

Resistor array R470 provides proper termination for the ECL logic inputs to the CH 1 Clock Drivers.

"C" CLOCK DRIVERS. These are external clock drivers consisting of Q450, Q550, Q460, Q560, and associated components. They provide the necessary −5 V to +5 V clock swings for the CCD "C" register gates. Each driver is simply an inverting buffer which accepts TTL inputs from the Phase Clock Array. During the Fast-In portion of the FISO acquisition cycle, the outputs of all four drivers are held HI by the Phase Clock Array. During the Slow-Out portion of the cycle, and at SEC/DIV settings of 100 μs and slower, the C Clock Drivers toggle at a 500 kHz rate in the normal four-phase sequence.

RESET DRIVER. This driver consisting of Q551 is identical to the C Clock Driver states. It takes the $\overline{\text{RESET}}$ signal input from U731C in the System Clocks circuitry (diagram 7). Like the C Clock Drivers, the Reset driver is driven HI during Fast-in and toggles at other times. The Reset driver output is held HI for only 200 ns of the 2 μs clock period.

−2 V Regulator

A −2 V supply needed to terminate all of the high-speed ECL signals on the Main circuit board is formed by U580B and Q580. The circuit is a simple series-pass regulator with R585 and R586 developing the −2 V reference for operational amplifier U580B from the −5 V supply. Feedback is through R587. Collector load resistors R486, R487, and R488 limit the power dissipation of Q580 and protect it from possible short circuits of the −2 V supply.

TRIGGERS AND PHASE CLOCKS

In the 2430, the acquisition system continuously acquires input samples. When the user-specified number of "pretrigger" samples have been moved into the CCD arrays, the trigger system is allowed to recognize trigger events. Sampling of the signal input to the CCD arrays continues (with new samples pushing out old samples) until a trigger occurs. After the trigger, the number of "post-trigger" samples needed to fill the waveform record are moved into the CCD arrays and sampling is stopped. The acquired samples are then moved out of the CCD arrays, digitized, stored to memory, and displayed. The acquisition system then begins again to fill the "pretrigger window" for the next acquisition; and, when that has been done, the trigger system is enabled to look for the next trigger event.

The Trigger circuits (diagram 11) detect when the user-defined triggering conditions are met and then allow the acquisition to be completed. When the triggering signal limits defined by the user for slope, level, and variable holdoff are detected by A/B Trigger Generator U150, the resulting trigger output is applied to Trigger Logic Array U370, where triggering conditions of delay mode, delay time or delay events count, and optional trigger sources are taken into consideration. The Trigger Logic Array outputs several trigger-recognition and acquisition-control signals that cause the acquisition system to finish the "post-trigger" portion of the acquisition.

The Phase Locked Loop and CCD Phase Clock circuits (diagram 11) control sampling and shifting operations of the CCD/Clock Driver hybrid. The Phase Locked Loop synthesizes the 200/250 MHz sample clock driving the CCD Phase Clock Array. The CCD Phase Clock Array uses this "master" clock to generate other CCD clocks in accordance with mode data written to it from the System μP.

A/B Trigger Generator

The A/B Trigger Generator circuit, composed of U150 and associated components, provides for selection and analog-type trigger detection from five input signals for each of the A and B triggers. These are the CH 1 and CH 2 vertical inputs, the EXT 1 and EXT 2 trigger inputs, and the line-trigger input (A trigger only). Two multiplexers internal to U150 select one of these signals as the trigger source for A Trigger and one (excluding the LINE signal) for B Trigger. Source selection depends on the states of the $\overline{\text{SR0A}}$, $\overline{\text{SR1A}}$, and $\overline{\text{SR2A}}$ (source select—A trigger) lines for the A Trigger and on $\overline{\text{SR0B}}$, $\overline{\text{SR1B}}$, and $\overline{\text{SR2B}}$ for B Trigger. The appropriate select bits are written into register U140 by the System μP whenever the operator makes a triggering condition change using the trigger source menus.

Control data from the System μP defining trigger mode, trigger coupling, and trigger slope are clocked serially (one bit at a time) from the CD (control data) line into two storage registers internal to U150. Clocking the $\overline{\text{CCA}}$ (control clock A) line moves the setup data to the A control register, while clocking $\overline{\text{CCB}}$ moves data to the B control register. When the control data has been loaded, each trigger circuit begins comparing its selected input signal to the user-defined trigger level for that trigger channel.

When the defined triggering criteria are met for either A or B, the associated trigger outputs (ATG, $\overline{\text{ATG}}$ for A Trigger; BTG, $\overline{\text{BTG}}$ for B Trigger) will go to their asserted (true) states. The exception is when the A Trigger holdoff has not finished (ATHO is still HI). When the holdoff ends, however, the next trigger event on the selected A Trigger input will assert the A Trigger output gates.

Each differential trigger gate is inverted and current buffered by a pair of differential transistors that allow quick response to the trigger edges by Trigger Logic Array U370.

Trigger Logic

The Trigger Logic circuit consists primarily of Trigger Logic Array U370. The Trigger Logic Array provides final trigger-source selection; trigger-point delays, delayed either by a specified amount of time or by a specified number of events; and ramp-control signals to the Jitter-Correction circuitry for resolving trigger-point ambiguities. The Trigger Logic Array also produces the trigger and external clock signals necessary to control operations of the CCD Phase Clock circuit.

The three enable inputs to U370, E1B (A3), E2B ($\overline{\text{WR}}$), and E3B ($\overline{\text{ACQSEL}}$), are all set LO whenever writing to addresses between 6080h and 6087h to enable the address inputs (A0, A1, and A2). The choice of eight addresses between 6080h and 6087h provides for different operating requirements of the Trigger Logic Array.

Depending on the address written to, one of the following actions may occur:

Mode control data may be loaded into the internal mode register.

The internal events and delay counter low-byte or high-byte of the number of events to be counted or delay may be loaded.

Various strobes used for internal control of the Trigger Logic Array may be generated.

Table 3-5 shows the action taken for each address selected.

Table 3-5

Trigger Logic Array Addresses (6080h-6087h)

Address Bits			Circuit Operation Initiated
A2	A1	A0	
0	0	0	Restart Acquisition
0	0	1	Force Manual Trigger
0	1	0	Load Mode Control Data from M0-M7
0	1	1	Latch Delay Counter Low-Byte from M0-M7
1	0	0	Latch Delay Counter High-Byte from M0-M7
1	0	1	Load Delay Counter from Delay Latches
1	1	0	Not Used
1	1	1	Reset All Latches

As previously mentioned, U370 provides final trigger-mode and source selection, dependent on data written from the System μP to a control register within U370 at address 6082h. The mode control data byte loaded from the M0-M7 input bus is built by the System μP and applied to the M0-M7 (mode) inputs from serial-input register U270 (diagram 5) via the GAD0-GAD7 bus lines. The data byte defines the A Trigger source, B Trigger source, Record Trigger source, Jitter Trigger source, and whether a single event or multiple events are needed to produce a trigger. Bit definition is shown in Figure 3-6.

After the control data byte is loaded and the acquisition is restarted, Trigger Logic Array U370 waits for EPTHO (end of pretrigger holdoff) to go HI at pin 28, indicating that the acquisition system has sampled the "pretrigger" points and is ready to complete the acquisition. With EPTHO set HI, the trigger logic begins watching the trigger source (as defined by the control data byte), waiting for a trigger event to occur.

Operation of the Trigger Logic Array is very sequential in the way it functions in the various trigger modes. An example is illustrated in the sequence of events for B RUNS AFTER trigger mode.

1. The System μP loads the "delay count" and "control mode" registers, then starts the acquisition (indicated by setting RSTACQ HI at TP370).

2. The Trigger Logic Array watches for EPTHO at pin 28 to go HI; signaling that the defined number of pretrigger points have been sampled.

3. With EPTHO HI, the Trigger Logic Array watches MTG and $\overline{\text{MTG}}$ (main trigger gate) for an A trigger event to start the delay counter. When a trigger occurs, JTRIG (jitter trigger) is generated, starting the jitter-correction circuits (via the RAMP and $\overline{\text{RAMP}}$ signals).

4. The defined delay count is decremented to zero by the DELCLK (delay clock) signal on pin 67 from Phase Clock Array U470. If the mode were A Delayed by B Events, the B Trigger events would be used to decrement the delay counter.

5. In this example, when the internal Delay count reaches 0, a RTRIG (record trigger) is generated for B RUNS AFTER. RTRIG is the "record trigger" point on the displayed waveform. If the mode were B TRIG AFTER, the Trigger Logic Array would begin watching for a B Trigger to occur on the DTG and $\overline{\text{DTG}}$ input pins (Delay Trigger Gate).

6. Time Base Controller U670 (diagram 8) counts the post-trigger samples as they are acquired. When the required count is reached to complete the acquisition, it resets EPTHO to LO and further triggers from the Trigger Logic Array are prevented from being generated.

The Time Base Controller then starts moving digitized samples to the Acquisition Memory and, when finished, tells the System μP that the acquisition is done. The System μP may then restart the whole process again for the next acquisition by writing appropriate data to the various trigger registers.

In external clock mode, the differential EXTCK and $\overline{\text{EXTCK}}$ (external clock) signals to the Phase Clock circuit replace the normal master-clock ($\overline{\text{MCLK}}$) signal and allows the B trigger events to be used as the events delay source.

CONTROL DATA BYTE

M7	M6	M5	M4	M3	M2	M1	MØ
JT1	JTØ	RT1	RTØ	ONEVNT	BTØ	AT1	ATØ

JITTER TRIGGER BITS

JT1	JTØ	SOURCE
Ø	Ø	A TRIGGER
Ø	1	B TRIGGER
1	Ø	END EVENTS
1	1	B TRIGGER

RECORD TRIGGER BITS

RT1	RTØ	SOURCE
Ø	Ø	A TRIGGER
Ø	1	END DELAY TIME
1	Ø	END DELAY EVENTS
1	1	B TRIGGER

ONE EVENT BITS

ONEVNT	EVENTS=1
Ø	NO
1	YES

B TRIGGER BIT

BTØ	SOURCE
Ø	DELAYED INST. TRIGGER
1	WORD TRIGGER OPTION

A TRIGGER BITS

AT1	ATØ	SOURCE
Ø	Ø	MAIN INST. TRIGGER
Ø	1	VIDEO TRIGGER OPTION
1	Ø	WORD TRIGGER OPTION
1	1	A*B TRIGGER

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Figure 3-6. Trigger Logic Array Control Data Byte.

The $\overline{\text{A TRIG}}$ and $\overline{\text{R TRIG}}$ outputs from Q287 and Q288 are TTL-buffered versions of the corresponding trigger signals and are routed to rear-panel BNC connectors.

Phase Locked Loop

The Phase Locked Loop circuit synthesizes the 200/250 MHz clock used by the Acquisition System. It consists of Phase/Frequency comparator U381 amplifier U580A, a voltage-tuned tank circuit, and a divide-by-50 counter internal to Phase Clock Array U470. The tank-circuit resonant frequency is set by the value of voltage-controlled capacitor CR580. The resulting clock is divided by 50 by the counter and is applied to the phase-frequency detector U381 on the FIV4 line. The FIV4 signal is compared to the reference clock REF4/5, and any phase or frequency error appears at the output of U381 as variable width pulses. These pulses are integrated by U580A to produce a dc voltage that represents the phase difference (fast or slow) and magnitude of error between the REF4/5 clock and the divided down master clock. This is the frequency-control voltage and varies the capacitance of varactor diode CR580, part of the tank circuit formed by the circuit board delay line and CR580. The tank is tuned by the control voltage so that the master clock frequency is precisely 50 times the reference frequency. Depending on the user-defined sweep rate and acquisition mode, the reference (REF4/5) will be either 4 MHz or 5 MHz, resulting in a 200 MHz or 250 MHz master clock (see Table 3-6).

Table 3-6

REF4/5 Frequency for Each SEC/DIV Setting

SEC/DIV Setting	REF4/5 Frequency	Phase Clock Array Clock Frequency
EXT CLK	Don't Care	EXT CLK
500 ns	4 MHz	200 MHz
1 μs	4 MHz	200 MHz
2 μs	5 MHz	250 MHz
5 μs	4 MHz	200 MHz
10 μs	5 MHz	250 MHz
20 μs	5 MHz	250 MHz
50 μs	Don't Care	1 MHz
100 μs	Don't Care	1 MHz

CCD Phase Clock

The CCD Phase Clock generates properly phased and frequency-related clocks that control most of the Acquisition system. These functions include moving samples into the CCD arrays, shifting within the arrays, jitter-correction control, peak-detection control, and trigger-delay clock generation. These clocks are derived from the 200/250 MHz master clock generated by the internal oscillator and the Phase Locked Loop circuit.

Two operating modes exist for the CCD arrays; FISO (fast-in, slow-out) and Short-Pipe. The Phase Clock circuit is set up to generate proper clocking signals for either mode by loading data into Gate Array Control Register U270 (diagram 5). This data is applied to U470 on the CC0-CC3 (chip control 0-3) lines and on the PD_{OFF} (peak detector off) line. The PD_{OFF} line enables/disables the peak-detector output lines (PD1, $\overline{\text{PD1}}$, PD2, and $\overline{\text{PD2}}$) and thus peak detection mode (see that description). The CC0-CC3 inputs control operating mode and clock selection as shown in Table 3-7.

FISO MODE. As explained in the CCD description, each CCD is made up of two identical differential channels using a serial-parallel-serial (SPS) structure. Samples are moved into and shifted within the CCD arrays using properly phased, overlapping clocks. Figure 3-5 shows a basic CCD structure (see CCD description, diagram 10).

Depending on whether the Side 1 channel or Side 3 channel is being acquired, the corresponding sample gate (SAM1 or SAM3) will go HI. This moves the present level of the input signal into the input well of the CCD arrays. Before the sample gate returns LO, the ϕ1A (phase 1-A register) clock goes HI and the charge is shared by the adjacent cells (input and ϕ1). When the sample gate returns LO, all charge moves to the ϕ1 cell. The ϕ2A clock then goes HI and charge is distributed into both the ϕ1 and ϕ2 cells. When ϕ1 returns LO, all charge will move into the ϕ2 cell. Similar shifts occur using the ϕ3A and ϕ4A clocks until ϕ1 occurs again, completing the cycle.

When 16 samples have been acquired in the A register, the TI (transfer into B) clock moves all 16 samples from the ϕ1A cells in parallel into the B register. The four phases of the B clocks shift samples down the 16 parallel B registers in a manner similar to that just described for the A register but at 1/16th the rate. The $\overline{\text{TTL1B}}$ clock (TTL-version of B clock ϕ1) is output to the Time Base Controller and allows it to keep track of how many samples have been acquired (in multiples of 32). This allows the Time Base Controller to know when the proper number of "pretrigger" points have been acquired and when to enable the Trigger Logic Array.

Table 3-7

Phase Clock Array Control Lines (CC3 through CC0)

SEC/DIV Setting	Control Bits				Mode
	CC3	CC2	CC1	CC0	
EXT CLK	0	0	0	0	
500 ns	0	1	0	0	FISO
1 μs	0	1	1	0	FISO
2 μs	1	0	0	0	FISO
5 μs	1	0	1	0	FISO
10 μs	1	1	0	0	FISO
20 μs	1	1	1	0	FISO
50 μs	x	x	0	1	FISO (Short-Pipe)
100 μs and slower	x	x	1	1	Short-Pipe

Once enabled, the Trigger Logic Array begins counting its predefined delay while samples continue to be acquired. The DELCLK (delay clock) output to the Trigger Logic runs at one-half the sample-clock rate, allowing the Trigger Logic to complete any defined delay. When delay is done, the JTRIG and RTRIG signals may be generated. When the JTRIG occurs, the RAMP and $\overline{\text{RAMP}}$ signals from the Trigger Logic start the Jitter-Correction Ramps. The JTRIG signal to U470 causes the TL0 (trigger location-bit 0) bit to latch the phase (HI or LO) of the master clock, defining which half of the cycle the trigger event occurred. The internal slow-ramp logic circuitry of U470 becomes enabled and, on the next two edges of the master clock, asserts the two pairs of slow-ramp (SLRMP) outputs. These outputs reverse the charge direction of the Jitter-Correction Ramp circuits (diagram 12) and start the Jitter-Correction Counters (diagram 13) on opposite edges of the master clock. See those descriptions for further information on trigger-jitter correction.

Depending on trigger mode, the RTRIG (record trigger) line will be asserted some time after JTRIG occurs. RTRIG is synchronized to the B-register clock and is output to the Time Base Controller on the SYNTRIG (synchronous trigger) line, telling it to start counting post-trigger samples. The RTRIG also loads a register internal to U470 with the present sample count to locate the trigger event (explained later). When the Time Base Controller has completed the post-trigger count, it will set SO (slow out) HI, switching the Phase Clock Array mode from "Fast In" to "Slow Out" mode. The various phase clocks are now derived from the 1 MHz 2XPC clock (from the Time Base Controller) instead of the 200/250 MHz master clock, and samples are shifted out of the CCD arrays at the A/D conversion rate.

Outputs TL0-TL4 (trigger location bits 0 through 4) define the trigger location within ±1/2 of a sample interval and allow the extra samples taken at the beginning and end of the CCD sample array contents to be discarded. Defining and discarding these samples is done because the trigger event may occur at any of 32 locations within the two A registers. Outputs TL1-TL4 locate the trigger at one of these 32 sample positions, allowing samples before the start of the waveform to be discarded. Output TL0 defines trigger position within the sample interval to either half of the interval (phase 1 side or phase 3 side) by sampling the phase of the master clock when the trigger occurred.

SHORT-PIPE MODE. A second acquisition mode, Short-Pipe mode, is used at SEC/DIV settings 100 μs/div and slower. In Short-Pipe mode, the ϕ2A clock that transfers samples down the input (A) register is disabled; and instead, the TI (transfer into B array) clock shifts samples straight down the first register of the B array to the output well. Sampling occurs at 1 MHz in Short-Pipe mode (500 kHz each side of the CCD array) as the various phase clocks are derived from the 2XPC clock. Trigger delays are generated at the SDC (slow-delay clock) rate since Short-Pipe mode connects the DELCLK output to the SDC input. Since sampling is occurring at a 1 MHz rate and the SEC/DIV is set so that a sample rate slower than this is required, some of the samples must be discarded. The discrepancy is resolved by Time Base Controller by counting and discarding the proper number of samples between those it allows to be saved. This allows effective sample rates much lower than the actual 1 MHz rate and, by routing the SDC signal to DELCLK, allows the trigger delays to be counted in terms of effective sample events.

In FISO mode, the $\overline{\text{TTL1B}}$ (TTL-level phase 1B) signal runs at 1/16 of the A-register clock rate and is used by the Time Base Controller to keep track of how many FISO samples have been taken. Each $\overline{\text{TTL1B}}$ clock indicates that 16 sample intervals have occurred. In Short-Pipe mode, the $\overline{\text{TTL1B}}$ clock runs at the A-register clock rate. By using the $\overline{\text{TTL1B}}$ count and the TL0-TL4 data, the Time Base Controller (U670, diagram 8) can precisely determine when the acquisition is finished.

TTL4C is a TTL version of the phase 4 clock for the C (output) register and runs at all times except during RESET. This is one of the signals required by the System Clock Generators for producing correctly timed Output Sample Clocks to the CCD Output circuitry (diagram 14) and the $\overline{\text{RESET}}$ clock to the CCD arrays.

JITTER CORRECTION RAMPS

The Jitter Correction Ramps located on diagram 12 are a portion of two dual-ramp timing circuits used to detect and measure the time difference between a trigger event and the sample clock. This information is needed when doing acquisitions at SEC/DIV settings greater that 500 ns to correctly place the data points obtained on different trigger events. The Jitter Correction Counters are located on diagram 13.

Jitter Correction Ramps

Operation of the RAMP1 and RAMP2 circuits is identical; therefore, only the RAMP1 Jitter Correction circuit will be described. Both Jitter Correction Ramps are initiated by the same trigger event, but they are switched to their slow-discharge mode on opposite edges of the sample clock. By switching on opposite edges, the trigger point has two distinct references which define the trigger point, allowing the System μP to detect and correct for metastable states of the trigger recognition logic.

The ramp generator consists of a constant current source used to rapidly charge an integration capacitor when the trigger event occurs and a second current source used to discharge the capacitor (more slowly) after the proper edge of the sample clock occurs. The fast-charge time is the actual time from the trigger event to the appropriate sample-clock edge. The time it takes the slow-discharge mode to discharge C491 gives a numerical representation (counted) of how high the ramp level reached when C491 was fast charging; and therefore, the time of the fast ramp.

Fast charging rate is determined by the constant current source formed by U590A, Q493, and associated components. The charging current is nominally 20 milliamperes through R590 and Q493. The voltage drop across R590 balances the +7.5 volt reference at pin 2 of U590A and keeps Q493 turned on just enough to maintain the balance at the operational amplifier inputs.

This charge current is switched through either Q491 or Q492, depending on whether the ramp should be ramping down slowly or ramping up quickly. When waiting for a trigger to occur, the SLRMP1 (slow-ramp 1) will be LO, turning Q491 on. Charging current from Q491, which would normally charge integration capacitor C491 (and the 50 pF circuit-board capacitor), is shunted to −5 volts by Q490, which is turned on by a HI $\overline{\text{RAMP}}$ (fast ramp) signal applied to its base.

RAMP CLAMPING. The clamping circuit made up of U590B, CR490, and associated components, holds the ramp summing-node voltage (collector of Q490) at zero volts while the circuit is waiting for a trigger to occur (signaled when RAMP and $\overline{\text{RAMP}}$ go to their true states). The summing-node voltage is applied to U590B on pin 6 where it is compared to the zero-volt clamp level (ground) on pin 5. When the summing node attempts to go below ground while Q490 is on, U590B will conduct more to maintain the balance at the input pins, thereby clamping the summing node at zero volts via R592 and CR490.

Transistor Q380 and its associated components clamp the positive peaks of both ramps at +3.2 volts via CR491. This clamping takes place at SEC/DIV settings slower than 500 ns/div because the SLRMP signal doesn't occur soon enough after the RAMP signal starts the ramp to reverse the ramp slope before the +3.2 V level is reached.

RAMP SWITCHING. When Trigger Logic Array U370 (diagram 11) detects that a trigger event has occurred, it sets the RAMP and $\overline{\text{RAMP}}$ signals to their active (true) states. The LO $\overline{\text{RAMP}}$ signal turns Q490 off to allow the integration capacitor to begin a fast charge, and the HI RAMP signal turns Q392 on to reverse bias CR490 and remove the clamp circuit from the summing node.

The charging current now linearly charges C491 and the circuit board capacitance positive (holding STOP1 LO through U490) until the proper edge of the next sample clock occurs (see Figure 3-7). This switches the SLRMP1 and $\overline{\text{SLRMP1}}$ signals to their true states, turning off Q491 and turning Q492 on.

With Q492 on, the charging current is routed through R497, producing a HI START1 signal and enabling the RAMP1 Jitter Correction Counter circuit (diagram 13).

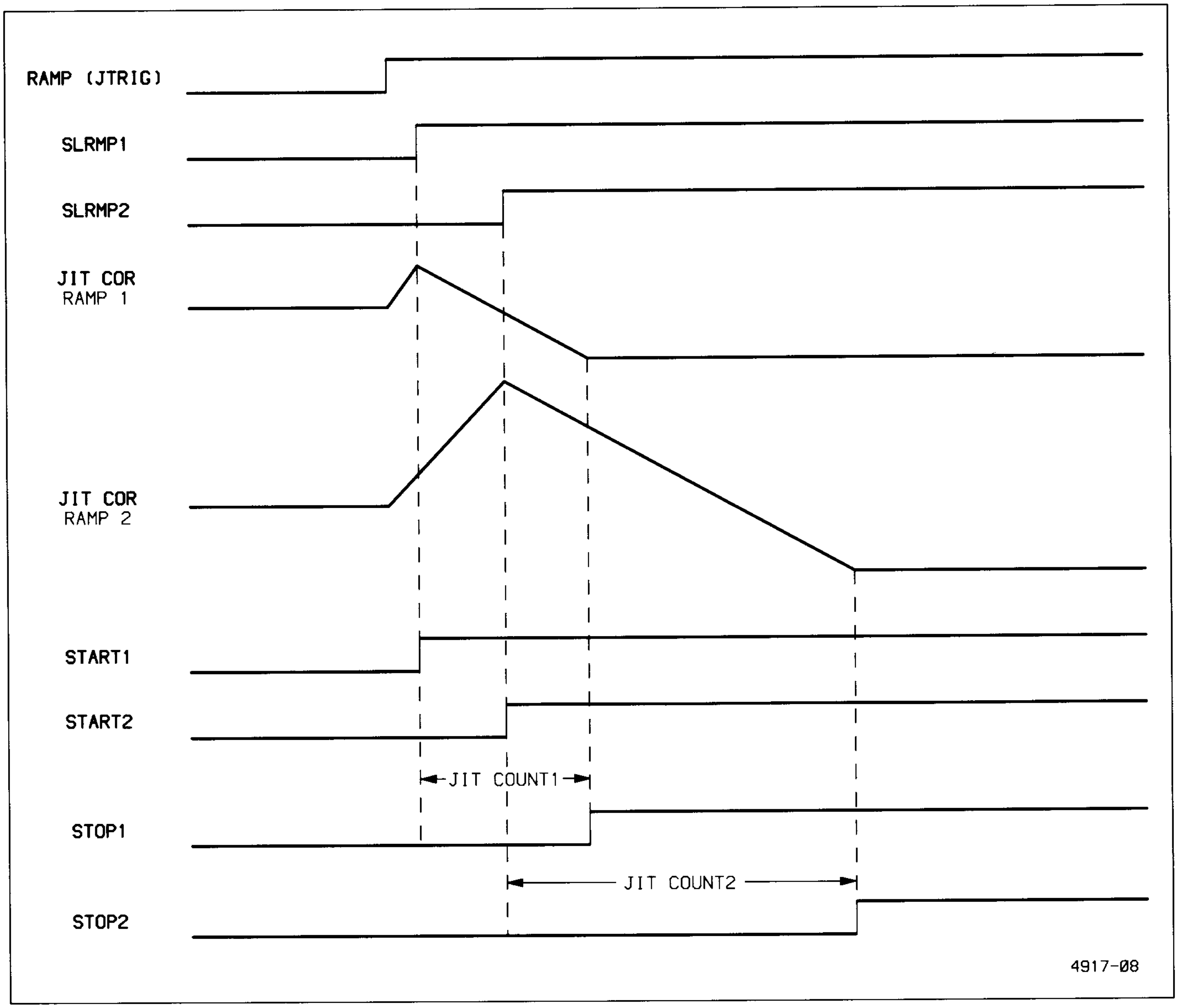


Figure 3-7. Jitter correction waveforms.

Since Q491 is now off, C491 begins the slow-ramp discharge through Q495 and R493. When the voltage held on C491 crosses the switching threshold of U490, STOP1 is switched HI to turn off RAMP1 Jitter Correction Counter at the proper count.

At the time of calibration, the JIT1 GAIN (jitter gain—ramp 1) value is set to the base of the discharge current source transistor, Q495, so that the ratio between charging rate and discharging rate is 1250:1 (approximately 20 mA from the charging current source to approximately 16 μA discharge current from Q495). The slow discharge time of C491 allows the RAMP1 Jitter Correction Counter to convert the peak amplitude of RAMP1 (dependent on the time that C491 was allowed to fast charge) into a count relating trigger-event position to the sample-clock edge.

After the Jitter Counter has been read, the RAMP, $\overline{\text{RAMP}}$, SLRMP1, and $\overline{\text{SLRMP1}}$ signals will be reset to their inactive states. This again clamps the summing-node voltage at zero volts and reapplies the charging current to the node in preparation for the next trigger event.

RAMP2. As mentioned earlier, the RAMP2 Jitter Correction circuit is running simultaneously, referenced to the opposite edge of the sample clock. The RAMP2 Jitter Correction Counter produces a count defining the trigger point relative to the opposite edge of the sample clock. Since both ramps have a possibility of an error in their slow-ramp starting times (due to metastable switching of the SLRMP1 and SLRMP2 signals) there will always be a chance of error present in the trigger-position count. The count from both ramps is checked, and the value closest to the nominal midrange count will be used by the System μP when placing the repetitively sampled data points. If both counts are in error, that acquisition is discarded.

TRIGGER HOLDOFF, JITTER COUNTERS, AND CALIBRATOR

Circuitry shown in diagram 13 performs a variety of functions.

The Trigger Holdoff circuits allow a delay to occur between the occurrence of a triggering event and when the A/B Trigger Generator is allowed to recognize another trigger event. Variable Holdoff can help the user prevent double triggering on aperiodic signals (such as complex digital words).

The RAMP1 and RAMP2 Jitter Correction Counters measure the time difference between the asynchronous trigger event and the actual sampling point of the waveform data. That information is needed by the System μP to place the random samples taken in REPET acquisition mode correctly with respect to data points taken in the previous acquisitions to fill the waveform record.

The Calibrator circuit generates a square-wave output having precise amplitude and frequency characteristics. The CALIBRATOR signal provided at the front-panel connector is useful for adjusting probe compensation and verifying VOLTS/DIV and SEC/DIV calibration.

The Side Board Address Decoder included in the circuitry is used by the System μP to enable the appropriate register or buffer on the Side board to read the Jitter Correction Counters, select the Holdoff Time, and communicate with the Front Panel μP.

Trigger Holdoff

The Trigger Holdoff circuit consists of a trigger-enabled, constant current source (actually one of three selectable sources added to a small permanent source) used to linearly charge a capacitor (one-of-two selectable cap values). The resulting integrator output is a linear ramp whose slope depends on the current-source and integration-capacitor selection. The ramp is applied to the Holdoff Comparator where it is compared to the user-definable (front-panel pot) holdoff-reference level. When the charging ramp crosses that level, the ramp rapidly discharges (resets) and ends the holdoff condition.

Holdoff Select

The Holdoff Select circuit, under System μP control, determines which of the Holdoff Current Sources and which of the integration capacitors will be used to produce the holdoff ramp. Its outputs are set by the microprocessor by writing data into Holdoff Register U762, residing at address 620Ch. Output bits HO0 through HO2 (holdoff control bits 0-2) enable their corresponding current-source transistor when HI. Bit HO3 is used for selection of the integration capacitor. The $\overline{\text{FPRESET}}$ bit allows the system processor to reset the Front Panel μP (diagram 3).

Buffer U761, residing at read location 602Ch, allows the System μP to check the holdoff circuit setup and to monitor the status of the A Trigger (ATG) and trigger holdoff (ATHO) bits.

Holdoff Current Sources

The Holdoff Current Sources provide the constant currents used to charge the integration capacitors (producing a linear ramp). The circuit consists of four transistor current sources, three of which may be turned on or off under control of the Holdoff Select circuit.

The bases of the four current-source transistors, Q761, Q771, Q772, and Q773, are held one diode-drop below +5 volts by CR772 and R773. This results in precisely +5 volts being present on the emitter of any conducting current-source transistor. The amount of current is set by the value of emitter resistor(s). Transistor Q773 will always be on while the other three current-source transistors can be turned on or off by the HO control bit via the the associated emitter diodes. A LO at the cathode of one of these diodes will disable the associated current source by reverse biasing the transistor junction; a HI at the cathode of a diode enables the charging-current source via the associated emitter resistor.

Charging Capacitor Selection

The Charging Capacitor Selection circuit composed of Q783, Q782, and associated components, selects the integrating capacitance. The magnitude of the charging current from the selected current source, in combination with the capacitance value, of the integration capacitor, determines charge rate (slope) of the holdoff ramp; and thereby, the holdoff time. Table 3-8 illustrates the holdoff time as a function of the selected current source and charging capacitor.

Charging current is stored on capacitor C882 when holdoff intervals less than or equal to 10 μs are desired. For longer holdoff periods, capacitor C881 and C885 are placed in parallel with C882 by turning Q782 on. Transistor Q782 turns on when HO3 (holdoff select 3) is LO, turning Q783 off. This pulls the gate of Q782 high and turns it on, placing the parallel combination of C881 and C885 in parallel with C882. Due to the relative capacitance ratios (1000:1), C881 is the dominant integrating element in the three-capacitor parallel combination.

Holdoff-Ramp Comparators

Two Holdoff-Ramp Comparators, U871 and U881, watch the holdoff ramp. Comparator U871 compares the ramp level to the user-defined reference level while U871 compares it to a predefined "end-of-holdoff" level.

Initially, a HI on the $\overline{Q}$ output of Holdoff Logic flip-flop U872A keeps Q781 turned on. The integration capacitors are discharged, and all the charging current is being shunted away from the capacitors through Q781. The user-definable holdoff reference applied to U871 pin 2 via R863 will always be more positive than this discharged level, so the output of U871 applied to the Holdoff Logic will be HI. This removes the reset from the Holdoff Logic flip-flop U872A and enables the occurrence of a trigger event (ATG going HI) to clock it.

When a trigger event occurs, discharge transistor Q781 turns off, allowing the selected integrating capacitors to charge. When the charging ramp reaches the user-defined HOREF (holdoff reference) level, the output of ramp comparator U871 will go LO. This resets flip-flop U872A of the Holdoff Logic which, in turn, turns Q781 back on.

The low-impedance path through Q781 discharges the integration capacitor very rapidly. When this discharging ramp crosses the −4.6 volt level (defined by R887 and R888), the output of U881 will go LO, resetting the Holdoff Logic circuit. This ends the holdoff pulse and allows the next trigger to be accepted.

Transistor Q781 remains on until the next trigger event, at which time the cycle repeats itself. Propagation delays through the Analog Trigger and the Record Trigger devices ensure that the discharging ramp will always reach the −5 V level before another trigger event can start the next holdoff ramp.

Table 3-8

Holdoff Delay Range for Current Source vs Charging Capacitor Combinations

Charging Capacitor	Holdoff Delay Range 909 μA Current Source	90.0 μA Current Source	9.09 μA Current Source	827 μA Current Source
1000 pF	10 ns - 100 ns	100 ns - 1 μs	1 μs - 10 μs	
1.1 μF	10 μs - 100 μs	100 μs - 1 ms	1 ms - 10 ms	10 ms - 100 ms

Holdoff Logic

The Holdoff Logic initiates and controls the holdoff ramp and produces the holdoff pulse controlling the delay between one trigger event and the next. It starts the holdoff ramp when a trigger event is detected, begins ramp discharge when the user-defined HOREF level is reached, and ends the holdoff pulse when the ramp crosses the "end-of-holdoff" level.

Initially, the Set and Reset inputs of U872A will be HI, allowing the flip-flop to watch the ATG (analog trigger) line for a trigger event. While it is waiting, its $\overline{Q}$ output will be HI, keeping Q781 on and the integration capacitors discharged.

When an ATG occurs, the HI level at the input of the flip-flop is clocked to the Q output while the $\overline{Q}$ output goes LO. This LO turns Q781 off and allows the selected current source(s) to charge the capacitors. At the same time, the LO is applied to pin 10 of U872B, forcing its Q output HI. This is the ATHO (analog trigger holdoff) signal and indicates that an analog trigger has occurred. This signal is applied to A/B Trigger Generator U150 (diagram 11) to prevent it from recognizing another trigger until the holdoff time ends.

As the charging ramp reaches the user-defined (front-panel Holdoff pot) reference level, the output from comparator U871 will go LO. This $\overline{CROSS}$ (reference crossing) level is applied to U872A and resets the flip-flop. The $\overline{Q}$ output, now HI, turns Q781 on and begins discharging the ramp at a rapid rate. The HI $\overline{Q}$ output from U872A removes the Set level from U872B and allows the ENDHO (end of holdoff) level from U881 to reset the ATHO level LO when the discharging ramp reaches −4.6 volts.

As mentioned earlier, propagation delays in the A/B Trigger Generator and the Trigger Logic Array ensure that another trigger (ATG) will not occur until Q781 has discharged the integration capacitors fully to −5 V. This ensures that holdoff ramps always start from a known point, and thus maintains holdoff stability.

The width of the ATHO pulse represents the time from which one analog trigger event was accepted to when the next trigger event is allowed (next acquisition record). By varying this time (front-panel Holdoff control) the displayed waveform may be adjusted to exclude undesired trigger events (which may cause display instability).

Jitter Correction Counters

The RAMP1 and RAMP2 Jitter Correction Counters convert the discharge time of their associated Jitter Correction Ramps to binary numbers relating trigger-event positions to the edges of the sample clock. Since operation of both Jitter Correction Counters is identical, only the RAMP1 Jitter Correction Counter will be described.

The RAMP1 Jitter Correction Counter is an eight-bit counter that is started and stopped by signals from the RAMP1 Jitter Correction circuit. It counts the 8 MHz clock pulses over the interval when the Jitter Correction Ramp is discharging, thus converting the peak value of the ramp to a binary number. Since that value is directly proportional to the time difference between a trigger event and the next sample-clock edge, the number derived by the counter gives a precise time measurement of where the trigger occurred with respect to the sampled data. That information is used by the System μP to correctly place the random-sampled data points obtained in REPET acquisition mode with respect to the previously acquired random data points as the waveform record is filled.

Initially, the RAMP1 Counter (composed of U852A and U852B) is held reset by the HI from pin 6 of U841A. When the START1 (start counter 1) input goes HI (signaling start of the slow discharge of integration capacitor C491, located on diagram 12), the rising edge of the next 8 MHz clock pulse will enable the counter by clocking the $\overline{Q}$ output of U841A LO. The Q output of the "stop" flip-flop U841B is LO and enables U851B to pass falling-edge clock pulses to U852A at an 8 MHz rate.

The counter increments until the RAMP1 Jitter Correction circuit detects the discharge threshold has been crossed. When this occurs, STOP1 (stop counter 1) applied to U841B will go HI. The next rising edge of the 8 MHz clock disables U851B via U841B and stops the counter.

The System μP may then read the counter contents via U752 at address-decoded location 620Fh. Counter contents for the B Jitter Correction Counter may be read at location 620Eh.

When the jitter ramps are reinitiated (in preparation for the next trigger event), the START1 and STOP1 signals will return LO. The next rising edge of the 8 MHz clock will reset the Jitter Correction Counter by clocking pin 6 of U841A HI.

Address Decoder

Address Decoder U781 monitors the address bus to determine when various buffers and registers on the Side board are to be enabled for communication with the System μP. Table 3-9 illustrates this decoding.

Table 3-9

Side Board Address Decoding

Address (hex)	Selects or Enables
6208	LED Register
6209	Front-Panel Register
620A	No connection
620B	No connection
620C	Write/Read Holdoff Register
620D	Set Holdoff Flip-Flop
620E	Read Jitter Correction Counter 1
620F	Read Jitter Correction Counter 2

Calibrator

The Calibrator circuit is composed of U731, U831, Q831, and associated components. Output frequency is set by the CALCLK signal from the Time Base Controller (diagram 8). The output frequency follows the SEC/DIV setting from 50 ns/div to 20 ms/div and is set to display from 2.5 to 10 calibrator cycles across the ten graticule divisions over those settings. This feature allows quick and easy verification of the acquisition time base rates. The Calibrator circuitry is essentially a voltage regulator that is switched off and on, producing a square-wave output signal at the CALIBRATOR loop.

When the CALCLK (calibrator clock) signal, at the base of U831D (applied via R885) is LO, U831C (configured as a diode) is forward biased. This shunts bias current away from Q831, keeping it turned off. When Q831 is off, the front-panel CALIBRATOR output is pulled to ground potential, through R831, thereby setting the lower limit of the CALIBRATOR square-wave signal.

As the CALCLK signal goes from LO to HI, the base of U831D is pulled HI, reverse biasing U831C. Bias current for Q831 now flows through R834 and R835, turning it on. The voltage at the emitter of Q831 rises to a level of +2.4 volts, determined by the voltage regulator composed of U731, U831A, U831B, Q831, and associated components. This regulated level is divided down to +400 mV p-p, by the resistive divider formed by R832 and R831, and applied to the front-panel CALIBRATOR loop at an effective output impedance of 50 ohms.

CCD OUTPUT

The CCD Output circuits (diagram 14) convert the two differential output signals from each CCD into single-ended signals for subsequent A/D conversion. The single-ended analog voltages are applied to Track-and-Hold circuits where they are held until the time-multiplexed A/D Converter digitizes the stored samples.

Single-Ending Amplifiers

There are four identical Single-Ending Amplifiers used to convert the four differential CCD array outputs to single-ended signals for A/D conversion. Operation of the Channel 1—Side 1 Single-Ending Amplifier is described.

Side 1 signal outputs from U450 are applied through R876A and R876B to the bases of U775A and U775B. Transistors U775A and U775B form a differential transconductance amplifier that provides high-impedance loading of the CCD array outputs. The collectors of the two transistors are connected to operational amplifier U770A which is configured as a differential-input, single-ended output transresistance amplifier. The connection of R771 to the +7.5 V supply causes the output of U770A to be level shifted to +7.5 V. The resulting output at pin 1 of U770A is a level-shifted, attenuated, single-ended replica of the differential CCD array output signal with most common-mode interference removed.

Track-and-Hold Amplifiers and Multiplexers

The Track-and-Hold Amplifiers and Multiplexers allow a single A/D Converter to digitize all the analog samples from both CCD arrays by time-multiplexing the output samples to the single converter. The four Track-and-Hold circuits are identical; and, for brevity, only the CH 1—Side 1 circuitry will be described.

The output from U770A is applied directly to sampling switch U560A, an enhancement-mode MOS-FET device. The switch gate is controlled via Q660 by the $\overline{\text{OSAM1}}$ (Output Sample from Channel 1) logic signal, and is closed when the data being shifted out of the CCD is stable. When $\overline{\text{OSAM1}}$ is LO, the switch is on, and hold capacitor C561 charges to the signal level of U770A. When $\overline{\text{OSAM1}}$ is HI, the switch is off, and C561 holds its voltage level. Figure 3-3 (shown previously in the "System Clocks" description) shows the timing of $\overline{\text{OSAM1}}$ and $\overline{\text{OSAM2}}$ during the Slow-Out and Short-Pipe modes of CCD operation. During Fast-In mode, $\overline{\text{OSAM1}}$ and $\overline{\text{OSAM2}}$ are both held LO.

The level stored on Hold capacitor C561 is buffered by operational amplifier U770B. The operational amplifier, along with Q771, converts the applied input sample voltage to output current.

Selection of the CH 1—Side 1 current signal to be digitized by the A/D Converter is controlled by the $\overline{DS11}$ (Data Select-Channel 1—Side 1) line. As shown in Figure 3-3, only one of the four DS signals will be LO at any time. A LO $\overline{DS11}$ signal applied to the base of Q770 will turn that transistor off. The other transistor of CH 1 (Q870) and both of the CH 2 transistors (Q780 and Q880) are on to shunt their associated signal currents to ground. Each of the four shunting transistors will be turned off in sequence to allow its associated signal current to pass to the CCD DATA node via a series common-base transistor (Q772 for Channel 1—Side 1). The resulting CCD DATA signal is a time-multiplexed combination of all four CCD output channels (two from CH 1 and two from CH 2).

Precise current matching of the Side 1 and Side 3 signal offsets is achieved by setting the DAC-generated CENTER 1 voltage at the time of calibration. Similar offset matching for CH 2 is done with the CENTER 2 signal.

Secondary Supplies

The Secondary Supplies circuit, composed of U861A, U861B, U861C, U861D, and associated components, provides operating voltages used by the CCD Output circuitry. The voltage level of the A2D REF (−0.5 V analog-to-digital reference) is determined by the current through R861 from operational amplifier U861C and is set by the resistive divider string formed by R762, R763, and R764 from the +10 V_{REF} supply. The other voltage outputs (+7.5 V and +9 V_{RA} and +9 V_{RB}) are set by the various taps on the resistive voltage divider and buffered by operational amplifiers.

A/D CONVERTER AND ACQUISITION LATCHES

The A/D Converter and Acquisition Latches (diagram 15) circuit consists of eight-bit A/D Converter U560, eight-bit Min-Max Comparator U740 and U732 (for ENVELOPE acquisitions), Acquisition Latches U631, U632, U630, and U640, and latch switching circuitry to direct and latch the acquired data point values.

A/D Converter

A/D Converter U560 is an 8-bit flash converter that digitizes the analog samples from the CCD arrays at an overall conversion rate of 2 MHz. (See the partial diagram 15 in the Diagrams section for instruments with serial numbers below B011146.)

The A2D REF voltage (−0.5 volt) is amplified and inverted by U880 to produce the 2 V reference voltage used by the A/D Converter. Noise and ripple are filtered from the amplified reference voltage by L770, C560, and C776. The negative side of the reference is tied to ground; therefore, input voltages for conversion may range from 0 V to +2 V. The time-multiplexed CCD Data signal current develops a voltage across R880 that is offset by the A2D REF and then amplified and inverted by U780 to produce an input signal to the A/D Converter within the 0 V to +2 V range needed. The amplified signal is applied to the analog input of U560 after being filtered by L780 and C770.

The input sample is converted on the falling edge of $D_2$4XPC, a 2 MHz clock signal. A valid data byte representing the analog input voltage appears on the A/D Converter output approximately 20 ns later. That data byte is applied to the 8-bit Magnitude Comparator formed by U740 and U732, with the four LSB going to U740 and the four MSB of the byte going to U732.

Envelope Min-Max Comparator

For ENVELOPE Mode acquisitions, glitch-catching at the slow SEC/DIV settings is done by the Envelope Min-Max Comparator circuit formed by four-bit comparators U740 and U732. At SEC/DIV settings slower than 50 μs, analog Peak Detectors U440 and U340 provide more samples than needed to fill the required 50 data points (25 min-max pairs) per division, so not all are saved. During each envelope sampling interval (1/50 of the SEC/DIV setting at 50 μs and slower), the Min-Max Comparator compares every Peak Detector min/max value from A/D Converter U560 to the last-latched maximum or minimum byte to determine which sample will be saved. If the new byte value is greater than the latched byte value, the MAX output of Comparator U732 (pin 5) will go HI; if less than the latched value, MIN at pin 7 will go HI. If the A/D output value is equal to the latched value, both connected outputs of Magnitude Comparator U732 will remain LO. The final min byte and max byte obtained from each channel during an envelope sampling interval are saved to the Acquisition Memory as part of the envelope waveform record.

Since the input to the A/D Converter is time multiplexed between CH1 maximum, CH2 maximum, CH1 minimum, and CH2 minimum values from the Peak Detectors, the latched data applied to the Magnitude Comparator from the Max/Min Latches must also be time multiplexed to maintain the correct relationship for making the comparisons (CH1 maximum against CH1 maximum, CH1 minimum against CH1 minimum, etc.). The necessary time multiplexing is done by the Envelope Latching Logic circuitry.

Acquisition Latch Switching

NORMAL MODE ACQUISITIONS. In non-envelope mode, the LOAD LATCHES signal from the Time Base Controller remains in its HI state. With LOAD LATCHES HI at one of the inputs of OR-gates U512A and U512B, the MIN and MAX signals from the Envelope Min-Max Comparators are ignored, and the outputs from the gates are held HI. This causes each sample from the A/D Converter to be clocked directly through the Acquisition Latches.

Output enabling of the four Acquisition Latches is controlled by the DS11, DS13, DS21, and DS23 data select lines, which also control the multiplexing of the CCD analog samples to A/D Converter U560. The states of these select lines, only one of which may be HI at a time, are latched into the four flip-flops of U520 and U521 by the 20 MHz system clock (C20M1). The $\overline{Q}$ outputs of the flip-flops control output enabling of the four Acquisition Latches. One at a time, their outputs are enabled to apply the acquired data point to the output bus for transfer to the Acquisition Memory input buffer (U613, diagram 8). Two hundred and fifty nanoseconds after one of the Acquisition Latches has been enabled, the rising edge of the $\overline{4XPC}$ signal clocks the HI state present on the D inputs of the flip-flops of U510 and U511 to the Q output of the enabled flip-flop. That rising edge then clocks the data byte from the A/D Converter through the enabled Acquisition Latch to the input buffer of the Acquisition Memory.

ENVELOPE MODE ACQUISITIONS. In ENVELOPE MODE, the LOAD LATCHES signal input to U512A and U512B (from the Time Base Controller, diagram 8) forces each clock flip-flop in turn to clock the A/D Converter output data byte into its associated latch by holding their D inputs HI during the first four data point conversions in each envelope sampling interval. These first four samples (one byte in each Acquisition Latch) initialize the min/max data in the latches for comparison to the remaining data samples that occur in the envelope sampling interval.

The Acquisition Latch Switching circuitry multiplexes the latched CH 1 and CH 2 maximum and minimum data bytes to the inputs of the Envelope Min-Max Comparator so that each digitized sample from the A/D Converter is compared to the correct previous sample (CH 1 Min to the previous CH 1 Min, etc.). It also provides the proper enabling and clocking to direct a new maximum or minimum data bytes into the correct Acquisition Latch.

As in NORMAL Mode acquisitions, output enabling of the four latches is controlled by the DS11, DS13, DS21, and DS23 data select lines. The $\overline{Q}$ outputs of the flip-flops control output enabling of the four latches, causing the Acquisition Latch corresponding with the selected CCD output (CH 1 or CH 2, maximum or minimum) to apply the previously latched data byte to the inputs of the Envelope Min-Max Comparator. A/D Converter output data is thus always being compared to the proper maximum or minimum data value.

When the Envelope Min-Max Comparator detects that the A/D Converter output byte value is either above or below the latched byte value, the MAX or MIN output of U732 will go HI respectively. The HI is passed through U512A (MIN) or U512B (MAX) to the D inputs of flip-flops U510 and U511. Since the A/D Converter output byte value could represent any of the four CCD array channels, the data select lines that determine what sample is currently being output from the CCD arrays are applied to the reset inputs of U510 (A and B) and U511 (A and B). Only that clocking flip-flop corresponding to the selected data sample is enabled by a HI data select line; all others remain in the RESET state.

When the $\overline{4XPC}$ (2 MHz) clock occurs, the enabled clocking flip-flop transfers the level at its D input to its Q output. If that level is a HI (a new max has been found), the current A/D Converter output data byte (the new max) will be latched into the associated Max Latch (either U632 or U631, depending on whether it is CH 1 or CH 2 data), where it then becomes the new comparison level. MIN clocks are produced by U510B and U511A in a similar fashion, latching the new MIN values into either U640 or U630.

Acquisition Latches

During Envelope Mode, the Acquisition Latches perform as Min-Max latches (U631 and U632 Max; U630 and U640 Min) to hold the maximum and minimum data point values being compared during the sampling interval. These values are compared to each newly converted waveform sample to determine when new maximums or minimums occur. Output enabling and data latching are controlled by the Acquisition Latch Switching as previously described.

DISPLAY AND ATTRIBUTES MEMORY

The Display and Attributes Memory (diagram 16) is where the Waveform Processor stores waveform and readout data that is to be displayed on the crt. Digital-to-Analog converters (DAC), under control of the Display Control circuits, convert this stored data to the vertical- and horizontal-deflection signal currents that drive the Display Output amplifiers.

Vertical Display RAM

Vertical Display RAM U431 stores the vertical-deflection data for four 512-point waveforms. Data points to be displayed are written from the Save Memory into the RAM by the Waveform μP (diagram 2) on the WD bus (waveform data bus) via bus transceiver U322. The stored waveform display bytes are read sequentially out of the Vertical Display RAM in blocks under control of the Display Counter (diagram 17) and applied to Vertical DAC U142 to produce the analog vertical deflection signal of the displayed waveform.

To write data into the Vertical Display RAM, the Waveform μP puts the data byte to be written onto its WD bus and sets its $\overline{\mathrm{WRD}}$ (waveform read) bit HI. This HI enables bus transceiver U322, and the vertical data is applied to I/O (in/out) pins of the RAM. At the same time, the $\overline{\mathrm{DISP}}$ signal is address decoded LO (from decoder U570, diagram 2) for addresses between 8K and 12K, and the WAB address bit applied to U323B selects the Vertical RAM U431 via U421A. When the Waveform μP generates its write pulse ($\overline{\mathrm{WWR}}$), it is transmitted through U422A and U422D, writing data into the Vertical Display RAM. This process occurs for each data byte (point) of waveform information.

To display the stored data points, the System μP loads the starting address of the data block to be displayed into the Display Counter and selects the Display Counter to address the Vertical Display RAM (via the Address Multiplexer). The System μP also sets the $\overline{\mathrm{YON}}$ (vertical display on) bit applied to U421A and U421B LO, selecting the Vertical Display RAM and enabling its outputs. As the Display Counter increments, the selected block of data is sequentially clocked out onto the DY bus (vertical-display data bus) and applied to Vertical DAC U142 to produce the vertical deflection signal current to the Vertical Output Amplifiers.

If the Waveform μP needs to read data from the Vertical Display RAM, it outputs an address within 8K to 10K address space of the RAM. This address block is decoded by U323B to enable both the Vertical Display RAM (via U421A) and bus transceiver U322. Since the Waveform μP is trying to read data, its $\overline{\mathrm{WRD}}$ (waveform processor read) line will be set LO. This enables the RAM outputs via U323C and U421B and causes buffer U322 to direct the data onto the Waveform μP data bus.

Horizontal Display RAM

Operation of Horizontal Display RAM U440 is identical to that of the Vertical Display RAM just described. The Horizontal RAM chip select ($\overline{\mathrm{CSX}}$) is gated through U323D for addresses between 10K and 12K when $\overline{\mathrm{DISP}}$ is LO. Data that may be stored in the Horizontal Display RAM includes two 512-point waveforms and 1K × 8 of readout information. During a waveform display, the data output from the Horizontal RAM may be routed to either the Vertical DAC or Horizontal DAC, providing for either two more YT displays or two XY displays.

Attributes RAM

Attributes RAM U430 contains 4K × 1 points of data that tell the Z-Axis system (using the BRIGHTZ signal) whether or not a data point read from either the Vertical Display RAM or the Horizontal Display RAM should be intensified. Operation of the RAM is similar to that just described for the Vertical and Horizontal RAMs except that the data path is only one bit wide.

The write enable of the Attribute RAM ($\overline{\mathrm{WRA}}$) is gated by U422C between 12K and 14K when $\overline{\mathrm{DATT}}$ is LO from decoder U570 (diagram 17). $\overline{\mathrm{WRA}}$ going LO enables the data from bit WD7 of the data bus to be written to the addressed location. Gate U422A prevents the $\overline{\mathrm{WWR}}$ clock from being gated to U422C if the Display Counter is selected (Waveform μP not in control of the address bus).

To read attribute data out of the RAM, the Waveform μP sets $\overline{\mathrm{WRD}}$ LO. This LO, along with the address-decoded $\overline{\mathrm{DATT}}$ (attribute data) line, enables buffer U423A and places the addressed output bit from the D0 output of U430 onto bit WD7 of the data bus.

When displaying data from either (or both) the Vertical RAM or Horizontal RAM (the addresses applied to all three RAM chips are the same), the attribute data for each data point will be applied to the Z-Axis circuit to determine the intensity of each point. A HI bit from the D0 output of U430 will intensify the displayed point.

Horizontal Data Buffers

The Horizontal Data Buffers, U320 and U321, are used to route the data from the Horizontal RAM to either the Horizontal DAC or the Vertical DAC, depending on the type of display being produced.

For normal waveform displays, vertical deflection data may come from either the Vertical or the Horizontal Display RAM. To route data from the Horizontal RAM to the Vertical DAC, the outputs of the Vertical RAM will be disabled ($\overline{\mathrm{OEY}}$), the outputs of the Horizontal RAM will be enabled ($\overline{\mathrm{OEX}}$ goes LO), and buffer U320 will be enabled ($\overline{\mathrm{XTOVERT}}$ goes LO). These three signals are all controlled by the System μP by writing bits XON and XTOVERT HI into Mode Control Register U541 (diagram 17) and writing a LO to the YON output of the register. Now, data addressed in the Horizontal RAM is applied to the Vertical DAC to produce vertical waveform deflections.

For XY displays, Mode-Control bits XON, YON, and XY are set HI while XTOVERT is set LO. This applies addressed data from the Vertical RAM to the Vertical DAC and applies the addressed data from the Horizontal RAM to the Horizontal DAC via now-enabled buffer U321. A waveform versus waveform (XY) display results.

During readout displays, both U320 and U321 will be disabled, along with the Vertical RAM. Since the readout character-code data is stored in the Horizontal RAM, it will be enabled. Character-code data from the Horizontal RAM is output to the Readout State Machine, where it is converted to the appropriate horizontal- and vertical-deflection codes.

Readout Buffers

Readout buffers U240 and U140 direct the ten least significant bits (LSB) from the Display Counter to the Horizontal DAC and the Vertical DAC during readout displays. The buffers are enabled by a LO $\overline{\text{RO}}$ signal at their enable inputs.

Four of these bits, Q6-Q9, are applied to the four most significant bits (MSB) of the Vertical DAC input through U140A and are used to select one of the 16 available readout lines for the selected character to be displayed on.

The six LSBs are applied to the six MSBs of the Horizontal DAC and are used to select one of the 64 possible character positions on the selected readout line. Since a maximum of only 40 characters will actually be displayed on any given line, the gain of the Horizontal Output Amplifier increases when readout is being displayed. The center 40 character positions then fill the display horizontally. This action is more fully explained in the Horizontal Output Amplifier description.

Ramp Buffers

Ramp Buffers U130 and U140 apply the ten LSBs of the Display Counter address (via Address Multiplexer U210, U212, and U221 on diagram 17) to the Horizontal DAC during YT waveform (non-XY) displays. Since the Display Counter address is merely incrementing for waveform displays, a horizontal ramp results at the Horizontal DAC outputs. Each sequentially acquired data point is thus displayed at its corresponding horizontal (time-dependent) address on the crt. The buffers are enabled by the $\overline{\text{COUNTEN}}$ (counter enable) bit from the Mode-Control Register.

Volts Cursor Register

Volts Cursor Register U241 is an address-decoded memory location where the System μP writes the eight MSBs of the vertical-position data for volts-cursor displays. Data written into this register, along with two bits written into the Misc Register U540, define the vertical position of the Volts cursor. Since volts-cursor displays have two cursors, the microprocessor alternately writes the position data for each cursor into the registers just before it is displayed. Data is written into the register on the rising edge of the address-decoded $\overline{\text{VCURS}}$ clock pulse.

Volts-cursor displays are a special type of "waveform" display wherein the vertical deflection data from the Vertical Display RAM is disabled (by turning off the RAM chip select), and the data bits in Volts Cursor Register U241 (and the DY0-DY1 bits from the Misc Register U540, diagram 17) are applied to Vertical DAC U142 instead. Cursor display is automatically selected by the Z-Axis logic when neither WFM nor $\overline{\text{RO}}$ are asserted (not a waveform display and not a readout display). To start the display, the System μP asserts the START bit in the Display Control Register as it would for a waveform display, starting the Display State Machine. The result is a horizontal line displayed on the screen at the level set by the data from the Volts Cursor Register. When displaying cursors on a waveform, the two LSBs from the Misc Register are set to 0, decreasing the resolution from 1024 levels to 256 levels.

Time Cursor Register

Time Cursor Register U441 provides a function similar to the Volts Cursor Register. Time-cursor data is written to the register from the system processor on the rising edge of the address-decoded $\overline{\text{TCURS}}$ clock (time-cursor clock). This data is applied to Horizontal DAC U250 (along with the DX0-DX1 bits from the Misc Register) to define the horizontal position of the cursor. A software ramp previously written into Vertical RAM U431 is applied to Vertical DAC U142 as the Display State Machine runs (started in the same way as the volts-cursor display).

For "directed-beam" cursors, such as the "+" made up of individual microprocessor-directed points displayed on screen, both cursor registers are enabled after the System μP writes one dot of XY position data into the registers. To display the addressed point, the processor sets the HZON (host z-axis on) bit in the Misc Register LO, then HI. The processor then calculates the next point of the "+", writes the position data to the cursor registers, enables the registers, and sets $\overline{\text{HZON}}$ LO to display that point. This cycle continues until the entire "+" is drawn.

Vertical DAC

Vertical DAC U142 generates complementary vertical-deflection currents used to drive the vertical deflection system from the digital data applied to its inputs. The data that appears at the DAC inputs is selected by the microprocessor via the Mode-Control Register and determines what type of display will be generated. The exclusive-OR gate U350A inverts bit DY9 during "non-readout" displays to create "bipolar" data relative to the vertical (graticule) center of the crt.

Horizontal DAC

Operation of Horizontal DAC U250 is identical to that of the Vertical DAC and produces the horizontal-deflection signal currents that drive the Horizontal Output Amplifier.

Diagnostic Buffers

The Diagnostic Buffers, U141 (vertical) and U243 (horizontal), allow the System μP to monitor the data being applied to the Vertical DAC and Horizontal DAC respectively. By forcing known data patterns through the various data paths and observing the data arriving at the DAC inputs, the diagnostic routines can verify functionality of much of the display system hardware. The buffers are enabled during diagnostics via the address-decoded Register Select logic.

DISPLAY CONTROL

The Display Control System (diagram 17) produces the crt waveform and readout displays from data stored in the Display RAM. The data, originally stored by the Waveform μP or the System μP, is read out of the RAM and is used to produce the individual dots that make up both waveform and readout displays. The Display System has two "state machines" for converting the stored data into the horizontal and vertical deflections that produce the waveform dots and readout characters.

For YT waveform displays, the Display State Machine generates 512 linearly spaced points across the face of the crt (horizontally). Each of these points may be displayed at any of 256 vertical positions on the crt. For XY displays, each of the 512 points that make up a waveform may be placed anywhere on the screen in a 256 × 256 matrix.

For readout displays, the face of the crt is vertically divided into 16 character lines each having 40 horizontal character positions on the line. Each of these character positions corresponds to a specific location in the readout memory space (stored in the Horizontal RAM). To display the readout, the Readout State Machine sequentially reads through the readout memory and displays the required character at the corresponding (memory-mapped) location on the crt screen. Each displayed character consists of a sequence of individual dots produced by the Readout State Machine.

Each of these display types is controlled and initiated by the System μP. The acquired waveform data points are written into the Display RAMs by the Waveform μP and the readout data is written in by the System μP. Display of this stored data is controlled by the System μP through data latched into the several display registers. The data written to the registers determines what type of display should be produced, how long (number of data points) it should be, and when it should start.

Register Select

The Register Select stage, composed of U550 and U450D (along with the System μP address decoding), address decodes the three LSBs of the System μP address bus to enable any of eight display "registers" for a read or write. These registers control such things as display mode (how the stored data is displayed, either XY or YT), which waveforms are displayed, and whether or not cursors and readout are to be displayed.

The enable inputs for U550 are controlled by the System μP. The $\overline{\text{DISPSEL}}$ (display select) is an address-decoded signal produced on the Processor board when any of the display memory addresses are output by the System μP. Negative OR gate U450D provides an enable to U550 whenever the System μP is trying to read or write. Address bit A3 provides the final enable when it is HI.

Once enabled, the three lowest address bits are used to select one of the eight outputs from U550. These outputs, when LO, enable or load one of the eight display registers. Enabling of these individual registers is explained in more detail in the specific register descriptions.

Mode Control Register

Mode Control Register U541 and associated gating circuits composed of U340, U442, U423B, and U350C, control the operating modes of the various display state machines.

Data from the processor data bus is written into data latch U541 when the $\overline{\text{MODECON}}$ (mode control) bit from U550 returns HI (after the PWRUP reset goes HI). These latched bits are used as enables to other portions of the display circuitry and control the overall function of the display.

NAND gates U340C and U340D do not allow the $\overline{YON}$ and $\overline{XON}$ enables (controlling the vertical and horizontal RAMs respectively) unless the display counter is running (PRESTART + DISPLAY is HI). Exclusive-OR gate U350C and tristate buffer U423B are used to enable horizontal-deflection bit DX1 only when the time cursor is being displayed (both RO and COUNTEN are LO). The remaining bits from the mode-control register are NANDed with the $\overline{DISP}$ (display running) signal and only affect their associated functions while the Display State Machine is running.

Buffer U542 provides a way for the System μP to read back the data written to the Mode Control Register U541.

Display Control Register

The operation of Display Control Register U530 is similar to that just described for the Mode Control Register. When enabled (by $\overline{DISCON}$), data from the data bus is written into U530 on the rising edge of the System μP $\overline{WR}$ (write) clock. These data bits determine how many data points are displayed, whether the display is to be read from memory in envelope mode (ENV), and whether the intensity of each dot should be bright or dim (DOTS).

The buffer U531 provides a way for the System μP to read back the contents of the Display Control Register.

Miscellaneous Register

Operation of the Miscellaneous Register is identical to that of the Display Control Register just described. The output bits control miscellaneous circuit functions, as the register name implies. The function of each bit is explained in the description of the associated circuitry.

Buffer U540 allows the System μP to read back the contents of the Miscellaneous Register.

Display Clocks

The state machines of the Display System run on clocks derived from the 5 MHz clock of the Secondary Clock Generator U710 (diagram 7). The Display Clocks circuit provides the signal frequency division and gating logic to properly condition clocks for the Display System circuitry.

The 5 MHz clock signal from the Time Base Controller circuit is buffered and inverted by U413C and is used to drive the Readout State Machine.

The 5 MHz clock is also applied to the counter made up of decade counters U410A and U410B, producing several intermediate clocks at their outputs. The 1 MHz 2QC clock, the 500 kHz 2QA clock, and the 250 kHz clock from U410B are gated together by U411A and produce the $\overline{SAMPLE}$ clock, having a LO duty cycle of 12.5%.

Buffer U413A inverts the 250 kHz clock used for the Z-Axis and Display State Machines.

Gates U411C, U412C, and U412D make up a clock-steering circuit that selects the source for clocks to the counters, depending on display mode. When displaying waveforms, readout, or cursors, the DISPLAY bit applied to U411C is HI. The RO and $\overline{RO}$ signals, applied to U412C and U412D respectively, do clock selection depending on whether readout or waveform data is to be displayed.

For waveform displays, RO applied to U412C is LO, holding its output to U411C HI. This HI, along with the HI DISPLAY bit, enables U411C, and the output of U411C follows the 250 kHz signal applied to U412D (since $\overline{RO}$ is HI). For readout displays, RO and $\overline{RO}$ are HI and LO respectively. This holds the output of U412D HI, and the output of U411C follows the $\overline{CLKRAM}$ (clock RAM) signal from the Readout State Machine. To completely disable the Counter clocks, the Display State Machine sets the DISPLAY bit applied to U411C LO.

Display Counter

The Display Counter stage, made up of U211, U220, and U222, generates the sequential addressing that the Display and Readout State Machines use to read the stored waveform and character data out of the display RAM. Depending on the type of information to be read from RAM (waveform or readout), clocks to the counter are selected by logic to produce waveform and readout displays at the proper refresh rates.

To display stored data, the System μP writes the eight MSBs of the 12-bit starting RAM address into U211 and U220 over the data bus by generating a LO $\overline{LDCOUNT}$ from the Register Select stage. The 4 LSBs of the address (all LO) are also loaded at the same time into U222. The counter then starts counting at the selected rate. When the count in U222 reaches 15, its $\overline{RCO}$ (ripple-carry output) goes LO for the last half of the clock cycle and enables U220. Due to a two-gate propagation delay through U222 to the $\overline{RCO}$ output, U220 will still be enabled on the rising edge of the next clock. This clocks U220, which is then disabled until U222 counts another 16 clocks. Counting continues, and eventually the $\overline{RCO}$ output of U220 enables U211, causing it to increment in a similar fashion. Counting continues until the Display State Machine determines that the desired display is complete, at which time it shuts off clocks to the counter.

The outputs of the counters change synchronously and are applied to the Multiplexer stage, which selects between these counter outputs and the microprocessor address bus for Display RAM addresses. The MAX output from U222 (occurring on count 15) is used in the Readout State Machine.

Address Multiplexer

The Address Multiplexer stage, under control of the Display State Machine, selects the address source for the various display RAMs from either the Waveform μP address bus or the Display Counter.

When the Waveform μP is writing acquired data into the display RAMs (Horizontal or Vertical), the Display State Machine selects the Waveform μP address bus (WA0-WAB) as the source for RAM addresses by setting the COUNTSEL (counter select) line LO. When displaying the stored data, COUNTSEL is HI, and the outputs from the Display Counter are routed to the various RAM address lines.

Exclusive-OR gate U350B is used to invert counter bit DC0 when displaying envelope data (ENV is HI). This causes data pairs (max-min) to be read out in reverse (relative to how they were stored) and produces an envelope display that always starts with a MIN point.

Display State Machine

The Display State Machine determines when display of stored data should start and stop, depending on other conditions in the Display System.

To start a display, the System μP writes a HI for the START bit into Display Control Register U530. This HI is applied to the D input of flip-flop U415A and clocked to its Q output on the falling edge of the 250 kHz clock (rising edge of the $\overline{250\ kHz}$ clock). This latched STARTDIS bit (HI) is then applied to the D input of U414A and to pin 9 of U313. Since the Display Counter has not reached its final value (this is the starting point), the output level of the three lower AND gates within U313 are LO, thereby enabling the output AND gate (it has inverting inputs). With the previous display cycle finished (as it is for this discussion), the DISDN (display done) bit applied to pin 10 of U313 is also HI. The 250 kHz clock applied to this enabled AND gate causes the output of U313 to go HI on the falling edge to clock the HI STARTDIS bit to the Q output of U414A. This latched signal is the DISPLAY bit that enables the Display Counter clocks (via U411C).

The DISPLAY bit is delayed slightly by the propagation delays of the START bit through the flip-flops and gates. Therefore, the PRESTART bit is written HI to cause the output of U323A to be HI until the DISPLAY bit is latched into flip-flop U414A. The HI PRESTART + DISPLAY bit from U323A selects the counter outputs to address the Display RAMs (via the Address Multiplexer stage). After the DISPLAY bit is latched into U414A, the System μP sets the START and PRESTART bits from the Display Control Register LO. The LO START bit is clocked to the Q output of U415A, disabling the 250 kHz clocks through U313 to U414A, and the LO PRESTART bit allows the DISPLAY signal to control OR-gate U323A.

With the DISPLAY bit to U411C set HI, clocks from either U412C or U412D clock the Display Counter. Which one does the clocking depends on whether the data to be displayed is readout or waveform information. If readout information is being displayed, the $\overline{RO}$ bit (from the Mode Control Register) applied to U412D will be LO, disabling the 250 kHz clock (output of U412D is held HI). At the same time, R/O applied to U412C is HI, enabling the $\overline{CLKRAM}$ (clock RAM) signal from the Readout State Machine to clock the address counters.

If waveform data is to be displayed, $\overline{RO}$ from the Mode Control Register is HI and RO is LO. The LO RO level applied to U412C closes the $\overline{CLKRAM}$ path (output of U412C is held HI) while the HI $\overline{RO}$ level applied to U412D opens the 250 kHz clock path through U412D and U411C.

The two display-control bits, STOP512 and STOP1024, applied to U313 determine how many data bytes are read from the selected display RAM (Horizontal, Vertical, and Attribute) before stopping the current display cycle. Only one of these two bits is HI at any time. The outputs of the unselected AND gates within U313 are LO, and along with the LO caused by the LO STARTDIS bit, enable the output gate of U313. The selected AND gate watches its appropriate counter bit and, on the falling edge of the bit, causes a clock at the output of U313. This clocks the now LO STARTDIS bit to the Q output of U414A, disabling U411C (and thus clocks to the Display Counter), and resets the DISDN at the $\overline{Q}$ output HI in preparation for the next display cycle.

The DISDN signal is also sent to the System μP Interrupt Logic to tell it when the currently assigned display task is complete. When the processor detects the HI DISDN, it writes data out to the display register to start the next display cycle. The System μP, knowing how much waveform and readout data needs to be displayed, does the writing at a rate that keeps the overall display-refresh rate constant.

Displaying a single waveform requires 512 data points be read from RAM, so STOP512 is set HI. A two-waveform display or a single-waveform envelope display will require STOP1024 to be HI. Readout displays may also consist of up to 16 lines of readout, in which case STOP1024 would be set. This is further explained in the Readout State Machine description.

The $\overline{\text{STOPDIS}}$ bit applied to the reset inputs of U414A and U415A provides the System μP with a way to stop any display in process.

Z-Axis Logic

The Z-Axis Logic determines when to turn the display beam on or off for each of the various display modes. These displays are readout, waveform, cursor-normal, cursor-dashed, and diagnostic (host-forced) Z-Axis on.

To enable readout or waveform displays, the Display State Machine sets its DISPLAY output HI. This enables U415B, U414B, and U312C.

During readout displays, the $\overline{\text{RZON}}$ (readout Z-Axis on) signal from the Readout State Machine is LO for each point that should be turned on and HI when the display should be blanked. The level of this signal is sampled by U415B at a 5 MHz rate. The Q output of U415B controls the Z-Axis through U450B and U223C, and since it is synchronized to the 5 MHz clock used to clock the Readout State Machine, the intensity of each dot is not the same.

For waveform displays, the DOTS bit from Display Control Register U530 will be set HI by the System μP. This HI, along with the HI DISPLAY signal from the Display State Machine, enables U312C. As long as a waveform display is taking place, the 250 kHz clock turns the display dots on and off with a 50% duty cycle via U312C and U223C. When the Display State Machine determines that the waveform display is over, it sets its DISPLAY bit LO, disabling U312C. For nonwaveform displays, the DOTS bit is LO, also disabling U312C.

For cursor displays, the HI DISPLAY signal enables D flip-flop U414B, and the $\overline{\text{250 kHz}}$ clock begins clocking the data from the output of U312B to the Q output of U414B. Since a cursor display is neither a waveform nor a readout display, the DOTS signal applied to inverter U413D is LO while the $\overline{\text{RO}}$ signal applied to NAND-gate U312B is HI. This enables U312B, and the output of U412A then controls the D input signal to flip-flop U414B. That signal is clocked to the Q output and applied to U223C to control the Z-Axis signal $\overline{\text{ZON}}$.

When displaying the inactive cursor (the one not selected for control by the cursor pot), the ACTIVELC (active line cursor) bit from the Misc Register to pin 2 of U412A is set LO. This causes the output of U412A to be HI, and the Z-Axis remains on as long as that particular cursor is being displayed.

When the other (active) cursor is to be displayed, the System μP sets the ACTIVELC bit HI. The output of U412A is then dependent on the DC3 signal from the Display Counter. The DC3 signal has a 50% duty cycle and changes states every eight characters (for cursors, the character is a single dot), so the resultant cursor display appears as a dashed line.

The $\overline{\text{HZON}}$ (host Z-Axis on) bit applied to U450B from the Misc Register (U540) allows the System μP to turn the Z-Axis on during diagnostics and allows verification of Z-Axis functionality. When set LO, $\overline{\text{HZON}}$ produces a LO at the output of U450B output, and thus at the $\overline{\text{ZON}}$ (Z-Axis on) output of U223C. This keeps the Z-Axis turned on until the $\overline{\text{HZON}}$ bit is reset HI by the processor.

Readout State Machine

The Readout State Machine produces the alphanumeric readout on the crt from character-code data stored in the Horizontal RAM. For readout displays, the face of the crt is vertically divided into 16 character lines each having 40 horizontal character positions on the line. Each of these character positions corresponds to a specific location in the readout memory space (stored in the Horizontal RAM). To display the readout, the Readout State Machine sequentially reads through the readout memory and displays the required character at the corresponding (memory-mapped) location on the crt screen. Each displayed character consists of a sequence of individual dots produced by the Readout State Machine.

Since the position of the character on the screen is related directly to the RAM location, the LSBs of the Display Counter are used to position the character on the crt screen. The six LSBs of the counter are applied to the Horizontal DAC and select 1-of-64 character locations on a line (only the center 40 are displayed) and the next four LSBs are applied to the Vertical DAC to select 1-of-16 display lines.

Once this rough positioning is done, the Readout State Machine displays a sequence of dots that make up the addressed character, each dot being positioned relative to the rough display position.

Character codes, sequentially read from the Horizontal RAM, are applied to seven address lines of a character ROM (U420). These select the block of dot-position data within the ROM corresponding to that character code. Five more address bits are generated by an incrementing Dot Counter (U416B and U416A) and sequentially clock the XY dot-position data from the selected ROM block. The horizontal and vertical dot-position data is applied to the Horizontal and Vertical DACs and is used to deflect the crt beam relative to the selected on-screen character position.

The operation of the Readout State Machine is ROM based; it proceeds through a sequence of states based on data loaded from a ROM.

Initially, when power is first applied, both the PWRUP (power up) and DISPLAY signals applied to U450A are LO. These states cause a LO at the reset input of presettable counter U231 that resets its output count to zero. The reset state will remain until the instrument power comes up (PWRUP goes HI) and the system processor determines that a display should be produced (it starts the Display State Machine and DISPLAY goes HI).

With the reset removed, presettable counter U231 is enabled to either count (up) or do a parallel load from the four MSBs output from the addressed location within U232 on the next rising edge of the 5 MHz clock. The COUNT/LOAD select line from the data selector U230 determines whether counting or loading will occur.

The LOAD/DECIDE bit output from the addressed ROM location within U232 is applied to the enable input of U230 and determines whether the COUNT/LOAD line is forced LO (U230 disabled by LOAD/DECIDE being HI) or whether one of the decision inputs is selected (via select inputs A, B and C of U230). When the LOAD/DECIDE bit from U232 is LO, it indicates that the state machine is at a decision point as to whether counter U231 should count or load (instead of just automatically loading the next state). The condition tested to make this decision is selected by the select inputs to U230 and are as follows:

D0—R/O (readout) goes HI when a readout display should start.

D2—AND gate U233A watches for the 12th character address (11).

D3—EOCH (end of character) goes LO on the last character dot and causes the next state to be loaded.

D4—EOL (end of line—X9 bit U440, diagram 16) goes HI when readout line is over.

D5—AND gate U223B watches for the 64th character address (63) to indicate that the next character is the beginning of a new line.

ROM U330, addressed in parallel with U232, outputs three bits unique to the state selected and is used to clock the dot counter (U416B and U416A), clock the Display Counter, and to turn on the Z-Axis for readout dots.

The flow chart in Figure 3-8 illustrates operation of the Readout State Machine.

As the state machine runs, the counter outputs of U231 (the "current-state") are first reset to state "0." The data output from the O4-O7 (outputs 4-7) lines of U232 contain the "next-state" data, O1-O3 (outputs 1-3) hold the select data for the data selector U230, and output O0 (output 0) is the LOAD/DECIDE bit. In addition, the outputs from U330, used to turn on the Z-Axis if appropriate (RZON), increment the character ROM dot counter U416B-U416A (CKDOTCTC), and clock the Display Counter (CLKRAM) to address the next character, are now at their state 0 condition (all HI).

The COUNT/LOAD signal from U232 determines what action counter U231 takes when the next 5 MHz clock occurs. If LO, the data from outputs O4-O7 of U232 is loaded to the counter outputs; if HI, the counter increments.

The LOAD/DECIDE line, along with the three channel-select inputs to U230, gives the state machine the ability to determine when certain events have occurred. When the LOAD/DECIDE bit from ROM U232 is HI, indicating that no decisions need be made in the present state, data selector U230 is disabled and the COUNT/LOAD output to U231 are forced LO. On the next 5 MHz clock, the "next-state" data from U232 (outputs O4-O7) is merely loaded into counter U231.

If the "present-state" data output from U232 has the LOAD/DECIDE bit set LO, indicating that some circuit condition needs to be tested to determine what to do next,

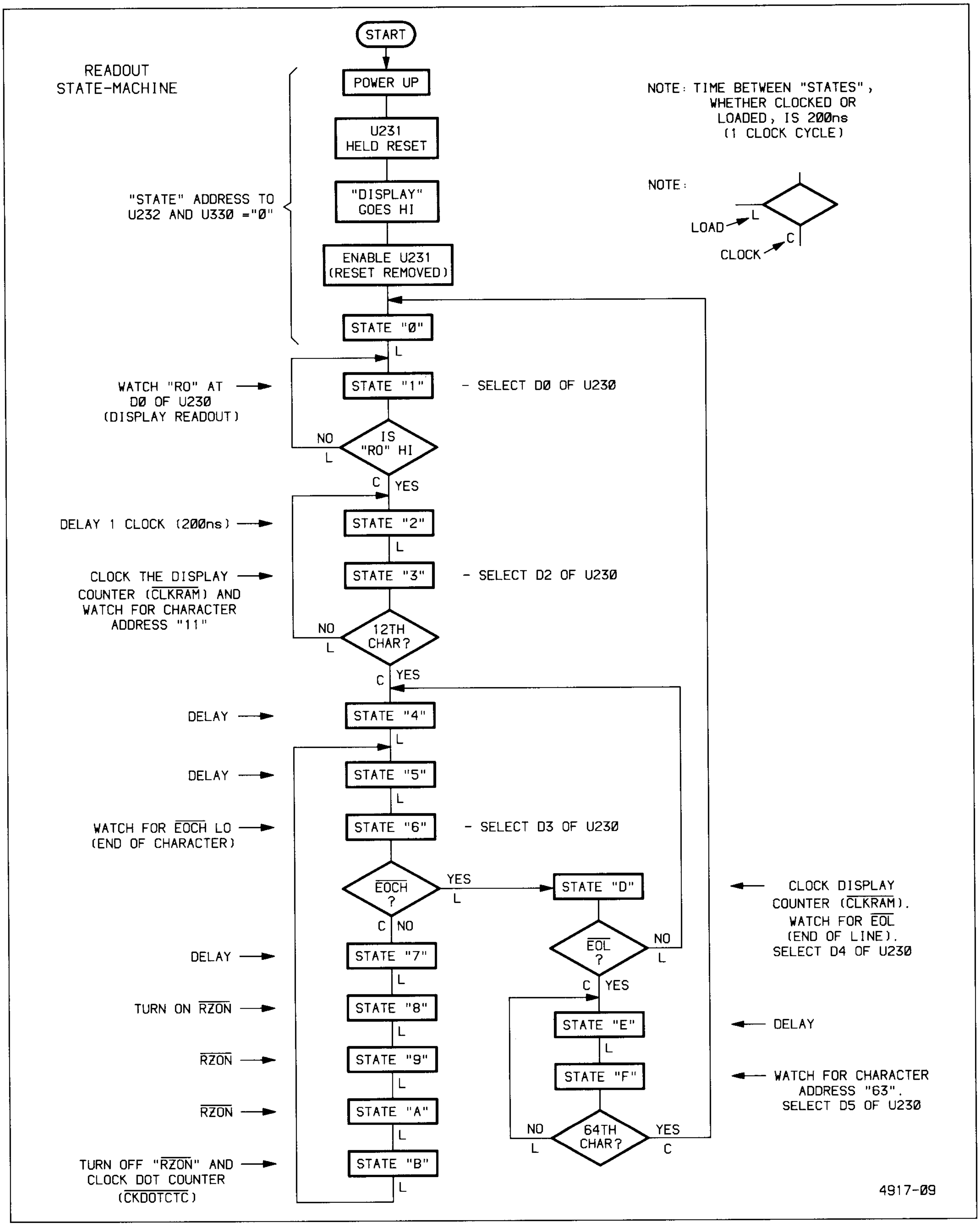


Figure 3-8. Readout State Machine flow chart.

data selector U230 is enabled. The three data bits (O1 through 03) from U232 define which condition needs to be tested and selects one of the D inputs of U230 to route to U231 via the COUNT/LOAD line. Whether or not the condition being tested for is present at the selected D input determines whether counter U231 counts or loads.

To go from state "0" to state "1," data from U232 is loaded into U231.

The state 1 data from U232 has the LOAD/DECIDE signal set LO, and the next three bits select input D0 of U230 to watch. This is the R/O (readout) line, and it is set HI by the System μP when it wants to start a readout display. If R/O is LO (don't start yet), COUNT/LOAD is also LO and the "next-state" data from U232 is loaded into counter U231. For state 1, the next-state data is also 1, so the state machine just cycles in state 1 until R/O goes HI.

When R/O goes HI, the COUNT/LOAD line follows and the next 5 MHz clock increments the counter to state "2." State 2 has the LOAD/DECIDE bit set HI, so the next clock merely loads the next-state data (which happens to be 3) into U231.

State "3" clocks the display RAM (using CLKRAM from U330), enables U230, and selects its D2 input. AND gate U223A, producing the D2 input level, monitors the Display Counter address lines, looking for address 11. Address 11 corresponds to the twelfth character (remember character 0) and the first character displayed on the crt. (See Display Output description for further explanation.) If address 11 has not been encountered yet, the next-state data from U232 will be loaded into U231.

This next-state data is 2. Returning to state 2 resets the CLKRAM bit from U330 HI so the next state 3 will clock the Display Counter again. This loop between states 2 and 3 continues to clock the Display Counter until U223A detects address 11. When this occurs, COUNT/LOAD goes HI and the next 5 MHz clock increments the state to "4."

State "4" resets CLKRAM HI and disables U230. The next clock loads state "5," a 200 ns delay, into U231. The next clock loads state "6."

State "6" data from U232 enables U230 and selects its D3 input. This is the EOCH (end of character) bit from the character ROM U420 and will only be LO for the last dot of any given character. As long as EOCH is HI (not the last dot), U231 will increment to state "7" on the next clock. State 7 disables U230, terminating the test condition.

State "8" is loaded from state 7 and turns on the Z-Axis via RZON (readout Z-Axis on) from U330. States "9" and "A" (hex) are sequentially loaded from the previous state and also have RZON asserted. These three cycles in sequence turn the Z-Axis on for 600 ns for each readout dot to be displayed.

State "B" is loaded from state "A" and does two things. It turns RZON off (HI) and sets CKDOTCTC (clock dot counter) LO, incrementing the dot counter made up of U416B and U416A. This addresses the next byte of XY deflection data within U420 in preparation for the next dot display cycle.

The next 5 MHz clock loads state 5 from state B and resets the CKDOTCTC from U330 HI. State 6 is next loaded from state 5 and is once again checking for EOCH (described earlier).

If EOCH is set LO this time (signaling the last dot), counter U231 will be loaded to state "D" (instead of clocked to state 7 as described earlier). State D clocks the Display Counter via CLKRAM, enables U230 and selects its D4 input. This input monitors the EOL signal (X9 bit) from the Horizontal RAM which will be set HI when the last character of a given line of readout information has been displayed. When EOL (end of line) is detected, U231 increments to state "E." If it is not detected, state 4 will be reloaded from state D data and the next character will be displayed as described before.

State "E" resets the CLKRAM signal from U330 and disables U230. The next 5 MHz clock loads state "F" from state E data.

State "F" data clocks the Display Counter via CLKRAM, enables U230 and selects its D5 input. AND gate U223B watches for Display Counter address 63; i.e., the 64th character. If the 64th character is not detected, state E is loaded from the state F data, resetting CLKRAM HI in preparation for the next state F and the associated CLKRAM pulse. The looping between states E and F continues to increment the Display Counter until U223B detects address 63 (the 64th character).

The 64th character is significant in that the next character is the start of the next line. When address 63 is detected, U231 is clocked from state F to state 0. The routine is now back to where it started, and the next line may be displayed in a similar manner.

DISPLAY OUTPUT

The Display Output circuits (diagram 18) convert the current outputs from the Horizontal and Vertical digital-to-analog converters (DACs) to the voltage levels used to drive the crt deflection plates. The Display Output circuit includes a vector-generation function that allows the individual dots of a waveform display to be translated into smooth lines connecting the waveform points (vectors on). A Display Mode switching circuit under control of the System μP selects which type of signal is applied to the output amplifiers for the various display types (envelope, dots, vectors, or readout).

Vertical and Horizontal Input Buffers

Operation of the Vertical and Horizontal Input Buffers is identical; so for brevity, only the Vertical Input Buffer circuit operation is described.

The Vertical Input Buffer, JFET operational amplifier U170 and its associated components, translates the complementary output currents from the Vertical DAC (U142, diagram 16) to an output voltage. Complementary, in this case, means that the sum of the currents is a fixed value; if one current increases, the other decreases by the same amount.

Current from the Vertical DAC output connected to pin 3 of U170 develops a voltage across R163. This voltage causes the output of U170 to move in the same direction until the feedback current through R164 applies an equal voltage to pin 2 of U170. The output voltage of the Input Buffer at pin 6 is the (signed) sum of voltages across R163 (+) and R164 (−). The gain of the stage is 1 V per mA (differential).

Vertical and Horizontal Vector Generators

Operation of the Vertical and Horizontal Vector Generators is similar. For brevity, only the Vertical Vector Generator is described in detail, and the differences in the two Vector Generators pointed out. Each Vector Generator consists of a High-Current Difference Amplifier, a Sample-and-Hold circuit, and an Integrator circuit that transforms the step voltages output from the Sample-and-Hold circuit to smooth transitions (vectors). See Figure 3-9 for a simplified diagram.

The step transitions from Vertical Input Buffer U170 are applied to the High-Current Difference Amplifier, made up of U281, Q182, Q181, and associated components, through R172. Initially (before the first integration occurs), input pin 3 of U281 is referenced to ground through R161; deviation from this ground reference seen at the other

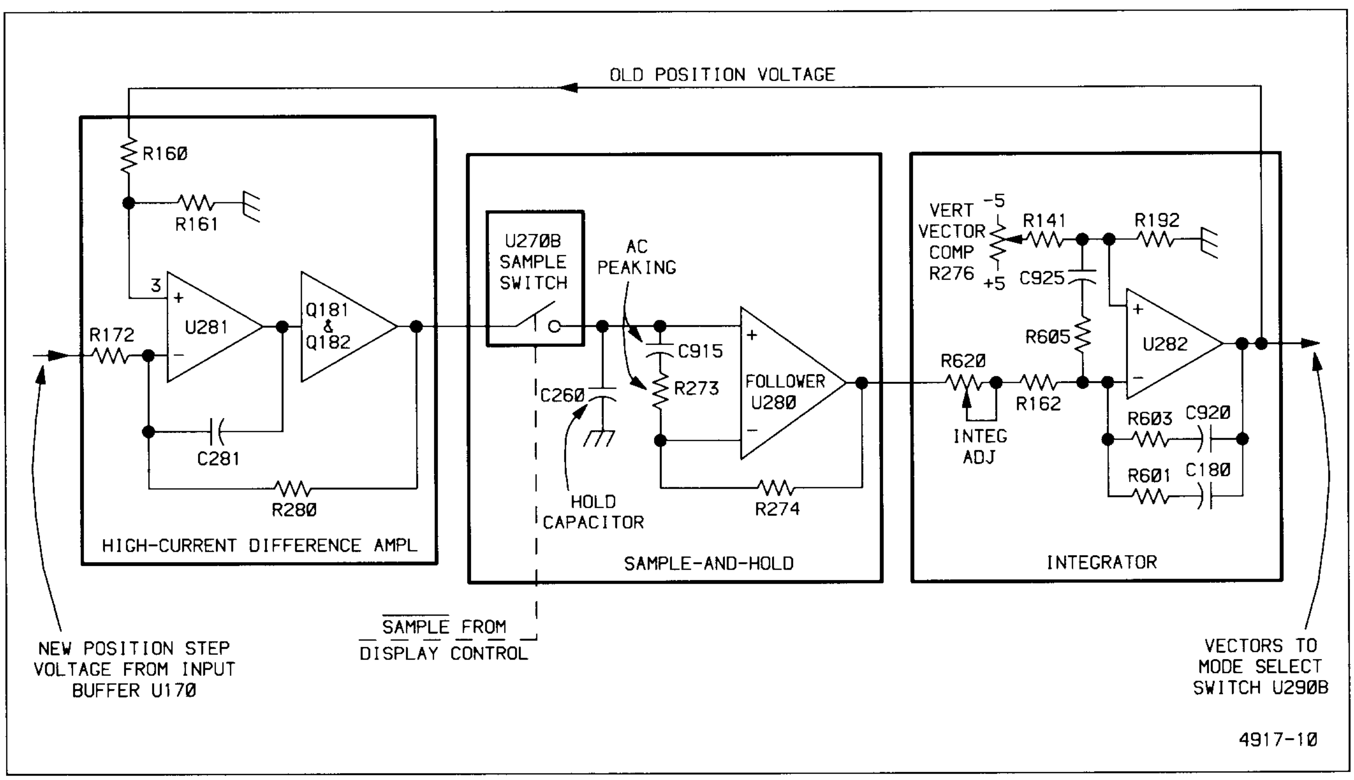


Figure 3-9. Vertical Vector Generator.

input (pin 2) causes the output (pin 6) of U281 to move in the opposite direction. This voltage change is applied to the base of Q181 (via R145) and to the base of Q182 (via series diodes CR193 and CR194 from R145). These transistors are biased in their linear region and act as emitter followers for the signals at their bases. Two series diodes between the bases of the transistors separate the base voltages by 1.2 volts, so the emitters of both transistors are at about the same potential. Negative feedback from the amplifier output (junction of R194-R196) is via R280. The resistance ratio of R280 to R172 sets the voltage gain of the amplifier at −1. Capacitor C281, from the output of U281 back to the input at R172, provides a fast feedback path to smooth transition spikes.

Sample Switch U270B, Hold Capacitor C260, and Voltage Follower U280 form a sample-and-hold circuit. The output of the High-Current Difference Amplifier at the junction of R194 and R196 is allowed enough time to settle to its new level before the 250 kHz $\overline{\text{SAMPLE}}$ pulse goes LO. At that time, the output of the Difference Amplifier is applied to the input of Voltage Follower U280A, and C260 is charged rapidly to that output voltage level. The $\overline{\text{SAMPLE}}$ pulse returns HI, and the BX output of the data selector goes to its high-impedance state to start the hold time. Voltage Follower U280 has high-impedance FET inputs; therefore, Hold Capacitor C260 discharges very little during the hold time.

The output of Voltage Follower U280 is held at the voltage level across C260; that level causes some value of current to flow through the series combination of R620 and R162 to the input of Integrator U282 (pin 2, the inverting input). The output of Integrator U282 at pin 6 ramps linearly for the duration of the hold cycle. (Actually, it ramps for almost the whole cycle, since the charge on Hold Capacitor C260 reaches the final level slightly before the sample switch is opened to start the hold time.) The time constants of the integrating network composed of R162 and of the series combination of R601 and C180 in parallel with R603 and C470 are such that the output of Integrator U282 reaches the new point position just as the next $\overline{\text{SAMPLE}}$ gate to U270B occurs. (A step change of 1 volt at the input causes a ramp of −1/4 V per μs (or −1 volt over the 4 μs cycle hold time.)

The feedback of this "new" point position to U281 through R160 modifies the reference at pin 3 of Difference Amplifier U281 (new reference is one-half the output voltage at U282 pin 6). The next voltage from Input Buffer U170 is applied to the input (pin 2 of U281) of the Difference Amplifier which now amplifies the difference between the present point position on screen (represented by the voltage at pin 3 of U281A) and the new position (applied to pin 2 of U281A). This difference voltage is sampled and stored on Hold Capacitor C260 where it sets a new current level through R162 and R620 from the output of Voltage Follower U280 to the input (pin 2) of Integrator U282A.

This cycle just described of comparing the old position to the new one, sampling the difference, and ramping to the new position continues for each point of a vector waveform display.

The adjustment associated with Voltage Follower U280 is INT ADJ potentiometer R620. This pot (the integrator adjustment) is used to compensate for charge current introduced from analog switch U270B. A corresponding adjustment is not present in the Horizontal Vector Generator circuit. A VECTOR COMP adjustment is present in both the Vertical and Horizontal Integrator circuits. The pots (R276 vertical and R376 horizontal) are used to adjust for minimum vertical and horizontal offset between the vector and dot displays.

Mode Select

The Mode Select Switch consists of data selector U290A (horizontal) and U290B (vertical). The switches route the various X-Axis and Y-Axis signal sources to the Horizontal and Vertical Output Amplifiers. The select signals to U290 coming from Miscellaneous Display Register U540 (diagram 17) allow the System μP to switch to the various display modes (Envelope, vectors, dots, and readout). The System μP does this by writing control bits to the 1Q and 2Q output of Display Register U540 (AMP1 and AMP0 respectively) which are applied to select input SEL_B (pin 9) of U290B and to SEL_A (pin 10) of U290A.

An envelope waveform display is produced by selecting the X0 and Y0 inputs of U290 to be switched to the Output Amplifiers. The signal applied to the Horizontal Output Amplifier for YT displays is the incrementing count from the Display Counter, and it moves the electron beam horizontally across the face of the crt. In the Vertical circuitry, a sample-and-hold circuit formed by Data Selector U270A and Hold Capacitor C912 bypasses the Vertical Vector Generator circuitry. The 250 kHz signal driving the data selector, derived from the same Clock Divider circuit that supplies the $\overline{\text{SAMPLE}}$ signal (U410A and B, diagram 17), is delayed slightly by the rc combination of R607 and C900. The delay allows the analog signal at the output of the Vertical DAC to settle before the sample from Input Buffer Amplifier U170 is taken. The voltage on C912 is applied to the rc integrator made up of R165 and C166 to produce a min-max envelope with shaded vectors between the successive dots.

To produce a vector display of a waveform, the System μP selects the X1 and Y1 inputs of U290. This routes the outputs from the Vector Generators (previously described) to the Horizontal and Vertical Output Amplifiers.

For non-vector waveform displays, the X2 and Y2 inputs are routed to the outputs of U290. These signal lines, V DOTS and H DOTS, come directly from the output of the Vertical and Horizontal Input Buffers (U170 and U370B), bypassing the Vector Generators. Since the data applied to the Horizontal DAC in YT mode is from the incrementing Display Counter, the Y-Axis vertical deflections are displayed versus a linear X-Axis ramp (horizontal time axis). If XY mode is in effect, the data applied to the Horizontal DAC is the digitized waveform data used to provide the X-Axis deflection signal. In either YT mode with vectors off or XY mode, a dot waveform display is seen on the crt.

To display readout, the H READOUT and V READOUT signals at the Y3 and X3 inputs are switched to the outputs of U290. The resistive divider formed by R171 and R282 slightly decreases the amplitude of the signal from the Vertical DAC to ensure that all the Readout vertical data points are limited to eight vertical graticule divisions and will appear on screen. Operational amplifier U392B and its associated resistors perform the opposite function on the H READOUT signal from the Horizontal DAC, increasing the gain of that signal. This horizontal expansion causes the center 40 characters of a displayed readout line (out of a possible 64) to horizontally fill the screen. (See the Readout State Machine description for further details.)

Horizontal and Vertical Output Amplifiers

Operation and circuitry of the Horizontal and Vertical Output Amplifiers is nearly identical. Therefore, only the Horizontal Output Amplifier circuit operation is described.

The selected horizontal signal from U290A is applied to operational amplifier U392A configured with a variable gain set by R586. (The corresponding buffer in the Vertical Output Amplifier has a slightly different variable gain range.) Operational amplifier U392D is an inverting amplifier having a gain of about two. Horizontal offset is adjusted with R587.

The output of U392D drives the negative horizontal-deflection plate (H−) of the crt and operational amplifier U392C. Operational amplifier U392C is configured as an inverting buffer with unity gain, and its output drives the positive horizontal-deflection plate (H+).

Spot-Wobble Correction

The Spot-Wobble Correction circuit provides a dynamic correction of spot-shift on the crt caused by signal intensity changes (crt electron-beam current changes). Correction is accomplished by injecting offsetting currents that vary linearly with beam-current changes into the Vertical and Horizontal Output Amplifiers.

The beam-current control voltage is inverted by U460A and applied to one end of R583 and R584 while the other end of both potentiometers is connected to the noninverted control signal. Each potentiometer is adjusted over this "differential" range to minimize the associated spot wobble while viewing a special calibration display provided with the Extended Calibration function.

HIGH-VOLTAGE SUPPLY AND CRT

The High-Voltage Power Supply and CRT circuit (diagram 19) provides the voltage levels and control circuitry for operation of the cathode-ray tube (crt). The circuitry consists of the High-Voltage Oscillator, the High-Voltage Regulator, the +61 V Supply, the Cathode Supply, the Anode Multiplier, the DC Restorer, Focus and Z-Axis Amplifiers, the Auto Focus Buffer, the CRT, and the various CRT Control circuits.

High-Voltage Oscillator

The High-Voltage Oscillator transforms power obtained from the −15 V unregulated supply into the various ac levels necessary for the operation of the crt circuitry. The circuit consists primarily of transformer T525 and switching transistor Q628 connected in a power oscillator configuration. Sinusoidal low-voltage oscillations set up in the primary winding of T525 are raised by transformer action to high-voltage levels in the secondary windings. These ac secondary voltages are applied to the +61 V Supply, the DC Restorer, the Cathode Supply, and the Anode Multiplier circuits that provide the necessary crt operating potentials.

Oscillation occurs due to the positive feedback from the primary winding (pin 4 to pin 5) to the smaller base-drive winding (pin 3 to pin 6) used to provide base drive to switching transistor Q628. The frequency of oscillation is approximately 50 kHz and is determined primarily by the parallel resonance frequency of the transformer.

OSCILLATION START UP. Initially, when power is applied, the High-Voltage Regulator circuit detects that the crt cathode voltage is too positive and pulls pin 3 of transformer T525 negative. The negative level is applied to the base of switching transistor Q628 through the transformer winding and forward biases it. Charge begins to flow in the primary winding through the transistor collector circuit and produces a magnetic field around the transformer primary winding. The increasing magnetic field induces an in-phase voltage in the base-drive winding that further supports the base-emitter voltage bias of the transistor. This in-phase feedback causes Q628 to remain on and continue supplying energy to the parallel resonant circuit formed by the winding inductance and interwinding capacitance of the transformer. As the primary voltage peaks, then begins falling, the induced magnetic field begins to decay. This decreases the base-drive voltage through the base-connected winding and begins to turn Q628 off.

As Q628 turns off, the magnetic field around the primary winding continues to collapse, and a voltage of opposite polarity is induced in the base-drive winding. This turns the switching transistor completely off. Once again, as the magnetic field builds and then reverses, the voltage induced in the base-drive winding changes direction, forward biasing Q628. At that point, the primary winding current starts increasing again, and the switching transistor is again turned on hard by the feedback supplied to the base-drive winding. This sequence of events occurs repetitively as the circuit continues to oscillate.

The oscillating magnetic field couples power from the primary winding into the secondary windings of the transformer. The amplitudes of the voltages induced in the secondary windings are a function of the turns ratios of the transformer windings.

High-Voltage Regulator

The High-Voltage Regulator consists of U168A and associated components. It monitors the crt Cathode Supply voltage and varies the bias point of the switching transistor in the High-Voltage Oscillator to hold the Cathode Supply voltage at the nominal level. Since the output voltages at the other secondary winding taps are related by turns ratios to the Cathode Supply voltage, all voltages are held in regulation.

When the Cathode Supply voltage is at the proper level (−1900 V), the current through R263 and the 19 MΩ resistor internal to High-Voltage Module CR565 holds the voltage developed across C260 at zero volts. This is the balanced condition and sets the output of integrator U168A at a level providing correct base drive for Q628 to hold the secondary voltages at their proper levels.

If the Cathode Supply voltage level tends too positive, a slightly positive voltage will develop across C260. This voltage causes the output of integrator U168A to move negative. The negative shift charges capacitor C717 to a different level around which the induced feedback voltage at the base-drive winding will swing. The added negative bias causes Q628 to turn on earlier in the oscillation cycle, delivering more energy per cycle to the resonant transformer. The increased energy in the resonant circuit increases the secondary voltages until the Cathode Supply voltage returns to the balanced condition (zero volts across C260). Opposite action occurs should the Cathode Supply voltage tend too negative.

+61 Volt Supply

The +61 Volt Supply circuit provides power to several other circuits on the High-Voltage board. Diode CR411 provides half-wave rectification of the first-tap voltage from the secondary of T525 and stores that charge on C317. Transistor Q215, zener diode VR210 and the associated components form a buffered zener regulator. Diode CR315 protects the base-emitter junction of Q215 should a failure reverse-bias the junction. Capacitor C218 stores a relatively large charge at the regulated level and supplies operating current to the load during current surges.

Cathode Supply

The Cathode Supply circuit is composed of a voltage-doubler and an rc filter network contained within High-Voltage Module CR565. This supply produces the −1900 V accelerating potential to the CRT cathode and the −900 V slot lens voltage. The −1900 V supply is monitored by the High-Voltage Regulator to maintain the regulation of all voltages from the High-Voltage Oscillator.

The alternating voltage from pin 10 of transformer T525 (950 V peak) is applied to a conventional voltage-doubler circuit at pin 7 of the High Voltage Module. On the positive half cycle, the input capacitor of the voltage doubler (0.006 μF) is charged to −950 V through the forward-biased diode connected to ground at pin 9 of the module. The following negative half cycle adds its ac component (−950 V peak) to this stored dc value and produces a total peak voltage of −1900 V across the capacitor. This charges the 0.006 μF storage capacitor (connected across the two doubler diodes) through the second diode (now the forward-biased diode) to −1900 V. Two rc filters follow the voltage doubler to smooth out the ac ripple. A resistive voltage divider across the output of the filter network provides the −900 V slot lens potential.

Anode Multiplier

The Anode Multiplier circuit (also contained in High-Voltage Module CR565) uses voltage multiplication to produce the +14 kV CRT anode potential. Circuit operation is similar to that of the voltage-doubler circuit of the Cathode Supply.

The first negative half cycle charges the 0.001 μF input capacitor (connected to pin 8 of the High Voltage Module) to a positive peak value of +2.33 kV. The following positive half cycle adds its positive peak amplitude to the voltage stored on the input capacitor and boosts the charge on the second capacitor of the multiplier (and those following) to +4.66 kV. Following cycles continue to boost up succeeding capacitors to values +2.33 kV higher than the preceding capacitor until all six capacitors are fully charged. This places the output of the last capacitor in the multiplier at +14 kV above ground potential. Once the multiplier reaches operating potential, succeeding cycles replenish charge drawn from the Anode Multiplier by the crt beam. The 1 MΩ resistor in series with the output protects the multiplier by limiting the anode current to a safe value.

Focus Amplifier

The Focus Amplifier, in conjunction with the auto-focus circuitry, provides optimum focus of the crt beam for all settings of the front-panel INTENSITY control. The Focus Amplifier itself consists of two shunt-feedback amplifiers composed of Q145, Q152, and their associated components. The outputs of these amplifiers set the operating points of a horizontally converging quadrapole lens and a vertically converging quadrapole lens within the crt. The convergence strength of each lens is dependent on the electric field set up between the lens elements.

Since the bases of Q145 and Q152 are held at constant voltages set by their emitter potentials, changing the position of the wiper arms of the ASTIG and FOCUS pots changes the current in the base resistors, R261 and R145. This changes the feedback currents in R245 and R246 and produces different output levels from the Focus Amplifiers; that in turn, changes the convergence characteristic of the quadrapole lenses.

Initially, at the time of adjustment, the FOCUS and ASTIG potentiometers are set for optimum focus of the crt beam at low intensity. After that initial adjustment, the ASTIG pot normally remains as set, and the FOCUS control is positioned by the user as required when viewing the displays. When using the FOCUS control, transistor Q152 is controlled as described above; however, an additional current is also supplied to the base node of Q145 from the FOCUS pot through R262. This additional current varies the base-drive current to Q145 and provides tracking between the two lenses as the FOCUS control is adjusted during use of the instrument.

Auto Focus Buffer

The convergence strengths of the quadrapole lenses also dynamically track changes in the display intensity. The VQ signal, applied to the crt at pins 5 and 6, is linearly related to the VZ (intensity) signal driving the crt control grid, and increases the strength of the lenses at higher crt beam currents. (A higher beam current requires a stronger lens to cause an equal convergence of the beam.) The emitter follower Q500 buffers the VZ signal (offset 15 volts by VR316) to the first and second quadrapole lenses. A linear relationship (as opposed to the "ideal" exponential relationship) between the Z-Axis drive (VZ) and quadrapole voltage (VQ) provides adequate dynamic focusing for low to medium Z-Axis drive. The High-Drive Focus adjustment R400 sets the attenuation factor at the output of buffer Q500. Capacitors C409 and C295 compensate for the capacitive loading of the quadrapole elements.

Z-Axis Amplifier

The high-voltage, high-speed transresistance amplifier U227 produces VZ, the Z-Axis drive signal. The amplifier has two signal inputs: ZINT—a current input that determines the output voltage VZ, and $\overline{\text{ZON}}$—a TTL gating signal that causes VZ to go to its lowest value (approximately 8 V) when HI. Capacitor C139 supplies current to U227 during VZ transitions, R137 is a current limiter, and C234 is a bootstrap capacitor to speed up VZ edges.

DC Restorer

The DC Restorer provides crt control-grid bias and couples both the dc and the low-frequency components of the Z-Axis drive signal to the crt control grid. This circuit allows the Z-Axis Amplifier to control the display intensity by coupling the low-voltage Z-Axis drive signal (VZ) to the elevated crt control grid potential (about −1.9 kV). Refer to Figure 3-10 for the following description.

The DC Restorer circuit operates by clipping an ac voltage waveform at the grid bias and the Z-Axis drive levels. The shaped ac waveform is then coupled to the crt control grid through a coupling capacitor that restores the dc components of the signal.

GRID BIAS LEVEL. An ac drive voltage of approximately 300 V peak-to-peak is applied to the DC Restorer circuit from pin 7 of transformer T525. The negative half-cycle of the sinusoidal waveform is clipped by CR541, and

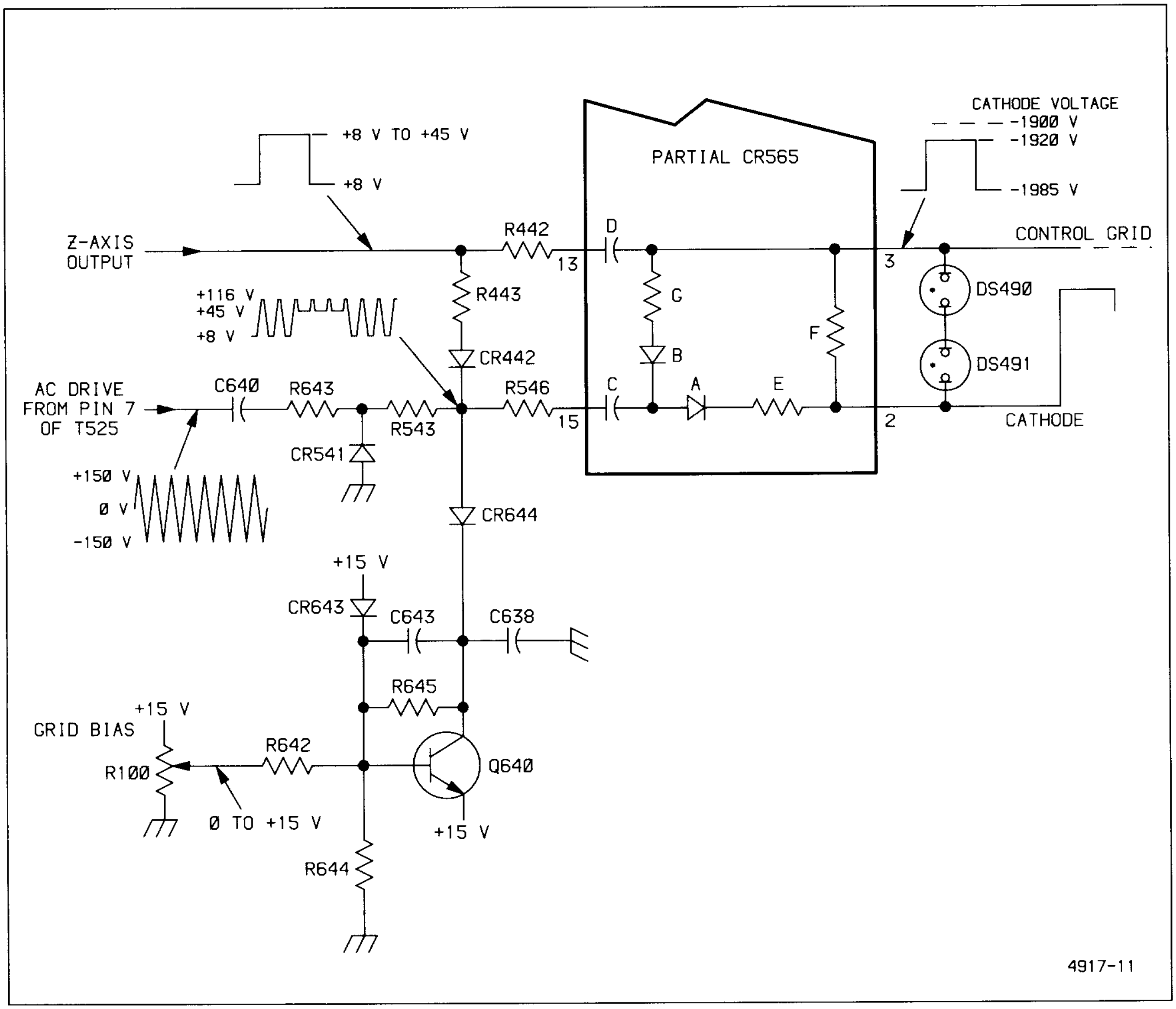


Figure 3-10. DC Restorer.

the positive half-cycle (150 V peak) is applied to the junction of CR442, CR644, and R546 via R643 and R543. Transistor Q640 and associated components form a voltage clamp circuit that limits the positive swing of the ac waveform at the junction.

Transistor Q640 is configured as a shunt-feedback amplifier with C643 and R645 as the feedback elements. The feedback current through R645 develops a voltage across the resistor that is positive with respect to the +15.6 V on the base of the transistor. The value of this additive voltage plus the diode drop across CR644 sets the clamping threshold. Grid Bias potentiometer R100 varies the voltage across base resistor divider R642 and R644 and thus sets the feedback current through R645. The adjustment range of the pot can set the nominal clamping level between +45 V and +75 V.

When the amplitude of the ac waveform is below the clamping threshold, diode CR644 will be reverse biased and the ac waveform is not clamped. During the time the diode is reverse biased, transistor Q640 is kept biased in the active region by the charge retained on C643 from the previous cycle. As the amplitude of the ac waveform at the junction of CR442 and CR644 exceeds the voltage at the collector of Q640, diode CR644 becomes forward biased, and the ac waveform is clamped at that level. Any current greater than that required to maintain the clamp voltage will be shunted to the +15 V supply by transistor Q640.

Z-AXIS DRIVE LEVEL. The variable Z-Axis signal (VZ) establishes the lower clamping level of the ac waveform applied to the High Voltage Module. When the amplitude of the waveform drops below the Z-Axis signal level, CR442 becomes forward biased, and the ac waveform is clamped to the Z-Axis signal level. The VZ level may vary between +8 V and +50 V, depending on the setting of the front-panel INTENSITY control.

The ac waveform, now carrying both the grid-bias information and the Z-Axis drive information, is applied to a DC Restorer circuit in the in the High-Voltage Module where it is lowered to the voltage level of the crt control grid (approximately −2 kV).

DC RESTORATION. The DC Restorer circuit in the High-Voltage Module is referenced to the crt cathode voltage via a connection within CR565. Capacitor C (labeling shown in Figure 3-10), connected to pin 15 of CR565, initially charges to a level determined by the difference between the Z-Axis signal level and the crt cathode potential. The Z-Axis signal sets the level on the positive plate of capacitor C through R443, CR442, and R546; the level on the negative plate is set by the crt cathode voltage through resistor E and diode A. Capacitor D is charged to a similar dc level through resistor F and R442.

When the ac waveform applied to pin 15 begins its transition from the lower clamped level (set by the Z-Axis signal) towards the upper clamped level (set by the Grid Bias potentiometer), the charge on capacitor C increases. The additional charge is proportional to the voltage difference between the two clamped voltage levels.

When the ac waveform begins its transition from the upper clamped level back to the lower clamped level, diode A becomes reverse biased. Diode B becomes forward biased, and an additional charge proportional to the negative excursion of the ac waveform (difference between the upper clamped level and the lower clamped level) is added to capacitor D through diode B and resistor G. The amount of charge added to capacitor D depends on the setting of the front-panel INTENSITY control, as it sets the lower clamping level of the ac waveform. This added charge determines the potential of the control grid with respect to the crt cathode.

The potential difference between the control grid and the cathode controls electron-beam current (the display intensity). With no Z-Axis signal applied (INTENSITY control off), capacitor D will be charged to its maximum negative value since the difference between the two clamped voltage levels is at its maximum value. This is the minimum intensity condition and reflects the setting of the Grid Bias potentiometer. During calibration, the Grid Bias pot is adjusted so that the difference between the upper clamping level (set by the Grid Bias pot) and the "no signal" level of the Z-Axis drive signal (VZ) produces a control grid bias that barely shuts off the crt electron beam.

As the INTENSITY control is advanced, the amplitude of the square-wave Z-Axis signal increases accordingly. This increased signal amplitude decreases the difference between the upper and lower clamped levels of the ac waveform, and less charge is added to capacitor D. The decreased voltage across capacitor D decreases the potential difference between the control grid and the cathode, and more crt beam current is present. Increased beam current increases the crt display intensity.

During the periods that capacitor C is charging and discharging, the control grid voltage is held stable by the long-time-constant discharge path of capacitor D through resistor F. Any charge removed from capacitor D during the positive transitions of the ac waveform will be replaced on the negative transitions.

The fast-rise and fast-fall transitions of the Z-Axis signal are coupled to the crt control grid through capacitor D. This ac-coupled fast-path signal sends the crt electron beam to the new intensity level, then the slower DC Restorer path "catches up" to handle the dc and low-frequency components of the Z-Axis drive signal.

Neon lamps DS490 and DS491 prevent arcing inside the crt by preventing the control grid and cathode from becoming too widely separated in voltage.

Other CRT Control Circuits

The CRT Control Circuits produce the voltages and current levels necessary for the crt to operate. Operational amplifier U168B, transistor Q269, and associated components form an Edge-Focus circuit that establishes the voltages for the elements of the third quadrapole lens. The positive lens element is set to its operating potential by Edge Focus adjustment pot R300 (via R393). This voltage is also divided by R278 and R277 and applied to the noninverting input of U168B to control the voltage on the other element of the third lens.

The operational amplifier and transistor of the Edge-Focus circuit are arranged as a feedback amplifier with R279 and R179 setting the stage gain. Gain of the amplifier is equal to the attenuation factor of divider network R278 and R277; so, total overall gain of the stage from the wiper of R300 to the collector of Q269 is equal to unity. The offset voltage between lens elements is set by the ratio of R279 and R179 and the +10 V reference applied to R179. This arrangement causes the two voltages applied to the third quadrapole lens to track each other over the entire range of Edge Focus adjustment R300.

Other adjustable level-setting circuits include "Orthogonality" Alignment pot R305, used to rotate the beam alignment after vertical deflection. This adjustment controls the amount of current through the Y-Axis alignment coil around the neck of the crt and is set to produce precise perpendicular alignment between the X- and Y-Axis deflections. The TRACE ROTATION adjustment pot, R1077, is a front-panel control. The effect of the adjustment is similar to the Y-Axis Alignment pot, but when adjusted, it rotates both the X-Axis and the Y-Axis deflections on the face of the crt. A final adjustable level-setting control is the Geometry pot R200, adjusted to optimize display geometry.

SYSTEM I/O

The System I/O circuits (diagram 20) provide methods of getting various types of signals or voltages into and out of the 2430. These include a GPIB interface, an XY Recorder interface, Word-Trigger interface, an audio bell, and the probe-power connectors used to supply power to active probes.

GPIB

The GPIB interface provides the 2430 with an electrical interface adherent to the IEEE 488-1980 Standard using protocols defined in the Tektronix GPIB Codes and Formats Standard.

GPIB data transfers are done under control of U630, a GPIB Controller integrated circuit. The controller automatically produces proper handshaking and data direction control. Data is transferred to and from the GPIB bus through bidirectional buffer U624. Handshaking signals are transferred to and from the GPIB bus via the handshaking bidirectional buffer, U720. Data transfers between the GPIB Controller and the System μP are through bidirectional buffer U532.

When power is first applied, the $\overline{\text{GPIBRESET}}$ signal from register U754 holds GPIB Controller U630 in its reset state. The System μP then removes the reset and begins to initialize the internal registers of the GPIB Controller. To write data into the registers, the System μP writes data to the memory-mapped addresses between 6800h and 6807h. These addresses produce a LO $\overline{\text{GPIBSEL}}$ and a LO address bit A3 applied to U332B and enable the GPIB Controller. Data is written to the internal register defined by address bits A0-A2.

The GPIB Controller is now initialized and begins watching the handshake lines on the GPIB bus, looking for a data transfer to be initiated by another GPIB device on the bus. Data transfer may also be initiated by the System μP by writing data into the GPIB Controller data register. In either case, activity on the GPIB bus follows the sequences presented in Figures 3-11 and 3-12.

When data has been read into the controller from the GPIB bus, the $\overline{\text{GPIBINT}}$ (GPIB interrupt) request is asserted, telling the System μP that GPIB data is available. To receive the data, the System μP reads the GPIB Controller internal data register, automatically resetting the interrupt request.

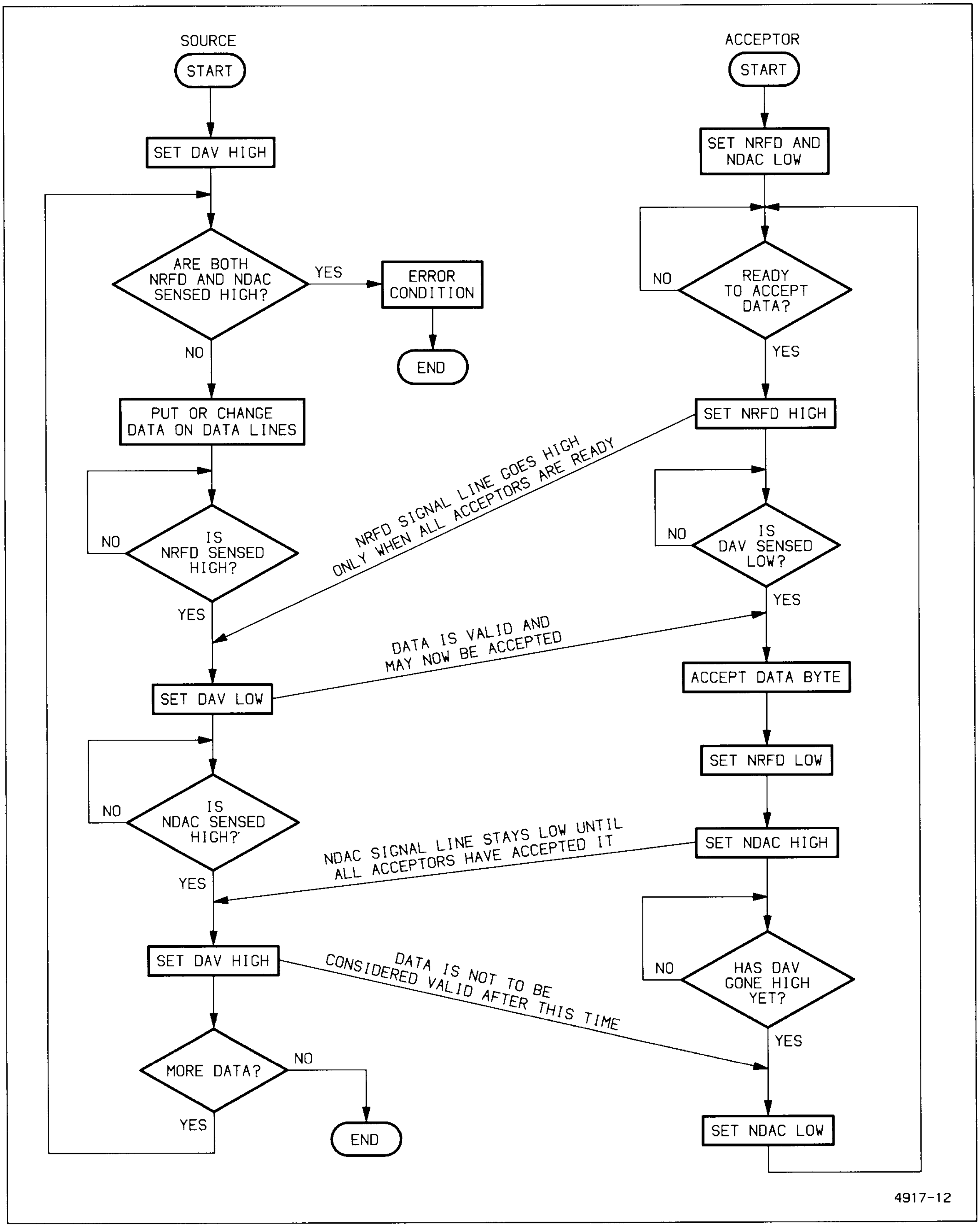


Figure 3-11. GPIB data flow diagram.

Status of the GPIB operations is displayed on the three front-panel GPIB Status LEDs. These LEDs are turned on or off by the System μP by writing three control bits into Word Probe and GPIB LED Register U754.

Information about GPIB commands and functions implemented in the 2430 may be found in Appendix A of the 2430 Operators Manual.

The GPIB may be set up to operate with a ThinkJet® printer as a listen-only device on the bus. No controller may be used, and the printer should be the only device other than the 2430 on the bus.

XY Recorder

The XY Recorder circuit allows acquired waveform data to be output to an XY plotter for producing hard copies. The XY Recorder circuit is under direct control of the System μP via Miscellaneous Register U760 (diagram 1).

Analog demultiplexer U130 is used to select and enable the data for the X and Y outputs connected to the external plotter. The $\overline{\text{XYSAMP}}$ (XY sample) bit from the Miscellaneous Register is set LO by the System μP to enable U130 when XY samples are supposed to be plotted. The $\overline{\text{XYHOME}}$ (home position) bit selects whether the plotter pen should be positioned at the "Home" position (for setting up the plot size and position) or whether it should go to the position defined by the levels from the Horizontal and Vertical DACs. "Home" position applies −2 V to both outputs, as determined by resistive divider R130-R132.

The rc networks between buffer stages of each channel (R142-C210 and R120-C120 for the vertical path, R140-C208 and R116-C118 for the horizontal) serve to smooth the voltage transitions between the step-like outputs from the DACs, resulting in a smoother plot.

The PENLIFT bit applied to Q402 is used to open and close the relay contacts of K302, and thus lift or lower the plotting pen during noncontiguous plotting. Polarity of the TTL-compatible PENLIFT signal (determining whether the pen is lifted with the relay open or closed) may be set by the operator from the plot menu to accommodate the various plotters available. (See the operators manual for the XY Plotter in use to determine the polarity requirement of the PENLIFT output signal.)

Word Trigger and GPIB Status Control Register

The Word Trigger circuit provides interface and control of the external Word Trigger Probe. Two bits from Control

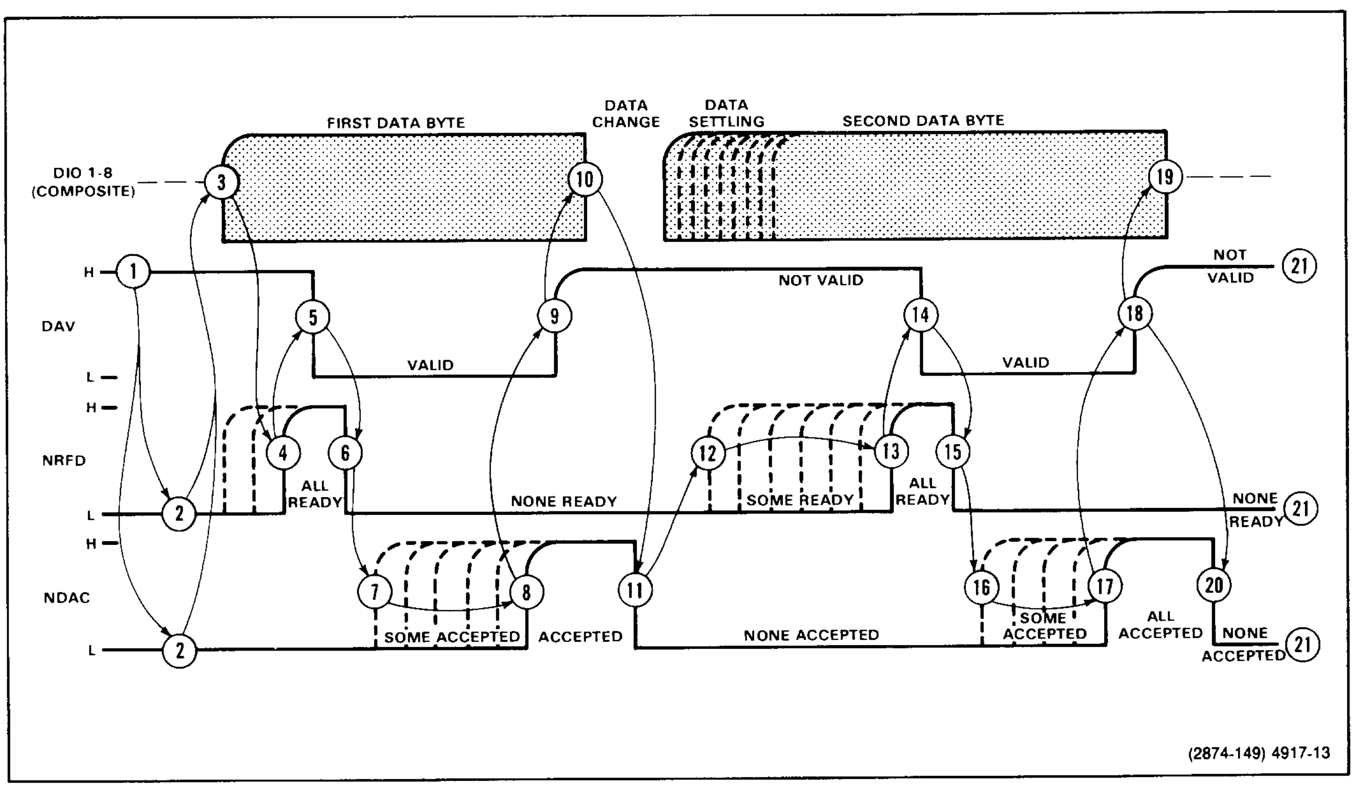


Figure 3-12. GPIB three-wire handshake state diagram.

Register U754 are used to set the recognition mode of the Word Trigger Probe. Forty bits of serial data are applied to the W DATA (word data) line and clocked into the serial shift register in the word probe by toggling the W CLOCK (word clock) line. Once loaded, the Word Trigger Probe outputs a trigger pulse each time (and as long as) the set conditions are met.

The $\overline{\text{WDTTL}}$ output is applied to the trigger circuits of the 2430 where, if selected as the trigger source, it produces a scope trigger event. The trigger signal is buffered to the rear panel by U844D, Q720, and the associated components. Output levels are TTL compatible, with the maximum HI level being set by R716 and VR717. Output impedances are 47 ohms LO and 227 ohms HI. Diode CR722, zener VR717, and resistors R717 and R718 provide protection of the output circuit should an out-of-range voltage be applied to the output connector.

The remaining inputs and outputs of Control Register U754 are used to control the GPIB Status LEDs and to reset GPIB Controller U630.

Bell

The Bell circuit allows the 2430 to produce an audio tone to draw the operator's attention to certain warning and error conditions. The circuit consists of a free-running oscillator whose signal is gated through the output speaker.

The oscillator consists of timer U274, configured as an astable multivibrator (oscillator), and output transistor Q594, used to buffer the oscillator output. Current flowing in R274 and R276 charges C372 up until it crosses the trigger level at pin 2 of U274. This sets the output applied to the base of Q594 LO, turning the transistor off, and sets the discharge output at pin 7 to ground potential. Capacitor C372 now discharges through R276 until the threshold level at pin 6 is reached, at which time the output at pin 3 goes HI and the discharge pin goes to a high-impedance state. Capacitor C372 begins to charge through R274 and R276 again, completing the cycle. The cycle continues as long as instrument power is applied, alternately turning Q594 off and on with an approximate 50% duty cycle.

The BELL line from the Miscellaneous Register (U760, diagram 1) is used to gate this oscillator signal through the speaker to produce the audio output. As long as BELL is LO, transistors Q596, Q558, and Q592 are off, and current is cut off to speaker LS498.

When BELL goes HI, transistor Q596 turns on, which in turn, turns on Q588. With Q588 on, the base of Darlington transistor Q592 is pulled HI. Now, whenever the oscillator transistor Q594 is on, proper biasing conditions for Q592 are established and current flows from the $+5\ V_D$ supply to ground through Darlington Q592, the speaker LS498, and transistor Q594. When Q594 turns off, current flow is interrupted until the oscillator turns Q594 back on.

Since LS498 is inductive, the current decay portion of its cycle (Q594 off) tends to force pin 1 of the speaker above the $+5\ V_D$ supply level. Diode CR594 becomes forward biased in this case and shunts the decay current back to the $+5\ V_D$ supply, protecting transistor Q594 from overvoltage conditions.

As long as the BELL line remains HI, the speaker produces an approximate 2 kHz tone. In practice, the System μP sets the BELL line HI for a short time ($\simeq$4 ms), turning Q588 on, starting the tone and rapidly charging C590. When BELL returns LO, C590 gradually discharges through R594. As the capacitor discharges, bias on Q592, and thus current through the speaker, is reduced, causing the sound to gradually fade out in a pleasing "bell-like" tone.

Probe Power

The Probe Power outputs on the rear panel provide access to three of the instrument power-supply voltages and may be used to power approved voltage- and current-probe accessories. Contact your Tektronix sales representative for a list of approved probe accessories.

Video Option Control Register

The Video Option Control Register (U750 on diagram 20) is written to by the System Processor (address-decoded location 6012h) to control operational setup of the Video Option. The Video Option Control Register is initialized on power-up and provides for control of the following functions:

1. Selection of trigger field (Field1 or Field2).

2. Choice of triggering on positive- or negative-sync input signals (NEG-SYNC).

3. Selection of correct polarity of the offset signal via the CH2 INV signal.

4. Control of the display functions (TV CLAMP and FAST CLAMP).

5. Enabling the TV Trigger circuit to trigger the scope.

6. Selection of TV Line Coupling—allowing all lines to produce a trigger signal to the main Trigger circuit of the 2430.

VIDEO OPTION

The Video Option (diagram 21) consists of additional hardware and firmware installed in the host instrument to enhance triggering on and viewing of composite video signals. The Video Option block diagram located in the tabbed foldout pages in the rear of the manual may be an aid in following the Video Option circuit descriptions.

The Video Option circuitry contains both video-signal processing and trigger-generation circuits. The video-signal processing circuits stabilize the input signal and separate the television synchronization signals (horizontal and vertical sync pulses) from the composite video signal. The trigger-generation circuits then count these separated sync pulses to determine when a TV Trigger signal is to be produced.

In the video-signal processing circuits, the gain of the AGC (automatic gain control) Amplifier is automatically adjusted to produce the correct signal amplitude to the Sync Pickoff Comparator for proper sync separation over a wide range of input signal levels. The Trigger Back-Porch Clamp adjusts the back-porch level of the input signal through the Fixed-Gain Amplifier on each sync pulse. The feedback to the Fixed Gain Amplifier compensates for level shifting caused by any power-line ripple riding on the composite video signal. The Sync-Tip Clamp circuit monitors the horizontal-sync pulse amplitude and produces the automatic-gain-control voltage that sets the gain of the AGC Amplifier. Sync pulses are separated from the composite video signal by the Sync Pickoff Comparator. The horizontal- and vertical-sync pulses are further separated by the Pulse Stretcher and Field Generator circuits for use in producing the horizontal clock and field-sync signals needed by the Trigger Generation circuitry.

To set up the Video Option operating modes, the System Processor writes control settings to the TV Control Register (diagram 20) in the System I/O circuitry. The latched setting in the register is held until a different mode is needed. Programmable counters, also under System processor control, count the extracted horizontal sync pulses (lines) until the line number for the selected trigger point is reached. At that point, if the main trigger circuit is finished with holdoff, the TV Trigger Generator circuit produces a TV Trigger to the A/B Trigger Generator to trigger the next storage acquisition.

An additional display function added to Channel 2 is the TV CLAMP feature. When enabled, the circuitry holds the back-porch level of the displayed signal on Channel 2 at ground level. The Channel 2 Vertical Display Clamp circuit checks the back-porch levels of the incoming TV signal on Channel 2 and produces offsetting voltages to the Channel 2 Preamplifier to bring those levels back to ground reference. The circuit action produces a stable vertical signal display of a TV signal by removing power supply ripple that may be present. Either inverted or noninverted signals may be displayed with the TV CLAMP feature.

Video Signal Processing Circuitry

AGC AMPLIFIER. The AGC (automatic gain control) Amplifier, Q514, U612, and U710B, amplifies the composite-video input signal from the selected trigger channel. Stage gain is controlled by feedback that is derived from the amplitude of the incoming horizontal sync pulses. The amplifier itself is formed by two cross-connected differential amplifier pairs in U612 that permit normal or inverted amplification of the signal. The front-panel SLOPE/SYNC switch selects whether the amplifier is inverting or noninverting to match the required signal polarity for the sync-separation circuits. For correct operation of the sync separation circuit, the composite-video signal must be sync-negative; therefore, if a "noninverted" signal display has positive sync, the SLOPE/SYNC switch may be pressed to invert the signal (+ SLOPE LED is on for positive-sync input display). Inversion only occurs in the trigger Sync Separator path; the display polarity remains unaffected.

Gain of the AGC Amplifier is controlled by the action of the Trigger Back-Porch Clamp, the Sync-Tip Clamp, and the Automatic Gain-Control circuitry working together to set the channel resistance of FET Q514 and thereby the gain of AGC Amplifier U612. Amplifier gain is automatically adjusted to maintain the sync-tip level at a known point relative to the back-porch amplitude of the signal. This action provides an accurate and stable pickoff point on the signal to the Sync Pickoff Comparator circuit (Q504 and Q510) with input video signals of different or varying amplitudes. The minimum gain of the circuit is decreased (to permits the application of higher amplitude signals) by the use of constant-current diodes CR526 and CR620 as the current sources for the differential amplifiers.

When power is first applied, the operating level of the AGC Amplifier is established by feedback only. With no signal applied, the channel resistance of Q514 is minimum, setting the gain of the AGC Amplifier to maximum. With maximum gain and no signal, the feedback loops of the Back-Porch Clamp and the Sync-Tip Clamp set the circuit gain as if an average "ground" signal were being received.

The composite-video input signal is applied to one input of the differential AGC Amplifier at pin 3 of U612 and to Dc-Offset Amplifier U710B via a low-pass filter composed of R714 and C714. The low-pass filter averages the signal at the input of U710B so that only the average (dc) signal level appears at the output of U710B and on pin 11 of U612. Since the input signal swings about this average level, the AGC Amplifier output signal will be centered in its linear amplification region.

The base-emitter bias of the differential output transistors within U612 are controlled by the NEG-SYNC signal from Video Option Control Register U750 (diagram 20). When the NEG-SYNC bin is set HI, the transistors connected to pins 2 and 9 will be biased on, with those at pins 6 and 13 biased off. When NEG-SYNC is set LO, the conducting transistors are switched, and the polarity of the output signal driving transistor Q612 is inverted. Common-base transistor Q612 level shifts the output signal from the AGC Amplifier and provides voltage gain to drive U610D.

FIXED GAIN AMPLIFIER. The Fixed Gain Amplifier circuit, formed by U610A, B, and C, Q502, and U710C, provides additional gain to the video signal from the AGC Amplifier. The Trigger Back-Porch Clamp circuit monitors the back-porch level of the resulting signal and injects an offsetting dc level into the Fixed Gain Amplifier via U710C to shift that level to approximately +4.5 V.

Emitter-follower U610D drives one input of a differential amplifier made up of U610A and U610B, while the other input is driven by the output signal of U710C. Transistor U610C and its associated components form the current source for the amplifier. The collector output of U610B drives the input of the Sync Pickoff Comparator.

Transistor Q502 and its associated circuitry act as a start-up circuit that monitors the dc output level of U610B and applies an offset voltage to pin 10 of U710C should that level go below zero volts. This occurs when going from a "no-signal" or low-signal condition to a strong signal. If the dc output level goes below ground, diode CR612 will become forward biased, shutting off Q502. With Q502 off, the −15 V supply applied via resistor R506 will forward bias CR606 to charge C713 negatively. This pulls the output voltage of U710C negative and decreases base drive to U610B. Reducing base drive reduces the collector current so that the collector voltage of U610B returns positive until the above zero-volt output level is restored and CR612 becomes biased off.

SYNC PICKOFF COMPARATOR. The Sync-Pickoff Comparator, composed of Q504 and Q510, switches when the amplitude of a sync pulse crosses the comparator threshold level. The switching threshold is set by the biasing resistors of Q510, R408 and R409, to about 50% of the sync level to eliminate any video information. The output signal from the collector of Q510 is the composite of all detected sync pulses, and the output of Q504 is an inverted replica of that signal.

SYNC-TIP CLAMP AND AUTOMATIC GAIN CONTROL. Transconductance Amplifier U510, in conjunction with the AGC Amplifier, is used to clamp the sync-tip level. Amplifier U510 is enabled by the bias current supplied by Q512 when sync tips turn that transistor on. This amplifier acts as a weak operational amplifier to set the sync-tip level constant when Q512 is conducting to supply bias current to pin 5 of U510.

The Sync-Tip Clamp holds the negative-sync tips at about +0.5 V, so the resulting sync pulses are approximately 4 V in amplitude. Anytime the negative-sync tips at the collector of U610B go below about +0.5 V, input pin 3 of U510 will go below the ground reference at the other input. This causes the output of U510 to go low when enabled, and C512 begins discharging slowly toward −15 V. This decreasing voltage is applied to the gate of FET Q514 to increase the channel resistance and decrease the gain of the AGC Amplifier. Since U510 is a transconductance amplifier, it can change the voltage across C514 only a small amount during each sync pulse, and a few horizontal-line cycles are needed to reduce the gain of the AGC Amplifier to the new operating level. Between sync tips, when amplifier U510 is disabled, the long time constant of R610 and C512 holds the bias for Q514 (and thus gain of the AGC Amplifier) nearly constant.

Diode CR502 acts to reduce AGC Amplifier gain quickly if the negative-sync-tip amplitude at the collector of U610B drops below −0.8 V. If the diode becomes forward biased, as it might should the signal amplitude go suddenly negative, Q510 will be turned on for a longer time until the signal amplitude returns to a lower level. Amplifier U510 can then increase the channel resistance of Q514 more quickly to reduce gain of the AGC Amplifier and return the sync-tip amplitude to the correct level.

TRIGGER BACK-PORCH CLAMP. The Trigger Back-Porch Clamp circuit formed by U504, U410A, and associated components, is enabled for a short time during each horizontal-sync pulse immediately following the sync tip (during the back-porch time). The output of the Trigger Back-Porch Clamp is used to hold the back-porch level of the composite-video signal to a predetermined dc level. This, in combination with the action of the Sync-Tip Clamp, produces sync pulses that are approximately 4 V in amplitude.

Transconductance Amplifier U504 is enabled by turning transistor U410A off on the falling (trailing) edge of the inverted sync pulse from Q504 (via C308). Bias current to turn on U504 is then supplied through R403. The amplifier will stay enabled until the current supplied by resistor R214 charges C308 back positive enough to bias U410A back on (in approximately 1 μs). During the time that U504 is enabled, it senses the back-porch level of the composite-video waveform applied to pin 3 via resistive divider R613, R602, and R604. Depending on whether the sensed level is above or below the ground reference level on pin 2, the amplifier output will either charge or discharge capacitor C713 to a new voltage level. This will slightly change the offset voltage applied to pin 4 of U610B (via U710C), shifting the entire composite-video waveform in the direction required to hold the back-porch level at +4.5 volts (zero volts on pin 3 of U504). During the period between back porches, C713 acts as a hold capacitor to maintain the offset bias on U610B.

PULSE STRETCHER. The Pulse Stretcher lengthens the horizontal-sync pulse width to produce a more symmetrical, faster rise-time clocking pulse. It also removes alternate equalizing and serrated pulses that occur during the NTSC TV signal vertical-sync block from the composite-sync waveform in order to maintain the correct horizontal clock rate.

Transistors U420B, U420C, and associated components form a monostable multivibrator used to stretch the width of the horizontal-sync pulses. The leading edge of each horizontal-sync pulse turns on U420C which, in turn, reverse biases diode CR224 via C325 to turn off U420B. The resulting HI at the collector of U420B keeps U420C biased on (via R421). The output at the collector of U420B remains HI until C325 charges to about +1 volt via R224; then, CR224 becomes forward biased to once again turn U420B on. The collector voltage of transistor U420B then drops to about +0.4 V, at which point diode CR329 conducts to clamp the output at one diode drop above ground. This stretched output pulse from the monostable multivibrator is level-shifted down one diode drop through CR328 to produce the TTL-compatible HORIZCLK signal used to generate trigger signals to the main Trigger circuit of the oscilloscope.

Since the equalizing and serration pulses in the vertical-sync block occur at twice the horizontal-sync rate (see Figures 3-13 and 3-14), every other one must be prevented from triggering the monostable multivibrator to keep the line count correct. The DLY'D HCLK (delayed Horizontal clock) applied to the base of U420B (via R210) holds that transistor on for a period of time between the normal horizontal line-sync pulses. This action effectively removes the unwanted pulses from the HORIZCLK output by preventing them from triggering the multivibrator circuit.

CLOCK FREE RUN. If non-NTSC standard television signals are being used, the vertical-sync block may not be serrated. To maintain the proper horizontal-sync rate during the absence of signal-supplied horizontal pulses, the Clock Free-Run circuit produces "artificial" clock pulses. Therefore, the line count will continue and be correct when the next horizontal-sync pulse does arrive. The signal used as the self-generated HORIZCLK signal is derived from the VCO (voltage-controlled oscillator) output (2XH) of the Phase-Locked Loop circuit. That signal, at twice the horizontal-sync rate, is divided by two at the Q output of flip-flop U220B. It is then wire-ORed into the HORIZCLK signal line via R334 and CR332. If a horizontal-sync pulse is not present to trigger the monostable multivibrator, CR332 will be biased on by the HI HCLK to pass that pulse to the HORIZCLK signal line. When the Phase-Locked Loop (PLL) circuit is locked (synchronized) with the incoming horizontal sync, the HCLK rising edge will slightly lag the incoming sync pulse to prevent jitter of the HORIZCLK signal to U524B.

PHASE-LOCKED LOOP (PLL). Phase-Locked Loop U314 locks onto the horizontal-sync signal to produce a synchronized clock at twice the horizontal-sync rate (2XH). The 2XH clock is used to extract the various sync- and field-identification signals from the composite-sync waveform. It is also divided and delayed to obtain the DLY'D HCLK (see Figure 3-13) signal used in eliminating alternate equalizing and serration pulses from the HORIZCLK signal and the input to the PLL Phase Comparator inputs.

The 2XH VCO (voltage-controlled oscillator) output is divided by two by flip-flop U220B to produce both the HCLK and $\overline{\text{HORIZCLK}}$ signals at the horizontal-line rate. Horizontal sync from the input signal is applied to the Phase Comparator input of U314 at pin 14 via U308B. The $\overline{\text{HORIZCLK}}$ from the $\overline{\text{Q}}$ output of U220B is applied to U314 at pin 3 through U308C.

Phase Comparator output 2 (PC2 OUT at pin 13) of PLL U314, outputs the PLL ERROR signal whenever the leading edges of the $\overline{\text{HORIZCLK}}$ signal on pin 3 and the horizontal-sync pulses on pin 14 do not coincide. The error signal output is integrated by R322, R320, and C322 to produce a voltage (applied to pin 9) used to correct the operating frequency of the VCO. When either no phase errors exist or no signals are present to compare (both phase-comparator inputs at the same level), pin 13 goes to a high-impedance state, and the voltage on C322 maintains the operating frequency of the VCO. Resistors R323 and R324 and capacitor C324 set the operating frequency range of the PLL circuit. A bleeder resistor, R327, reduces the charge on C322 slightly between each error signal output so that the $\overline{\text{HORIZCLK}}$ signal will always lag the horizontal-sync of the input signal by a small amount. This

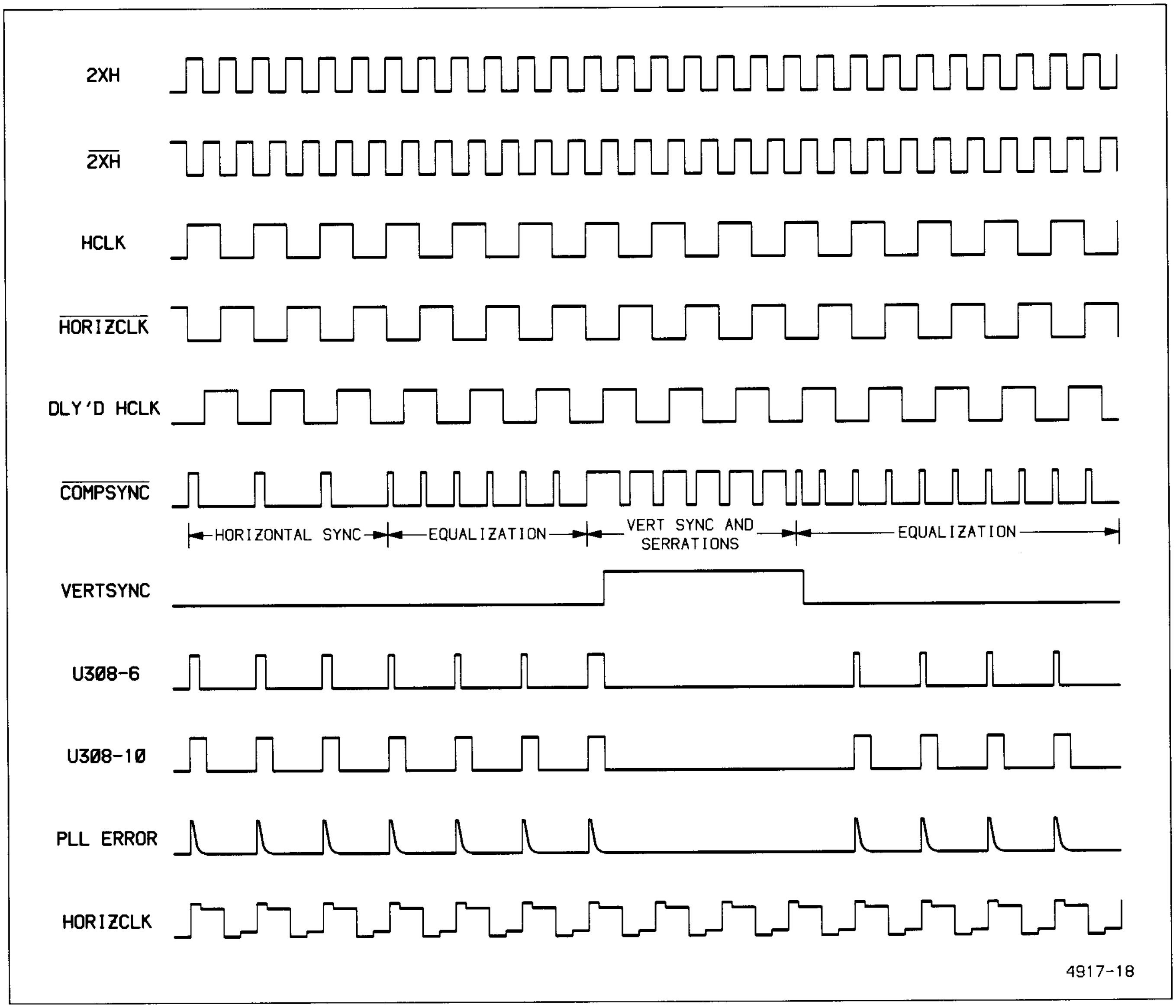


Figure 3-13. Video Option waveforms.

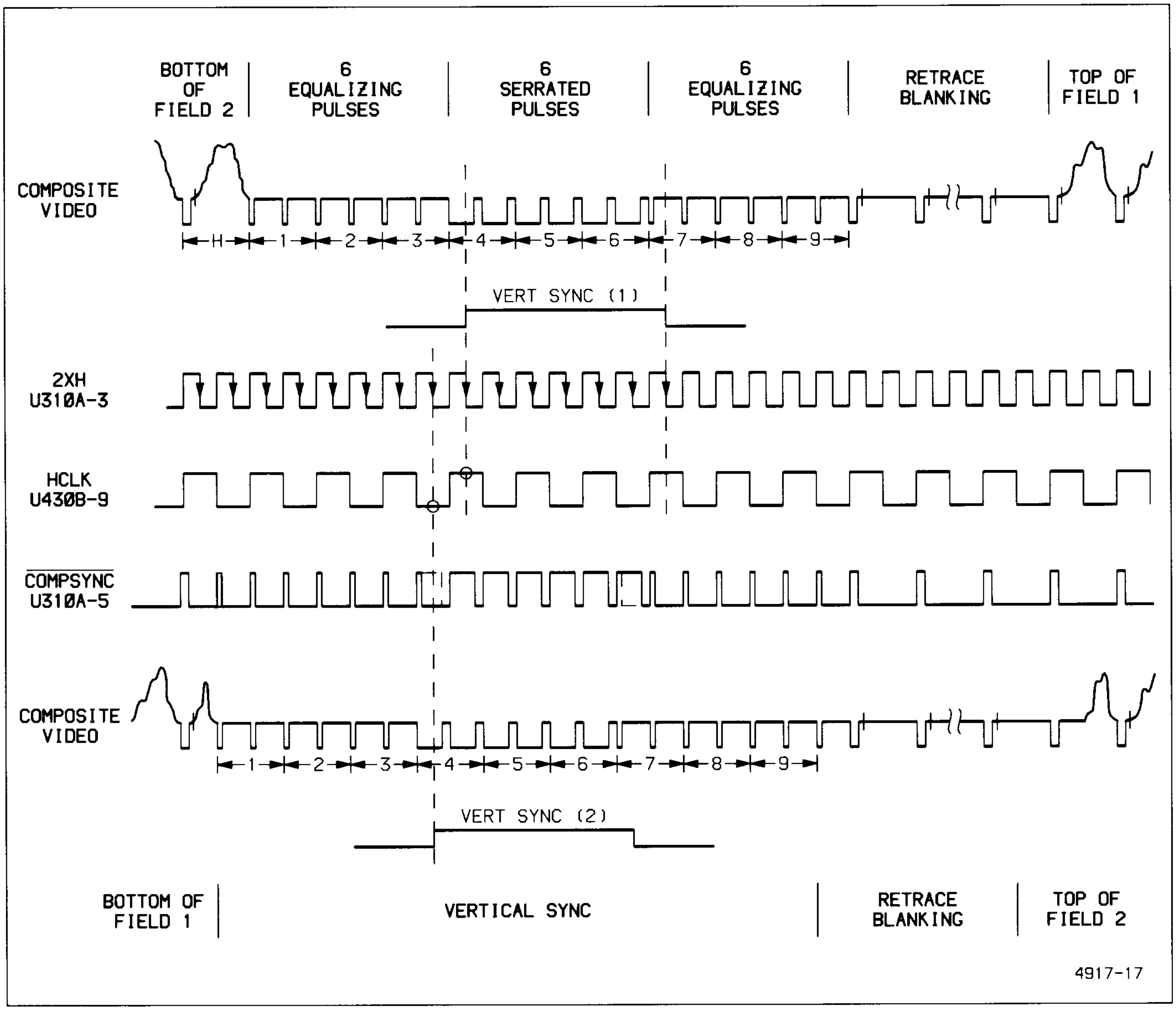


Figure 3-14. Video Option field-sync identification.

slight lag prevents the possibility of jitter in the HORIZCLK signal going to clock TV Trigger flip-flop U524B.

A similar signal (PLL LOCK) from pin 1 of the Phase Comparator is integrated by R326 and C330. If the PLL is not locked onto the input signal, the PLL LOCK output remains in the LO state long enough to be sensed by the PLL Unlock Detector. The long LO state of the PLL LOCK signal discharges C330 negative enough with respect to the emitter voltage of Q330, that the transistor becomes biased on. The collector voltage of Q330 will then go high, and Vertical Sync flip-flop U310A and Delayed Horizontal Clock flip-flop U220A will both be reset by the HI UNLOCKED signal. With U220A and U310A both reset, the DLY'D HCLK and VERTSYNC signals are held LO, and the equalizing pulses and vertical-sync serrations are no longer prevented from passing through NOR-gate U308B. The PLL Phase Comparator then sees the entire input signal during attempts to lock on so that locking will occur in the proper range. While the unlocked condition exists, the Channel 2 Vertical Display Clamp circuit is held disabled (via R328) by the HI state of $\overline{\text{TVCLAMP}}$ to prevent an invalid offset from being sent to the Channel 2 Vertical Preamplifier.

When lock is achieved, the phase difference between the two input signals becomes very small. The PLL LOCK pulse output level remains in the HI state (no error) long enough that C330 is allowed to charge positive and turn off transistor Q330. UNLOCK then goes LO to remove the resets from flip-flops U310A and U220A, allowing them operate, and $\overline{\text{TVCLAMP}}$ goes LO to enable the Channel 2 Vertical Display Clamp circuit. Unwanted equalizing pulses and the vertical-sync serrations are now prevented from passing to PLL Phase Comparator inputs by the DLY'D HCLK (delayed horizontal clock) and VERTSYNC signals applied to the PLL Phase Comparator Input NOR-gates, U308B and U308C (see Figure 3-13).

The DLY'D HCLK is shifted one-quarter HCLK cycle. When the DLY'D HCLK is HI, the outputs of both NOR-gates at the inputs to the PLL Phase Comparator are held LO, and the alternate equalizing pulses of composite-sync signal are prevented from passing to the PLL Phase Comparator. The vertical-sync serrations are prevented from passing through NOR-gate U308B by the HI VERTSYNC signal applied during vertical-sync times. Both types of unwanted pulses are thereby eliminated from the Phase Comparator inputs. The remaining sync pulses to be compared with the $\overline{\text{HORIZCLK}}$ signal are then only at the horizontal-sync frequency, and the VCO output frequency shifts slightly as necessary to bring that frequency to precisely twice the horizontal-sync rate (2XH). The charge on capacitor C322 holds the VCO to that output frequency throughout the vertical-sync period when all serration pulses are disabled from the Phase Comparator input and no comparisons are being made.

DELAYED HORIZONTAL CLOCK. The Delayed Horizontal Clock (DLY'D HCLK) is used to remove alternate equalizing pulses and serration pulses from the composite-sync waveform in order to maintain precise sync for horizontal line counting. The PLL-generated HCLK signal from the Q output of U220B is clocked into U220A by the $\overline{\text{2XH}}$ pulse from NOR-gate U308A (acting as an inverter). The inversion of the two-times clock delays the Q output of flip-flop U220A by one-quarter of a horizontal clock (HCLK) cycle. The quarter-cycle delay enables the HI portion of the output (applied to U420B via R210) to mask the alternate, unwanted equalization and serration pulses (occurring at twice the horizontal-sync rate) from the HORIZCLK output by preventing U420B, in the Pulse Stretcher circuit, from switching during those time periods. The same signal masks the unwanted equalization pulses from the PLL inputs by disabling NOR-gates U308B and U308C from passing signals to compare during the DLY'D HCLK HI state. All the vertical-sync serration pulses are eliminated from the PLL Phase Comparator input by the HI state of the VERTSYNC signal applied to the input NOR-gates.

VERTICAL SYNC. The Vertical Sync circuitry outputs pulses for both the Field 1 and the Field 2 vertical-sync times. These VERTSYNC pulses are used to toggle the Field Sync Generator. The VERTSYNC signal is produced by clocking the level of the $\overline{\text{COMPSYNC}}$ signal on the D input (pin 5) of U310A into that flip-flop using the inverted two-times horizontal clock $\overline{\text{2XH}}$. Figure 3-14 shows that only during a vertical-sync interval will the $\overline{\text{COMPSYNC}}$ signal be HI on the rising edge of the $\overline{\text{2XH}}$ clock. At all other (non-vertical sync) times, the $\overline{\text{COMPSYNC}}$ signal will be LO on the rising edge of the 2XH clock. Thus, the Q output of flip-flop U310A will be clocked HI during vertical-sync intervals for VERTSYNC, and it will be clocked LO during the rest of the field.

FIELD-SYNC GENERATOR. The Field-Sync Generator produces the FIELD signal used in identifying the individual fields of picture information. For interlaced-scan signals, the signal identifies which field a given line of picture information belongs to (exceptions are explained in the Line Counter description); while, for non-interlaced-scan signals, it toggles to indicate vertical sync. The circuit consists of an Interlace/non-Interlace Detector, a Vertical-Sync Latch (interlaced), and a Vertical-Sync flip-flop (non-interlaced).

To detect whether a signal is interlaced (two vertical-sync pulses per frame) or non-interlaced (only one vertical-sync pulse per frame), flip-flop U310B is clocked to transfer the level of the HCLK signal on the D input to the $\overline{Q}$ output by the VERTSYNC clock at the start of a vertical-sync period. For non-interlaced displays, the vertical-sync rising edge always occurs during a HI portion of the HCLK signal, and the $\overline{Q}$ output of U310B will be clocked HI; while, for interlaced displays, the $\overline{Q}$ output will alternate between HI and LO.

The $\overline{Q}$ from pin 12 of U310B controls two other flip-flops U430A and U430B, through the circuit action of transistors U420A and Q422. If the output of U310B is not toggling (non-interlaced signals), transistor U420A will be turned off by pull-down resistor R426. This allows the base bias voltage of Q422 to go positive as C426 charges through R429 and R428. Soon, Q422 is biased off and flip-flop U430B becomes reset. The reset on U430B from C426 holds the $\overline{Q}$ output HI to reverse bias CR334 and isolate the $\overline{Q}$ output from the FIELD signal line. At the same time, the LO TVINTERLACED signal applied to the set input of U430A from the collector of Q422 enables that flip-flop to toggle on the rising edges of the vertical-sync pulses applied to the clock input (pin 3). This toggling is required to reinitialize the counters after they have counted their last lines. The TVINTERLACED signal is also applied to the Processor Miscellaneous Buffer (U854, diagram 1) where it may be read by the System μP to determine whether the video signal is interlaced or non-interlaced. The System μP must be able to determine this information to properly control the line counting.

For interlaced displays, the output from U310B will toggle. This will alternately turn transistor U420A on and off at the vertical-field rate. The first time U420A gets turned on by an interlaced-system signal, it discharges C426 and turns Q422 on. Capacitor C426 will charge positive through R429 and R428 when U420A turns off, but the long time constant of the charging path prevents the charge from getting positive enough to reassert the reset to U430B before the next toggle cycle once again discharges the capacitor. Flip-flop U430A is held set by the HI TVINTERLACED (interlaced) signal asserted from the collector of Q422, and CR336 is reverse biased to isolate U430A from the FIELD signal line. The resulting FIELD signal, as a result of the output of flip-flop U430B, will be HI for all lines in Field 1 and LO for all lines in Field 2 (with a few exceptions that are explained in the Line Counters description).

LINE COUNTERS. Line Counter U530 contains three programmable counters (at decoded addresses 6808h through 680Fh) that are set by the System Processor to determine when the chosen line number in the field selected for triggering is reached. The various control registers of the counter are set up to count horizontal clock pulses (lines) to determine line location in the field.

The Line Counter is enabled whenever its address block is decoded by the system Address Decode circuitry. To differentiate it from the GPIB circuitry (which also answers for the same block of decoded addresses), the Video Option uses address bit A3 as a second chip select. Specific registers within the Line Counter are addressed using address lines A0-A2 applied to the register-select inputs. Reading and writing of the selected register is controlled by the System μP using the $\overline{WR}$ select line while the E (enable) clock synchronizes transfers to the System μP rate.

Once the proper setup data (defining counter mode and line number) is written to the Line Counter, the enabled counter will begin counting horizontal clock pulses (lines). Counters are alternately started as the FIELD signal toggles, and counters 1 and 2 produce a LO output when their predefined counts are reached. Counter 3 is used to determine the number of LINES in a FIELD (of FIELD 2 if in an interlaced system). The System μP checks the "previous field" line count by reading the counter contents via the data bus.

LINE COUNT ADJUSTMENTS. Depending on the type of signal being triggered upon (System M or non-System M) and the desired line for trigger, the System μP adjusts both the numbers preloaded to the counters and the field to which the assigned line-count relates. These line-count and relative-field adjustments are required for the following reasons.

1. The HORIZCLK coincident with a switch in the FIELD indicator does not produce a count. Since the FIELD change doesn't enable the opposite counter in time to catch the rising edge of the HORIZCLK (responsible for the change), the preloaded line count must be reduced by one.

2. The counters cannot produce a "zero-count" delay; i.e., the counter output goes LO one count (line) after the counter reaches zero. Even when set to zero, a count must still occur; so the line count must be reduced by one again.

3. The counter outputs merely arm the trigger circuit, with the next line sync producing the actual trigger; therefore, line count must be reduced again by one.

RELATIVE FIELD ADJUSTMENTS. For non-System M television signals (line one coincident with the FIELD sync pulse), the line-adjustment requirements described above require that the first three lines of either field be counted relative to the previous FIELD pulse.

Since, by definition, System-M fields begin numbering lines three lines before the vertical field-sync occurs, and due to the line-adjustment requirements described above, the first six lines of System-M fields must be counted relative to the previous FIELD pulse.

As stated in the "Line Count Adjustments," the trigger arming pulse occurs one line count prior to reaching the selected trigger line. Depending on whether the System Processor has selected the arming pulse relative to Field 1 or Field 2, either NAND-gate U541C or NAND-gate U541D will be enabled by a control bit (FLD1 or FLD2) from Video Option Control Register U750. The selected pulse, when it occurs, is passed through the enabled gate, through U541A and U424D, and appears as a clock pulse at the trigger-arm flip-flop, U524A.

TV TRIGGER GENERATOR. The TV Trigger Generator circuit produces the signal to trigger the Oscilloscope at the designated horizontal line. The output from the Line Counter arms the TV Trigger Generator circuit, enabling a trigger to be produced on the next line-sync pulse. Generation of a TV trigger from the circuit is enabled by a HI TVENA (TV-enable) bit from Video Option Control Register U750 (diagram 20).

In the Video Option, as in the main Trigger Generator a trigger signal is inhibited from being produced during trigger holdoff. For the holdoff period, the ATHO (A-trigger holdoff) signal applied to U424C is HI to hold arming flip-flop U524A reset which, in turn, holds trigger flip-flop U524A reset. When the holdoff processing cycle is completed, the ATHO signal goes LO to remove the reset from U524A and enable triggering.

Assuming TV Line Coupling mode is not active, the LINECPL (line coupling) bit applied to U541B pin 5 will be LO, and arming flip-flop U524A will be enabled. When the Line Counter has counted the proper number of lines relative to the Processor-selected field, flip-flop U524A will be clocked. This produces a HI "armed" level applied to the reset input of trigger flip-flop U524A that releases the reset condition of the flip-flop. The next HORIZCLK pulse (line) then clocks a LO to the $\overline{Q}$ output, $\overline{TVTG}$, that defines the trigger point in the acquisition record. The $\overline{TVTG}$ output is reset HI when trigger holdoff (ATHO) goes HI to reset the flip-flop via U424C and U524A.

When TV Line Coupling mode is selected, the LINECPL bit from the Video Option Control Register will be set HI. This causes flip-flop U524A to be immediately armed when A trigger holdoff ends by forcing a set signal to pin 4 of that flip-flop through NAND-gate U541B. In this mode, a trigger will occur on the first line sync following the end of each holdoff interval. The resulting display will be stable with respect to horizontal sync pulses but will not be stable with respect to the vertical sync pulses.

CH2 VERTICAL DISPLAY CLAMP. The Channel 2 Display Clamp circuit clamps the back-porch level of the triggered-display signal near the on-screen zero-volt reference. This allows automatic positioning of the display on the crt when probing various points with differing dc levels and removes vertical jitter that would be caused by 60-Hz hum riding on the television signal.

The Channel 2 Pickoff (CH2 PO) signal from the Channel 2 Preamplifier is applied through a low-pass filter formed by R524 and C514. The filter removes all the high-frequency components from the composite video signal, but its purpose is to specifically remove the color-burst modulation from the back-porch of the sync pulses. The filtered sync pulse is then amplified with respect to ground during its back-porch interval either by operational amplifier U514 or by operational amplifier U520, depending on the display polarity chosen by the operator. The selected comparator, when gated on (via U410A and either R410 or R411) during the back-porch interval, produces a dc-offset voltage used to shift the back-porch level of the displayed channel 2 signal to zero volts. Capacitor C522 acts as a hold capacitor to maintain a constant dc offset to the Channel 2 Vertical Preamplifier between back-porch samples. Operational amplifier U710D buffers the offset signal to the Channel 2 Preamplifier.

Offset gain of Channel 2 Preamplifier U320 is set higher when the CH2 VOLTS/DIV switch is set to 2 mV, 5 mV, 10 mV, 100 mV, or 1 V/Div. At those VOLTS/DIV settings, the FASTCLAMP bit is set LO to turn on U420E. This turns FET Q419 on and places C520 in parallel with C522 thus increasing the size of the hold capacitance. This slows down the loop response at the "more sensitive" offset gain setting of the Channel 2 Preamplifier to prevent oscillation.

CLAMP SWITCHING. The Clamp Switching circuit enables and disables the effect of the Channel 2 Vertical Display Clamp. The clamp circuit operation may be switched to provide correct clamping for either inverted or noninverted video signals.

When display clamping of the Channel 2 signal is not enabled, BCLAMPENA will be set LO, turning U420D on. The HI on the collector of U420D turns on U410B, U410C, and Q420 and turns off Q710 via U710A. Any enabling currents to offset amplifiers U514 or U520 are shunted through U410B and U410C respectively. With FET Q420 on, the input to U710D will be grounded. This disables the

Offset Buffer. With FET Q710 turned off via U710A, the offset line to the Channel 2 Vertical Preamplifier is open circuited, so no trace offsetting can occur.

When the Channel 2 Vertical Display Clamp is enabled, BCLAMPENA will be HI, turning U420D off. The LO on the collector of U420D turns Q420 off, enabling Offset Buffer Amplifier U710D to track the offset level output from the active Offset Amplifier, and the offset signal line to the Channel 2 Vertical Preamplifier is connected to the Offset Buffer by turning on Q710 via U710A.

Selection of either U514 or U520 is controlled by the CH2 INV signal and is dependent on the setting of the invert function in the associated COUPLING/INVERT menu. Since signal offsetting in the Channel 2 Preamplifier is done before the signal is inverted, offset voltages for inverted- and normal-signal displays must be of opposite polarity. Switching between these two offset amplifiers provides the required polarity change and allows the back porch of either display type to be clamped at the ground reference. Depending on the polarity of the CH2 INV (Channel 2 Invert) signal, either U410E or U410D will be on, turning off either U410B or U410C. U410B will be off when CH2 INV is HI and U410C will be off when it is LO. Bias current from the Trigger Back-Porch Clamp circuit to the offset amplifiers (U514 and U520) is not shunted away by the "off" transistor, and the offset amplifier associated with the off transistor will be biased on during the sync pulse back-porch interval.

Biasing current to enable the selected Offset Amplifier is produced during the back-porch interval when U410A (in the Trigger Back-Porch Clamp circuit) is turned off. Bias current through either R411 or R410 (depending on whether U410B or U410C is off) is supplied via R403. The other offset amplifier will be disabled since its bias current is being shunted through the "on" transistor. The amount of bias current permitted by Transconductance Amplifier U504 to the "on" amplifier provides a signal to the Channel 2 Preamplifier (after buffering by U710D) that vertically offsets the displayed signal on Channel 2.

Since the offset voltage must be maintained throughout the entire horizontal interval, capacitor C522 (and C520 in parallel if FASTCLAMP is not enabled) serves as a hold capacitor between back-porch samples. At some VOLTS/DIV settings the Channel 2 Preamplifier is set for higher offset gain. Transistor Q419 will be turned on for those settings, placing C520 in parallel with C522 to slow down the loop response. This prevents oscillation in the Channel 2 Preamplifier at the more sensitive gain settings.

Offset Buffer Amplifier U710D applies this "stored" offset level to the Channel 2 Preamplifier (via Q710), shifting the back porch of the displayed signal to near the on-screen ground reference (as set with the Vertical POSITION control).

Any time the Phase-Locked Loop is not locked (indicating that a proper TV Trigger signal is not present), the Channel 2 Vertical Display Clamp is turned off via R328 by a HI $\overline{\text{TVCLAMP}}$ signal from the PLL Unlock Detector to prevent sending invalid offsets to the Channel 2 Preamplifier. During the unlocked state of the PLL, FET Q420 is biased on to pull the input to Offset Buffer Amplifier U710D to ground, and FET Q710 is biased off via U710A (acting as an inverter to the $\overline{\text{TVCLAMP}}$ signal) to open circuit the offset signal line to the Channel 2 Preamplifier.

LOW-VOLTAGE POWER SUPPLY

The low voltages required by the 2430 are produced by a high-efficiency, switching power supply (diagram 22). This type of supply directly rectifies and stores charge from the ac line supply; then the stored charge is switched through a special transformer at a high rate, generating the various supply voltages.

AC Power Input

LINE SWITCHING AND LINE RECTIFIER. Ac line voltages of either 115 V or 230 V may provide the primary power for the instrument, depending on the setting of the LINE VOLTAGE SELECTOR switch S1000 (located on the instrument rear panel). POWER Switch S1350 applies the selected line voltage to the power supply rectifier (CR510).

With the selector switch in the 115 V position, the rectifier and storage capacitors C105 and C305 operate as a full-wave voltage doubler. When operating in this configuration, each capacitor is charged on opposite half cycles of the ac input, and the voltages across the two capacitors in series approximates the peak-to-peak values of the source voltage. For 230 V operation, switch S1000 connects the rectifier as a conventional bridge rectifier. Both capacitors charge on both input half cycles, and the voltage across C105 and C305 in series approximates the peak value of the rectified source voltage. For either configuration (with proper line voltage), the dc voltage supplied to the power supply inverter is the same.

SURGE PROTECTION. Thermistors RT717 and RT805 limit the surge current when the power supply is first turned on. As current warms the thermistors, their resistances decrease and have little effect on circuit operation.

Spark-gap electrodes E609 and E616 are surge voltage protectors. If excessive source voltage is applied to the instrument, the spark-gaps conduct, and the extra current quickly exceeds the rating of F1000. The fuse then opens to protect the power supply.

EMI FILTER. A sealed line filter, FL1000, is packaged with the line cord connector. It is effective in reducing noise with frequency components at and beyond 1 MHz. A differential mode filter is made up of R809, C816, R815, L715, L709, R808, R713, and C706 and is effective in reducing switch-mode noise up to 1 MHz. Resistor R1000 ensures that the capacitors in the line filter become discharged a short time after removal of the line cord so as to not present a shock hazard at the line cord connector. A combination common-mode and differential-mode filter is made up of T117, R217, R117, C218, C225, and C328. The line-rectification energy-storage capacitors (C105 and C305) also aid in the operation of this filter circuit. Resistors R410 and R400 bleed charge from the line-rectification capacitors to guarantee that they are discharged within a definite time after power is removed (turned off).

THERMAL SWITCH. Thermal Switch S1020 opens if the temperature of the power supply heatsink becomes abnormally high. High temperatures may indicate blocked ventilation holes or failed components. Opening the switch removes ac-line power from the supply to prevent any further damage from occurring. When the heatsink cools to its normal limits, the switch recloses. Opening of S1020 immediately shuts off the power supply, and the System μP does not perform its normal shutdown routine. Waveforms and front-panel settings are not saved on a thermal shutdown.

Control Power Supply

The control circuits for the power supply require a separate power supply circuit to operate. This independent power source is made up of Q148, Q240, Q836, and associated components.

Initially, when instrument power is applied, the positive plate of capacitor C244 is charged toward the value of the positive rectified-line voltage through R223. The voltage at the base of Q148 follows at a level determined by the voltage divider composed of R436, R244, CR239, R245, R640, Q836 and the load resistance placed on the supply. When the voltage across C244 reaches about +27 V, the base voltage of Q148 reaches +12.6 V and Q148 turns on, saturating Q240. The +27 V on the emitter of Q240 appears at its collector and establishes the positive voltage supply for the +12 V regulator stage formed by Q836, VR929, R245, and R640. With Q240 on, R244 is placed in parallel with R436 and both Q148 and Q240 remain saturated.

The +27 V level begins to drain down as the +12 V Regulator draws charge from C244. If the main power supply doesn't start (and thus recharge C244 via T335 and CR245) by the time the voltage across C244 reaches about +14 V, Q240 turns off. With Q240 off, resistor R244 pulls the base of Q148 low and turns it off also. (Capacitor C244 would only discharge low enough to turn off the transistors under a fault condition.) In this event, C244 would then charge again to +27 V, and the start sequence would repeat. Normally, the main power converter is delivering adequate power before the +14 V level is reached, and the current drawn through T335 via Q421 and Q423 induces a current in the secondary winding of T335 that charges C244 positive via diode CR245. The turns ratio of T335 sets the secondary voltage to approximately +17 V and, as long as the supply is being properly regulated, C244 is charged to that level and held there.

Power Conversion

The power converter consists of a buck-type switching Preregulator, producing width-regulated voltage pulses that are filtered to produce a preregulated dc current, and an Inverter stage that chops this preregulated current into ac to drive a power transformer. The transformer has output windings that provide multiple unregulated dc voltages after rectification has taken place. The main Preregulator components are Q421, Q423, CR426, C328, T335, T620, and U233. The fundamental Inverter components are Q521, Q721, T639, and U829B (see Figure 3-15).

PREREGULATOR. The Preregulator control circuit monitors the drive voltage reflected from the secondary to the primary of the Inverter output transformer T639 and holds it at the level that produces proper supply voltages at each of the secondary windings.

The Preregulator control circuit consists primarily of control IC U233, gate drive transformer T620, and the associated bias and feedback circuit elements. The voltage at the primary center tap of T639 is attenuated and applied to the voltage-sense input of control IC U233. This IC varies the "on time" of a series switch, depending on whether the sensed voltage is too high or too low. Transistors Q421 and Q423 form this "series switch," and are each active during alternate switching cycles. The on-time duty cycle of the series switch is inversely proportional to the rectified line voltage on C328. In normal operation, the series switch is on about one-half of the time. When the series switch is off, current to T639 is through CR426.

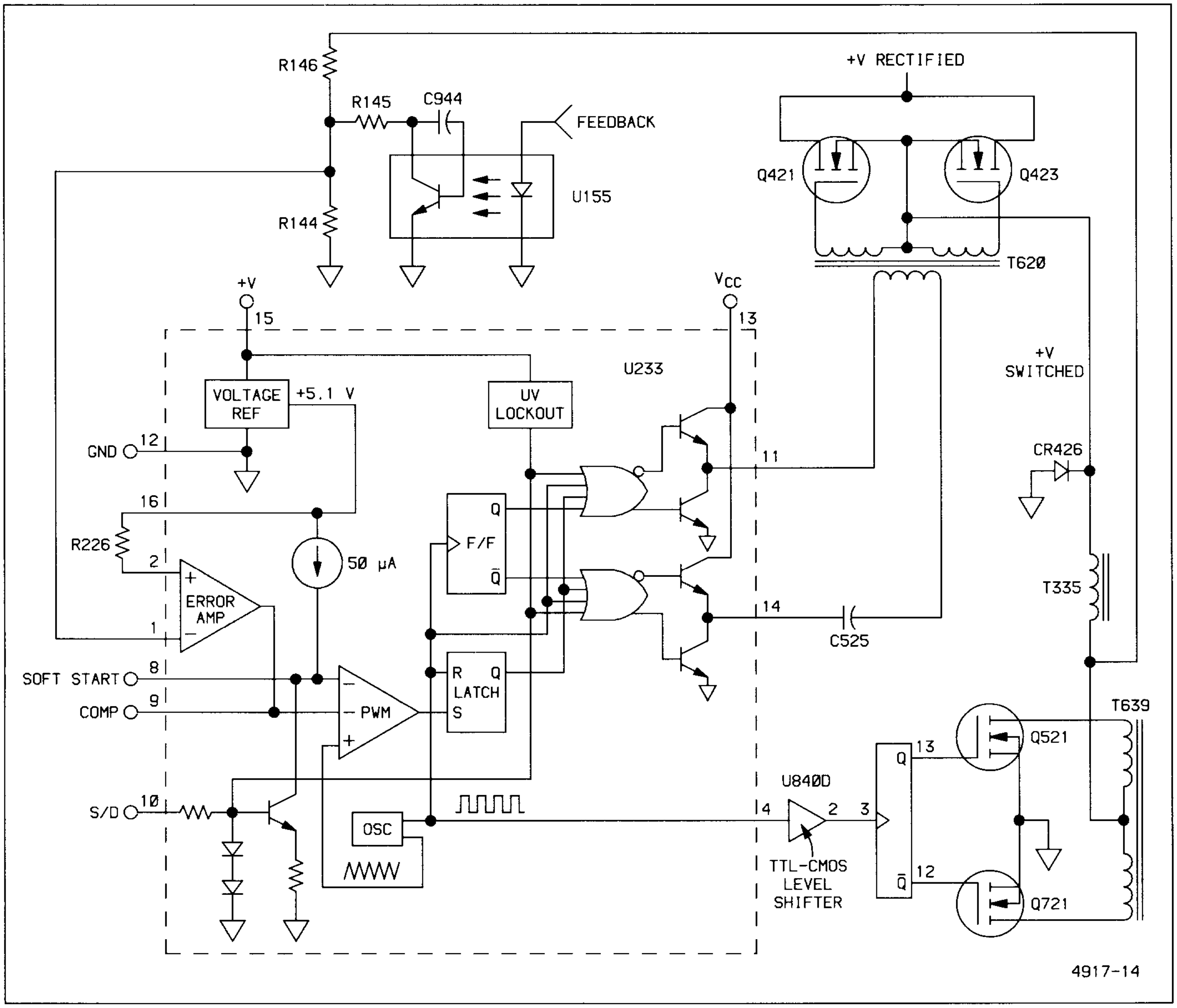


Figure 3-15. PWM Regulator and Inverter.

PREREGULATOR START-UP. As the supply for the Preregulator control IC is established, an internal oscillator begins to run. The oscillator generates a repetitive triangular wave (as shown in Figure 3-16) at a frequency determined primarily by R228 and C227 (with R227 having a minor effect since it controls the discharge time of timing capacitor C227).

As the control power supply turns on, a 50 μA current source internal to U233 begins to charge capacitor C128 positive. This charging level, applied to one of the negative inputs of the PWM comparator, allows drive pulses of greater and greater duty cycle to be generated. These pulses drive the series switching transistors (Q421 and Q423), and their slow progression from narrow to wide causes the various secondary supplies to gradually build up to their final operating levels. This slow buildup prevents a turn-on current surge that would cause the current-limit circuitry to shut down the supply.

PREREGULATION. Once the initial charging at power-up is accomplished (as just described), the voltage-sensing circuitry begins controlling the Inverter switching action. The voltage level at the primary center tap of T639 is divided by sense string R146-R144, and the resulting voltage is applied to the error amplifier internal to U233 at pin 1. The +5.1 V reference generated by U233 is applied to pin 2 of U233, the other input of the error amplifier. If the sensed level at pin 1 is lower than the reference level at pin 2 (as it always is for the first few switching cycles), the output of the error amplifier is high. This high level is applied to a negative input of the PWM comparator; the other negative input is applied from the soft-start capacitor (described previously).

The lower of the two negative input levels determines the actual negative comparison point of the PWM comparator; and this level determines the point at which the positive-going ramp, applied to the positive input, switches the PWM comparator to initiate the off state of the PWM switch. The PWM series switch is turned on at the beginning of each clock cycle; turn-off occurs when the positive-going ramp crosses the threshold level of the PWM comparator. The lower the level at the controlling (negative) input, the shorter the PWM switch "on time." Depending on the output level sensed, the duty cycle of the drive signal changes (sensed level rises or falls with respect to the triangular waveform applied to the positive PWM comparator input) to hold the secondary supplies at their proper levels.

Optoisolator U155 and resistor R145 form a control network that allows a voltage sensed at the FEEDBACK input to slightly alter the voltage-sense reference applied to pin 1 of U233. The FEEDBACK signal is generated by the +5 V Inverter Feedback amplifier (U189, diagram 23) and is directly related to the level of the +5 V_D supply line. If the FEEDBACK signal goes above its nominal level (+5 V_D is too low), base drive to the shunt transistor (in optoisolator U155) increases. This increase causes additional current to be shunted around R144 (via R145 and phototransistor of U155) and changes the ratio of the sensing divider. The voltage at the center tap of T639 must increase to balance out the changed sense ratio and maintain balance in the error amplifier. Since the output of the error amplifier controls the current to the primary winding of the output transformer, and since the error amplifier sensing depends on a balanced condition, the voltage at the transformer primary increases.

With a higher current applied to the transformer primary, higher voltages appear across the secondary windings of T639 with each cycle. This causes the secondary voltages to return to their nominal levels. As the +5 V_D line returns to its nominal level, base drive to the shunt transistor stabilizes at a level that keeps the sensed +5 V_D level in regulation. Should the FEEDBACK signal level tend too high, opposite control responses occur. Further information about the FEEDBACK signal is given in the +5 V Inverter Feedback description.

INVERTER. The Inverter circuit alternately switches current through each leg of the primary winding of output transformer T639. The circuit is made up of Q521, Q721, U840D, U829B, and associated components.

A clock pulse from U233 is applied to a TTL-CMOS level shifting buffer (U840D) at the beginning of every switching cycle. The level-shifted clock pulse at the output of U840 clocks U829B, a CMOS D-type flip-flop (configured to toggle with each clock). The Inverter switch transistors, Q521 and Q721, are alternately turned on and off by the flip-flop outputs and are connected to opposite ends of the primary winding of the output transformer. Driving the inverter switches in alternate fashion produces ac currents in the secondary windings of the output transformer that are rectified, providing the various unregulated dc supply voltages.

Primary Fault Sensing

Primary current, primary regulated voltage, and primary unregulated voltage are monitored by circuitry to prevent catastrophic failure. Should conditions arise that cause an excessive primary current or an excessive primary regulated voltage, limiting occurs. The excessive primary current and primary regulated voltage functions share much common circuitry, while the low unregulated primary voltage circuitry is entirely independent of the first two fault-sensing circuits.

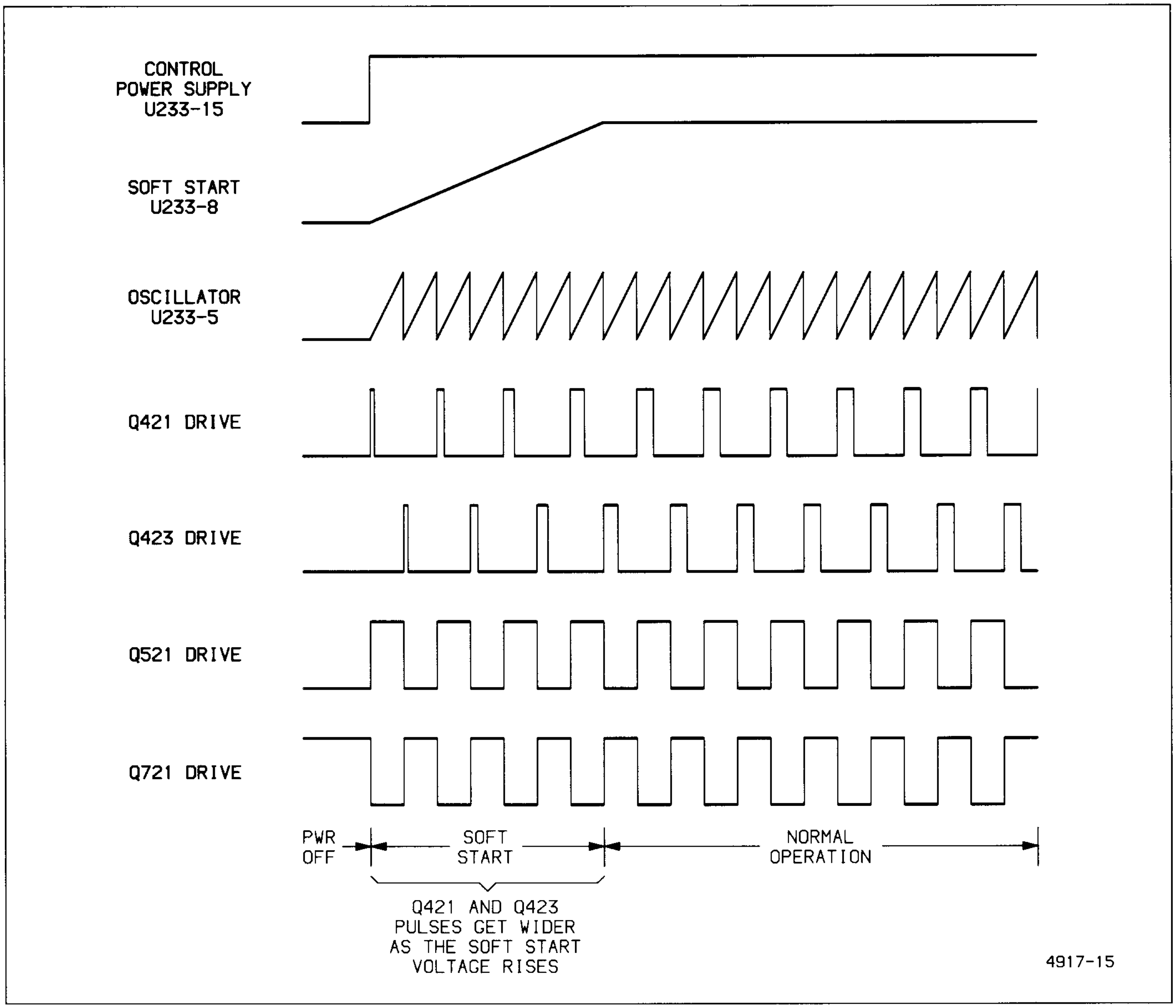


Figure 3-16. PWM switching waveforms.

PRIMARY OVER-CURRENT SENSING. The primary current of T639 through R727 produces a voltage signal that is filtered by R728 and C728 to remove high-frequency switching spikes. The filtered signal is applied to the inverting input of U840C. The noninverting input of the comparator is set at a level defined by the +5.1 V reference from U233 and voltage divider R935-R836. If an excessive-current condition exists (to the point that the inverting input of U840C goes more positive than the noninverting input), the comparator output goes low. The open-collector output of the comparator is "wire-ORed" with the open-collector output of the regulated primary over-voltage comparator (U840B) and drives U840A, connected as an inverting buffer. Buffer U840A drives the clock input of a CMOS flip-flop in U829, configured as a monostable flip-flop, used to shut down supply operation.

PRIMARY OVER-VOLTAGE SENSING. The regulated primary voltage is sensed by the voltage divider R129-R128, with C528 providing low-pass filtering to remove high-frequency switching spikes. The attenuated signal is applied to comparator U840B at the inverting input, while the noninverting input is connected to the +5.1 V reference from U233. Should the regulated primary voltage become high enough to raise the inverting input of the comparator more positive than the noninverting input, the comparator output goes to a low level. As previously stated, the output of this comparator is wire-ORed to the output of U840C and drives an inverting clock buffer U840A. This buffer in turn drives the clock input of the monostable flip-flop circuit used to shut down supply operation.

SHUTDOWN TIMER. The Shutdown Timer ensures that the preregulator series switch remains off long enough for energy stored in C128 (the soft-start capacitor) and C244 (the Control Power Supply energy-storage capacitor) to drain down via normal circuit loading should an over-current or over-voltage fault occur. Shutdown of the series switch (Q421 and Q423) occurs when the S/D (shutdown) input (pin 10) of U233 goes high. The Shutdown Timer, made up of U829A, R824, C829, R934, CR730, and CR824, controls this input.

Prior to being clocked, U829A (configured as a monostable flip-flop) is in a reset state with its Q output set low. This is the normal operating mode and allows the series switch to be controlled by the regulating functions of U233. Capacitor C829 charges to the Control Power Supply voltage via R824 and CR824 (diode CR824 shunts R934 when charging C829 to provide a relatively fast charging path). When the flip-flop is clocked (indicating a fault-sense from the voltage- or current-sense circuits), the Q output goes high and C829 begins to discharge. With Q high, CR824 becomes reverse biased so that discharge of C829 is through R934, providing a relatively slow discharge compared to the charging time. This ensures that the Q output of U829A is held high long enough for soft-start capacitor C128 and Control Power Supply capacitor C244 to fully discharge.

The high Q output of U829A, connected to the shutdown input to U233, turns off the PWM switch (Q421 and Q423) immediately and keeps it off until Q returns low (when the Control Power Supply decays and turns U829 off). However, the PWM clock continues to run and the Inverter switches (Q521 and Q721) continue to operate. Since the PWM switch is not operating, energy is not transferred to the Control Power Supply via T335, and C244 discharges below the minimum voltage level required by the Control Power Supply circuit (through the normal circuit load). When this minimum level is reached, the Control Power Supply regulator disconnects from C244, interrupting the power to the control circuitry and stopping the Inverter switches.

Monostable U829A is designed to remain active long enough for the Control Power supply to decay and disconnect. The disconnect level is approximately half of the Control Power Supply voltage and, once disconnected, supply voltage is reestablished in 0.5 to 2 seconds. The time it takes C244 to charge from the "disconnect threshold" to the Control Power Supply "turn-on threshold" is the dominate factor in determining the power supply restarting time when recovering from an over-current or over-voltage fault condition.

Capacitor C829 is once again charged through R824 and CR824 with a relatively short time constant, allowing U829A to be triggered again (if the fault persists) by the time the Control Power Supply restarts.

LINE UP. The Line Up circuit, composed of U834B, U265, and associated components, senses the level of the rectified line voltage and relays its status through the PWRUP circuit to the System μP. The signal from voltage divider R325-R835 is low-pass filtered by C835 and is applied to the inverting input of comparator U834B. The noninverting input of the comparator is referenced to the +5.1 V reference from U233. The output of the comparator drives the light-emitting diode of optoisolator U265, so whenever the rectified line-input voltage is below the normal operating level (approximately +178 V), the light-emitting diode (LED) is off. With the LED off, the output phototransistor of U265 is biased off.

At instrument turn-on, after the rectified line voltage comes up, the control power supply begins supplying power to the control circuitry. At that time, the output of comparator U834 goes LO at pin 7 to turn on the LED in optoisolator U265. This action biases on the output transistor of the optoisolator and switches the LINE UP signal HI. Through the PWRUP signal circuitry, a HI LINE UP signal tells the System μP that ample line voltage is available for normal instrument operation.

When instrument power is turned off, the rectified line voltage begins dropping. At about 178 V, comparator U834 switches off the LED in U264, and the LINE UP signal goes LO. A LO output tells the System μP that power is dropping, and the μP begins shutting the instrument down in an orderly fashion before the secondary voltages go out of regulation.

Line Trigger

The Line Trigger circuit, made up of T415, U170A, and the associated components, provides a representation of the input line signal to the Trigger stage that is isolated from the power-line environment.

Since resistors R516 and R518 are large compared to the impedance of the primary winding in T415, the transformer operates in a current-driven mode. The secondary winding of T415 is connected to a transresistance amplifier stage consisting of U170A, C483, and R483. This amplifier presents a very low impedance to the output of the transformer and maintains the integrity of the line voltage signal representation. Capacitor C483 provides a negative-feedback path to high frequencies (relative to 60 Hz) and reduces noise on the line-frequency signal. The output of the transresistance amplifier drives the oscilloscope trigger circuitry.

Rectifiers

The Rectifiers convert the alternating currents from the secondary windings of the Inverter output transformer to the various unregulated dc voltages required by the instrument. Rectification is done by conventional diode rectifier circuits, and filtering is done by conventional LC networks.

LOW-VOLTAGE REGULATORS

The Low-Voltage Regulators (diagram 23) remove ac voltage noise and ripple from the various unregulated dc supply voltages. Each regulator output is automatically current limited if the output current exceeds the requirements of a normally functioning instrument. This limiting prevents any further component damage.

+10 V and −5 V References

Each of the power supply regulators controls its respective output by comparing the output voltage to a known reference level. In order to maintain a stable supply voltage, the reference voltage must itself be highly stable. The circuit composed of U180, U170B, U900, and associated components produces the two reference levels used by the regulator circuits.

Resistor R556 and capacitor C664 form an RC filter network that smooths the unregulated $+15\ V_A$ supply before it is applied to voltage-reference IC U180. The +10 volt output from pin 6 of U180 feeds a low-pass filter composed of R900 and C900. The output of this filter in turn feeds unity-gain buffer amplifier U900, the output of which is the source of the +10 V reference used by the various positive regulators. Low-pass filter R900-C900 provides filtering for the IC voltage reference and provides for a well-defined voltage rise of the $+10\ V_{REF}$ voltage at power-up.

Operational amplifier U170B and its associated components make up a −5 V Reference circuit used as the reference for the negative regulators. It is configured as an inverting amplifier with a gain of 1/2 and converts the $+10\ V_{REF}$ input to a precision $-5\ V_{REF}$ output.

+15 V Regulator

The +15 V Regulator uses three-terminal regulator U579 and operational amplifier U570A (arranged as the voltage sensor) to achieve regulation of the +15 V supply). The three-terminal regulator holds its output voltage on pin 2 at 1.25 V more positive than the reference input level applied to pin 1. The voltage at the reference pin is established by current in diode CR575 and is controlled by voltage sensor U570A.

Resistors R576 and R575 at the regulator output divide the +15 V level down for comparison to the +10 V reference applied to pin 3 of operational amplifier U570A. At initial power up, when the input voltage at pin 2 (from the divider) is lower than the +10 V reference, the output of amplifier U570A is high, and the output voltage is allowed to rise. As the regulator output reaches +15 V, the amplifier begins sinking current away from the reference pin of the three-terminal regulator via diode CR575. This sets the voltage on the reference pin at its nominal level and holds the output at +15 volts.

Current limiting for the +15 V supply is provided by the internal circuitry of the three-terminal regulator. Diodes CR576 and CR583 protect U570A from transient voltage reversals.

+8 V Regulator

The +8 V Regulator is composed of Q465, Q479, U470A, U470B, and the associated components. The circuit regulates the voltage and limits the supply current.

Initially, as power is applied, the voltage at pin 6 of U470B via R476 is lower than the +8 V reference level applied to pin 5 via divider R465 and R466. The output of U470B is forced HI, reverse biasing diode CR466. With CR466 (and CR465) off, all the current through R565 is supplied as base current to Q465, turning it on. This turns on the pass transistor Q479 at maximum current. This current charges up the various loads on the supply line and the output level moves positive.

As the regulator output rises toward +8 V, this positive-going voltage is applied to the inverting input of U470B through R476. When the output voltage reaches +8 V, the inverting input equals the reference at the noninverting input set by R465 and R466. Then, the output at pin 7 of U470B goes negative, forward biasing diode CR466 and shunting base-drive current away from Q465. This reduces the currents through Q465 and Q479 to levels that maintain a +8 V output. Since base drive source for Q465 is the +15 V supply, via R565, proper relative polarity between the two supplies is assured (preventing component damage in case of a failure on the +15 V supply line).

The over-current limiting circuit is of foldback design and is performed by operational amplifier U470A and its associated components. Under normal current demand conditions, the output of U470A is HI, keeping diode CR465 reverse biased. If the regulator output current exceeds approximately 1.3 A (as it might if a component fails), the voltage drop across R473 (added onto the +8 V output voltage) causes the inverting input of U470A to exceed the +8 V level at the noninverting input, and the output at pin 1 will go LO. This forward biases diode CR465 and reduces the forward bias on Q465 and thereby decreases the bias current to Q479. This in turn reduces the regulator output current through Q479 to decrease the output voltage. As the output voltage drops (applied to U470A pin 3), the output current required to cause limiting also decreases, causing both voltage and current to drop to low values as Q465 becomes biased off.

Pin 2 of U470A is pulled down through R477 to the $-8\ V_A$ supply so that the output of the foldback circuit becomes immediately HI at power-on. This initial HI holds CR465 biased off thereby preventing a false overcurrent sense and subsequent latchup at start-up as the +8 V regulated output seen on pin 3 of U470A rises from zero volts to its normal operating level.

+5 V Regulator

Regulation of the +5 V supply is provided by a circuit similar to that of the +8 V Regulator. As long as the relative polarity between the +8 V supply and the +5 V supply is maintained, base drive to Q870 is supplied through R864. The current through Q870 provides base drive for the series-pass transistor Q879.

When voltage-sense amplifier U870B detects that the +5 V remote-sense voltage has reached +5 V, it begins shunting base-drive current away from Q870 via diode CR866 and holds the output voltage constant.

Current limiting for the +5 V supply is done by U870A and associated components. Under normal current demand conditions, the output of U870A is high and diode CR865 is reverse biased. However, should the current through current-sense resistor R873 reach approximately 3 amperes, the voltage developed across R873 (added to the regulated +5 V output) raises the voltage at pin 2 of U870A (via divider R876 and R875) to a level equal to that at pin 3. This causes the output of U870A to go low, forward biasing CR865. Base drive current is then shunted away from Q870, and the output current in Q879 is reduced. Resistor R874 allows the supply to maintain regulation with the remote-sense line disconnected. Resistors R885 and R886 provide enough initial current to the load to prevent an excessive-current latchup of U470A as the power comes up.

−15 V Regulator

Operation of the −15 V Regulator, composed of U679, U570B and their associated components, is similar to that of the +15 V Regulator already described. The regulator is referenced to −5 V to allow sensing of the negative output level. Zener diode VR870 allows operational amplifier U570B to operate in its active region. Capacitor C873 is a speed-up capacitor that allows the regulator to respond more quickly to current surges and other transients and provides filtering of zener noise produced by VR870.

−8 V Regulator

Operation of the −8 V regulator is nearly identical to that of the +8 V Regulator, except that it is referenced to −5 V to allow sensing of negative voltages. Zener diode VR380 allows operational amplifiers U270A and U270B to operate in their linear regions.

The −8 V Sense input provides for remote sensing of the supply level on the Main board where regulation is the most critical. Since the −8 V level is remotely sensed, the IR drop caused by the impedance in the supply bus lines going to the main board and a small series resistor in the line (R121 on the Main board) causes the actual output level from the supply regulator to be closer to −8.4 V. (This is the voltage actually required by some of the −8 V load circuits.) Resistor R388 allows the supply to maintain regulation with the remote sense line disconnected. Current limiting of the combined −8 V and −8.3 V supplies occurs at about 3 amperes.

−5 V Regulator

Operation of the −5 V Regulator is similar to that of the +5 V Regulator. Current limiting of the −5 V supply occurs at about 3.1 amperes.

+5 V Inverter Feedback

Operational amplifier U189 and associated components are configured as a frequency-compensated voltage-sensing network. The circuit monitors the +5 V digital power supply line from the rectifiers and provides feedback to the Preregulator Control IC (U233) via optoisolator U155 (both on diagram 22). The feedback is used to trim the +5 V_D level by controlling the Preregulator. The FEEDBACK signal slightly varies the voltage to the Inverter output transformer and holds the output of the 5 V secondary windings at an optimum level. Output levels of the other secondary windings are related by turns ratio to the +5 V_D level and are also held at their optimum levels. This technique minimizes power losses in the series-pass transistors and increases regulator reliability.

Power-Up

The Power-Up circuit, composed of U189A, Q295 and the associated components, provides buffering and level shifting of the LINE UP signal to the System Processor.

Operational amplifier U189A is configured as a comparator referenced to +10 V_{REF} . When adequate power-line input voltage is available, the LINE UP signal will be HI. The output of the comparator will be LO, turning off transistor Q295. This results in a HI PWRUP signal to the System μP, indicating that the power supplies are stable. When adequate power-line voltage is not available, the LINE UP signal from the Preregulator circuit goes LO, the output level of U189A goes HI and turns Q295 on, resulting in a LO PWRUP signal to the System μP. This indicates that the various supply voltages may go out of regulation in about 10 ms.

Capacitor C195 provides a negative-feedback path for high-frequency signals and stabilizes operation of U189A.

DC-OK Sense

The output of the DC-OK Sense circuit is checked by the System Processor after it receives the PWR UP signal to verify that power supply voltages are within tolerance.

By itself, the resistive summing network made up of R794, R795, R797, R686, R688 and R796 would produce a voltage near zero volts if all supplies were within tolerance. This voltage may vary ±0.19 V, depending on slight variations in the individual supply output levels. The current in resistor R396 is, however, added into the summing node and shifts its operating point approximately 0.19 V positive.

The resulting voltage is compared to ground by comparator U395B and to +0.37 V by comparator U395A, establishing the tolerance window. Both open-collector outputs of the comparator are off, and the DCOK signal is HI, as long as the summing-node voltage falls within this window. Should the summing-node voltage exceed either limit, the associated comparator turns on its output transistor and pulls the DCOK signal LO, indicating that at least one of the power supplies is not operating properly.

PERFORMANCE CHECK AND FUNCTIONAL VERIFICATION PROCEDURE

NOTE

Perform the Self Calibration subsection of the Adjustment Procedure before performing this procedure. The Adjustment Procedure is Section 5 of this manual.

INTRODUCTION

This procedure is used to verify proper operation of instrument controls and to check the instrument's performance against the requirements listed in the "Specification" (Section 1). This procedure verifies instrument function and may be used to determine need for readjustment. These checks may also be used as an acceptance test and as a preliminary troubleshooting aid.

Removing the instrument cabinet is not necessary to perform this procedure. All checks are made using the operator-accessible front- and rear-panel controls and connectors.

Within the procedure, steps to verify proper operation of an instrument control or function that is not specified in the "Specification" section begin with the word "VERIFY." These functions ARE NOT specifications and should not be interpreted as such. Steps to check performance specifications begin with the word "CHECK."

PREPARATION

NOTE

This procedure assumes that the operator is sufficiently acquainted with this instrument's operation to obtain the initial and subsequent control settings necessary to perform the procedure. Complete instructions for setting the controls to obtain the various operating modes of this instrument are given in the 2430 Operators Manual.

Test equipment items 1 through 20 listed in Table 4-1 are required to perform this procedure. The specific pieces of equipment required to perform the checks within each subsection are listed at the beginning of that subsection. The item numbers in parenthesis next to each piece of equipment refer to the numbered equipment list of Table 4-1. Items 15 and 20 are used only for instrument calibration (see the Adjustment Procedure—Section 5).

Before performing this procedure, ensure that the LINE VOLTAGE SELECTOR switch is set for the ac power source being used (see "Preparation for Use" section of this manual). Connect the instrument to be checked and the test equipment to an appropriate power source. Turn the instrument on and ensure that no error message is displayed on the crt. If an error message is present, have the instrument repaired by a qualified service technician before performing this procedure.

This procedure is divided into subsections (VERTICAL SYSTEM, TRIGGERING SYSTEM, etc.) and further into steps (Verify CH 1 and CH 2 50 Ω Overload Protection, etc.). This arrangement allows verification of the functionality of the instrument's individual sections, as well as its conformance to individual specifications, without requiring performance of the entire procedure. Any number of steps (in any order) can be performed as long as ALL the parts of a step are performed in sequence and in their entirety.

Table 4-1

Test Equipment Required

NOTE: Item numbers 21 through 25 are needed for checking the 2430 TV Option 05 only.

Item and Description	Minimum Specification	Purpose	Example of Suitable Test Equipment
1. Leveled Sine-Wave Generator	Frequency: 250 kHz to above 70 MHz. Output amplitude: variable from 10 mV to 5 V p-p. Output impedance: 50 Ω. Reference frequency: 50 kHz. Amplitude accuracy: constant within 3% of reference frequency as output frequency changes.	Vertical, horizontal, and triggering checks and adjustments.	TEKTRONIX SG 503 Leveled Sine Wave Generator.[a]
2. Calibration Generator	Standard-amplitude signal levels: 5 mV to 50 V. Accuracy: ±0.25%, ±1 μV. Repetition Rate: 1 kHz. High-amplitude signal levels: 1 V to 60 V. Repetition rate: 1 kHz. Fast-rise signal level: 100 mV to 1 V. Repetition rate: 100 Hz to 100 kHz. Rise time: 1 ns or less. Flatness: ±0.5%.	Signal source for gain.	TEKTRONIX PG 506 Calibration Generator.[a]
3. Time-Mark Generator	Marker outputs: 10 ns to 0.5 s. Marker accuracy: ±0.1%. Trigger output: 1 ms to 0.1 μs, time-coincident with markers.	Horizontal checks.	TEKTRONIX TG 501 Time Mark Generator.[a]
4. Function Generator	Range: less than 1 Hz to 50 kHz; sinusoidal output; amplitude variable to greater than 10 V p-p open circuit with dc offset adjust.	Low-frequency checks.	TEKTRONIX FG 502 Function Generator.[a]
5. Power Supply	Range: 0 to 20 VDC.	50 Ω Overload verification.	TEKTRONIX PS 503A Power Supply.[a]
6. Digital Voltmeter (DMM)	Range: 0 to 140 V. Dc voltage accuracy: ±0.15%. 4 1/2 digit display.	XY Plotter output verification.	TEKTRONIX DM 501A Digital Multimeter.[a]
7. GPIB Controller	Conform to IEEE-488 (1978) standard.	Check GPIB operation.	TEKTRONIX 4041 System Controller.
8. GPIB Cable	Conform to IEEE-488 (1978) standard.	Check GPIB operation.	Tektronix Part Number 012-0630-03.
9. Coaxial Cable (2 required)	Impedance: 50 Ω. Length: 42 in. Connectors: BNC.	Signal interconnection.	Tektronix Part Number 012-0057-01.
10. Precision Coaxial Cable	Impedance: 50 Ω. Length: 36 in. Connectors: BNC.	Used with Calibration Generator.	Tektronix Part Number 012-0482-00.
11. Termination	Impedance: 50 Ω. Connectors: BNC.	Signal termination.	Tektronix Part Number 011-0049-01.
12. 10X Attenuator (2 required)	Ratio: 10X. Impedance: 50 Ω. Connectors: BNC.	Vertical and triggering checks.	Tektronix Part Number 011-0059-02.
13. 5X Attenuator	Ratio: 5X. Impedance: 50 Ω. Connectors: BNC.	Vertical and triggering checks.	Tektronix Part Number 011-0060-00.

[a]Requires a TM 500-Series Power-Module Mainframe.

Table 4-1 (cont)

Item and Description	Minimum Specification	Purpose	Example of Suitable Test Equipment
14. 2X Attenuator	Ratio: 2X. Impedance: 50 Ω. Connectors: BNC.	External triggering checks.	Tektronix Part Number 011-0069-02.
15. Alignment Tool	Length: 1 in. shaft. Bit size: 3/32 in. Low capacitance; insulated.	Adjust variable capacitors and resistors.	Tektronix Part Number 003-0675-00.
16. 10X Standard Accessory Probe (supplied with instrument)	DC to 250 MHz probe.	Signal input connector.	TEKTRONIX P6130.
17. 1X Probe	DC to 34 MHz probe.	Signal input connector.	Tektronix Part Number 010-6101-03. P6101.
18. Dual-Input Coupler	Connectors BNC female-to-dual-BNC male.	Signal interconnection.	Tektronix Part Number 067-0525-01.
19. BNC Female-to-Dual Adapter	Connectors BNC female-to-dual-banana male.	Signal interconnection.	Tektronix Part Number 103-0090-00.
20. Normalizer	Input Resistance: 1 MΩ. Input Capacitance: 15 pF.	Check input capacitance.	Tektronix Part Number 067-0681-01.
21. Pulse Generator	Period Range: 1 ms to 2 μs. Pulse Range: 0.5 ms to 1 μs. Amplitude variable from −5 to +5 V, independent pulse top and pulse bottom.	Check TV triggers for sync separation, Option 05 only.	TEKTRONIX PG 502 Pulse Generator.[a]
22. Sync and Linearity Test Generator	Conforms to TV System requirements.	Check TV triggers for back-porch clamp operation.	TEKTRONIX R147A NTSC Test Signal Generator. TEKTRONIX R148 Insertion Test Signal Generator.
23. Sine-Wave Oscillator	Frequency: adjustable to 60 Hz. Amplitude: adjustable to 3 V p-p into 75 Ω.	Check TV triggers for back-porch clamp operation.	TEKTRONIX SG 502 Oscillator.[a]
24. Coaxial Cable (2 required)	Impedance: 75 Ω. Length: 42 in. Connectors: BNC.	Signal interconnection.	Tektronix Part Number 012-0074-00.
25. Termination	Impedance: 75 Ω. Connectors: BNC.	Signal termination.	Tektronix Part Number 011-0055-00.

[a]Requires a TM 500-Series Power-Module Mainframe.

Step 10 of the VERTICAL CHECKS can be performed independently of other subsections and steps of this procedure. BEFORE PERFORMING ANY OTHER SUBSECTION STEP OF THIS PROCEDURE, THE INITIAL FRONT PANEL SETUP SUBSECTION MUST BE PERFORMED. This subsection is a procedure for setting up and storing a complete front panel setup that can be recalled. When performing any step of a subsection in this procedure, the first part (part a) will require that a recall of the stored front panel settings be performed and will specify the changes (if any) to be made to that setup. Make ONLY those changes specified; do not change any other control settings (including vertical and horizontal position settings).

NOTE

This instrument requires a 20 minute warm-up period before performance requirements can be checked. The instrument must be powered on for at least 20 minutes.

"Select" means to press the appropriate front panel button to obtain the stipulated menu on the crt screen. "Set," when preceded by a menu selection, indicates the stipulated menu function should be turned on or off by pressing the appropriate menu button. The function will appear underlined in the menu when turned on, not underlined when turned off. Control settings not listed do not affect the procedure.

INITIAL FRONT PANEL CONTROL SETUP

a. Select SAVE/RECALL SETUP

Set:	INIT PANEL	On

Select VERTICAL MODE

Set:	CH 2	On

Select CH 1 COUPLING/INVERT

Set:	50 Ω ON:OFF	ON

Select CH 2 COUPLING/INVERT

Set:	50 Ω ON:OFF	ON
Set:	A SEC/DIV	500 μs

b. Press the A/B TRIG button to select the B Trigger System.

c. Press the TRIGGER MODE button to display B TRIG MODE menu and set TRIG AFTER on. Press the A/B TRIG button to return to the A Trigger System.

d. Select STORAGE ACQUIRE and set REPET ON:OFF ON. Repeatedly press the menu button labeled AVG until a "16" appears above the AVG. Repeatedly press the ENVELOPE button until a "16" appears above ENVELOPE. Set NORMAL back on.

e. Select SAVE/RECALL SETUP and press the SAVE menu button.

f. Press the menu button labeled 1 to save the setup.

g. To display the Trigger Point Indicator, select EXTENDED FUNCTIONS menu. Press SYSTEM MISC and set TRIGT ON:OFF ON. TRIGT will remain on unless turned off by user.

VERTICAL SYSTEM

NOTE

Before performing the steps in this subsection, perform the INITIAL FRONT PANEL CONTROL SETUP at the beginning of this procedure.

Equipment Required (See Table 4-1):

Leveled Sine-Wave Generator (Item 1)	5X Attenuator (Item 13)
Calibration Generator (Item 2)	2X Attenuator (Item 14)
Power Supply (Item 5)	10X Probe (Item 16)
Coaxial Cable (Item 9)	1X Probe (Item 17)
Precision Coaxial Cable (Item 10)	Dual-Input Coupler (Item 18)
10X Attenuator (Item 12)	

1. Verify CH 1 and CH 2 50 Ω OVERLOAD Protection.

a. Recall the Initial Front Panel Setting by performing the following sequence: Select SAVE/RECALL SETUP, press the menu button labeled RECALL (menu will change), and then press the menu button labeled 1. Make the following changes to the front panel setup:

Set:	CH 1 VOLTS/DIV	1 V
	CH 2 VOLTS/DIV	1 V

Select VERTICAL MODE

Set:	CH 2	Off

Select CH 1 COUPLING/INVERT

Set:	50 Ω ON!OFF	OFF

Select CH 2 COUPLING/INVERT

Set:	50 Ω ON!OFF	OFF

b. Connect the Power Supply (Power Supply should be turned off) to the CH 1 OR X input connector via a BNC female-to-dual banana adapter and a 50 Ω BNC cable.

c. Using the CH 1 VERTICAL POSITION control, align the trace to the bottom graticule line.

d. Turn on the Power Supply.

e. Adjust the Power Supply output level until the CH 1 trace rises to 1 division above the center graticule line (5 V).

f. Select CH 1 COUPLING/INVERT and set 50 Ω ON!OFF to ON.

g. VERIFY—For a period of 1 minute, the readout display does not indicate any overload condition (50 Ω OVERLOAD).

h. Set 50 Ω ON!OFF to OFF and the CH 1 VOLTS/DIV to 5 V.

CAUTION

To prevent damage to the input circuitry when in 50 Ω DC coupling mode, the 20 V Power Supply should be turned off immediately if automatic OVERLOAD switching does not occur within 15 seconds after applying the power source and setting the 50 Ω coupling ON in part j.

i. Increase the Power Supply output level until the CH 1 trace rises to the center graticule line (+20 V).

j. Set 50 Ω ON/OFF to ON.

k. VERIFY—Approximately 10 seconds (no longer than 15 seconds) after CH 1 50 Ω ON/OFF is set to ON, the readout display indicates "50 Ω OVERLOAD" and the CH 1 COUPLING switches to GND.

l. Turn the Power Supply off.

m. Disconnect the Power Supply.

n. Clear the 50 Ω OVERLOAD condition by setting CH 1 COUPLING to DC.

o. VERIFY—The readout display no longer indicates "50 Ω OVERLOAD" and the CH 1 COUPLING/INVERT menu indicates DC on.

p. Select VERTICAL MODE and set CH 1 off and CH 2 on.

q. Repeat b through n using CH 2 control settings and input to verify 50 Ω OVERLOAD protection for CH 2.

2. Check CH 1 and CH 2 AC/DC/GND COUPLING/INVERT Modes.

a. Recall the Initial Front Panel Setting by performing the following sequence: Select SAVE/RECALL SETUP, press the menu button labeled RECALL (menu will change), and then press the menu button labeled 1. Make the following changes to the front panel setup:

Set:	CH 1 VOLTS/DIV	200 mV
	CH 2 VOLTS/DIV	200 mV
Select VERTICAL MODE		
Set:	CH 2	Off
Select CH 2 COUPLING/INVERT		
Set:	50 Ω ON/OFF	OFF
	GND	On
Select CH 1 COUPLING/INVERT		
Set:	50 Ω ON/OFF	OFF
	GND	On
Set:	A SEC/DIV	5 ms

b. Connect the CALIBRATOR output signal to the CH 1 OR X input connector using a 1X probe.

c. Set the CH 1 COUPLING/INVERT menu to DC on (a GND symbol disappears next to the CH 1 scale factor readout).

d. CHECK—Display for a square wave which steps positive (upwards) approximately 2 divisions from the center horizontal graticule line.

e. Set CH 1 COUPLING to AC (a sine wave symbol appears next to the CH 1 scale factor readout in upper left-hand corner of crt).

f. CHECK—Display for a tilted square wave of approximately 2 divisions (average) amplitude centered vertically around the center horizontal graticule line.

g. Set 50 Ω ON/OFF to ON (the sine wave symbol is replaced by an ohm symbol next to the CH 1 scale factor readout).

h. CHECK—Display for a square wave which steps positive (upwards) approximately .5 division from the center horizontal graticule line. VERIFY—That CH 1 COUPLING automatically switched from AC on to DC on.

i. Set INVERT ON/OFF to ON (an inverted arrow appears left of the CH 1 scale factor readout).

j. CHECK—Displayed square wave now steps downwards from the center horizontal graticule line and is approximately .5 division in amplitude.

k. Select VERTICAL MODE and set CH 2 on and CH 1 off. Select CH 2 COUPLING/INVERT to display that menu.

l. Move the probe from the CH 1 input connector to the CH 2 input connector.

m. Repeat parts c through j using the CH 2 input and controls.

n. Disconnect the test setup.

3. Check CH 1 and CH 2 VOLTS/DIV Display and Readout Accuracies. Check the A and B TRIGGER LEVEL Readout Accuracies.

a. Recall the Initial Front Panel Setting by performing the following sequence: Select SAVE/RECALL SETUP, press the menu button labeled RECALL (menu will change), and then press the menu button labeled 1. Make the following changes to the front panel setup:

Select VERTICAL MODE
Set: CH 2 Off

Select CH 1 COUPLING/INVERT
Set: 50 Ω ON/OFF OFF

Select CH 2 COUPLING/INVERT
Set: 50 Ω ON/OFF OFF

Select BANDWIDTH
Set: 20 MHz On

Select TRIGGER MODE
Set: AUTO On

b. Connect the Calibration Generator STD AMPLITUDE output to the CH 1 OR X input connector via a 50 Ω cable. Do not use a termination.

c. CHECK—CH 1 and CH 2 VOLTS/DIV and TRIGGER LEVEL readout accuracies as follows:

(1) Set VOLTS/DIV control to the first position listed in Table 4-2.

(2) Set the Calibration Generator STD AMPLITUDE output level to the corresponding Standard Amplitude Input Level in Table 4-2. Use the TRIGGER LEVEL control as necessary to obtain a stable display.

NOTE

To properly verify TRIGGER LEVEL readout accuracy, the Calibration Generator output must have rising and falling transition times (10% to 90%) > 20 nanoseconds. No overshoot should appear on the waveform.

(3) Verify that the generator output meets the requirements noted above.

(4) Use the VERTICAL POSITION control to set the bottom of the signal 3 divisions below graticule center.

(5) Select CURSOR FUNCTION and set VOLTS on.

(6) Using the CURSOR/DELAY control, align the selected cursor (segmented) with the bottom of the displayed waveform.

(7) Press the CURSOR SELECT button to select the other cursor (it will change from solid to segmented).

(8) Use the CURSOR/DELAY control to align this cursor to the top of the waveform. Take care to use the same reference points (top edge, bottom edge, or center) of the waveform and cursor as in subpart (6).

(9) CHECK—That the voltage reading displayed by the cursor readout is within the limits given in Table 4-2 in the "CURSOR VOLTS Readout Accuracy—NORMAL" column.

(10) Select STORAGE ACQUIRE and set ENVELOPE on.

(11) Using the CURSOR/DELAY control, readjust the cursors as necessary to align them to the top or bottom (discount noise) of the waveform. Press CURSOR SELECT as needed to toggle between the two cursors.

(12) CHECK—That the voltage reading displayed is within the limits given in Table 4-2 in the "CURSOR VOLTS Readout Accuracy—ENVELOPE" column.

(13) Set the ACQUIRE menu back to NORMAL on.

(14) Set the TRIGGER LEVEL control at the most positive voltage that produces a barely triggered, jittering display for the positive (+) setting of the SLOPE switch.

(15) CHECK—The A Trigger Level readings (upper right corner of display) are within the limits listed in the "(+) Peak" column under DC Coupling in Table 4-2.

(16) Set the TRIGGER LEVEL control at the most negative voltage that produces a barely triggered, jittering display for the negative (−) setting of the SLOPE switch.

(17) CHECK—The A Trigger Level readings are within the limits listed in the "(−) Peak" column under DC Coupling in Table 4-2.

(18) Set the TRIGGER LEVEL control for a stable display.

(19) Press the A/B TRIG button to set the B Trigger System on.

(20) Set HORIZ MODE to B.

(21) Set the TRIGGER LEVEL control at the most positive voltage that produces a barely triggered, jittering display for the positive (+) setting of the SLOPE switch.

(22) CHECK—That the B Trigger Level readings (upper right corner of display) are within the limits listed in the "(+) Peak" column under DC Coupling in Table 4-2.

(23) Set the TRIGGER LEVEL control at the most negative voltage that produces a barely triggered, jittering display for the negative (—) setting of the SLOPE switch.

(24) CHECK—That the B Trigger Level readings are within the limits listed in the "(−) Peak" column under DC Coupling in Table 4-2.

(25) Set the HORIZ MODE to A.

(26) Press the A/B TRIG button to set the A Trigger System on.

(27) Set the VOLTS/DIV control to the next position listed in Table 4-2.

(28) Set the Calibration Generator STD AMPLITUDE output level to the corresponding Standard Amplitude Output Level in Table 4-2.

(29) Use the VERTICAL POSITION control to set the bottom of the signal 3 divisions below graticule center.

(30) Repeat subparts (6) through (29) for each VOLTS/DIV setting listed in Table 4-2. Skip subparts (26) through (29) when checking the last VOLTS/DIV setting in the table.

(31) Press A/B TRIG to set the B Trigger System on. Select TRIGGER CPLG and set REJECT NOISE on.

(32) Press A/B TRIG to set the A Trigger System on (the A TRIG CPLG menu will be displayed). Set REJECT NOISE on.

Table 4-2

Accuracy Limits CH 1 and CH 2 CURSOR VOLTS Readout and A and B TRIGGER LEVEL Readouts

VOLTS/ DIV Con- trol	Stand- ard Ampl Out	CURSOR VOLTS Readout Accuracy		TRIGGER LEVEL Readout Limits—DC Coupling	
		NORMAL (2% + 0.04 div)	ENVELOPE (3% + 0.04 div)	+ Peak	− Peak
2 mV	10 mV	9.72 mV-10.28 mV	9.62 mV-10.38 mV	8.5 mV-11.5 mV	±1.2 mV
5 mV	20 mV	19.40 mV-20.60 mV	19.20 mV-20.80 mV	17.2 mV-22.8 mV	±2.2 mV
10 mV	50 mV	48.60 mV-51.40 mV	48.10 mV-51.90 mV	44.4 mV-55.6 mV	±4.0 mV
20 mV	0.1 V	97.20 mV-102.80 mV	96.20 mV-103.80 mV	89.6 mV-110.4 mV	±7.2 mV
50 mV	0.2 V	194.00 mV-206.00 mV	192.00 mV-208.00 mV	178.0 mV-222.0 mV	±16.0 mV
100 mV	0.5 V	486.00 mV-514.00 mV	481.00 mV-519.00 mV	448.0 mV-552.0 mV	±36.0 mV
200 mV	1 V	972.00 mV-1.03 V	962.00 mV-1.04 V	896.0 mV-1.1 V	±72.0 mV
500 mV	2 V	1.94 V-2.06 V	1.92 V-2.08 V	1.8 V-2.2 V	±160.0 mV
1 V	5 V	4.86 V-5.14 V	4.81 V-5.19 V	4.5 V-5.5 V	±360.0 mV
2 V	10 V	9.72 V-10.28 V	9.62 V-10.38 V	9.0 V-11.0 V	±710.0 mV
5 V	20 V	19.40 V-20.60 V	19.20 V-20.80 V	17.8 V-22.2 V	±1.6 V

(33) Set CH 1 VOLTS/DIV control to 50 mV.

(34) Set the Calibration Generator STD AMPLITUDE output level to 0.2 V.

(35) Repeat subparts (14) through (24), using 147 mV to 253 mV as the limits to check against in subparts (15) and (22) and +47 mV to −47 mV as the limits for subparts (17) and (24).

(36) Set the B COUPLING mode back to DC on.

(37) Press the A/B TRIG button to set the A Trigger System on (the A COUPLING menu will be displayed). Set A COUPLING to DC on.

(38) Set HORIZONTAL MODE to A.

(39) Set the CH 1 VOLTS/DIV control to 1 V and the Calibration Generator output level to 5 V.

(40) Select CH 1 VARIABLE and press and hold down the menu button labeled "↓" until the displayed waveform no longer decreases in amplitude.

(41) CHECK—That the amplitude of the displayed waveform is two divisions or less. VERIFY—That a ">" symbol appears immediately left of the CH 1 scale factor readout.

(42) VERIFY—That the amplitude of the displayed waveform increases when the menu button labeled "↑" is pushed.

(43) Press CAL. VERIFY—That the waveform has returned to its original amplitude and that the ">" symbol is no longer displayed.

(44) Select CH 1 COUPLING/INVERT and set INVERT ON!OFF to ON.

(45) Using the VERTICAL POSITION control, set the bottom of the waveform 3 divisions below graticule center.

(46) Repeat subparts (6) through (9) to check INVERT accuracy.

(47) Return INVERT ON!OFF to OFF.

(48) Select VERTICAL MODE and set CH 2 on and CH 1 off. Move the cable to CH 2 OR Y.

(49) Repeat subparts (1) through (48)—skipping (5)—to check the functions and accuracies for CH 2.

(50) Select TRIGGER MODE and set AUTO LEVEL on.

(51) Remove the cable from CH 2 OR Y input and connect the 5 V standard amplitude signal to CH 1 OR X and CH 2 OR Y through a Dual-Input Coupler.

(52) Using the CH 2 VERTICAL POSITION control, set the bottom of the CH 2 waveform 1.5 divisions below graticule center.

(53) Select VERTICAL MODE and set CH 1 on. Use the CH 1 VERTICAL POSITION to superimpose the CH 1 waveform exactly over the CH 2 waveform.

(54) Set CH 1 and CH 2 VOLT/DIV controls to 2 V. Set CH 1 and CH 2 off and ADD on.

(55) Align the cursors to the top and bottom of the displayed waveform as in subparts (6) through (8).

(56) CHECK—That the readout indicates between 9.72 and 10.28 V.

(57) Set CH 1 and CH 2 VOLTS/DIV back to 1 V and MULT on (ADD will be turned off).

(58) Align the cursors to the top and bottom of the displayed waveform as in subparts (6) through (8).

(59) CHECK—That the readout indicates between 23.80 and 26.20 V.

d. Set MULT off and CH 1 on.

e. Precisely align one voltage cursor to the graticule line three divisions above graticule center and the other cursor to the line three divisions below graticule center.

f. CHECK—That the voltage reading displayed is within 1% of 6.00 Volts (5.94 to 6.06).

g. Disconnect the test setup.

4. Check LF Linearity.

a. Recall the Initial Front Panel Setting by performing the following sequence: Select SAVE/RECALL SETUP, press the menu button labeled RECALL (menu will change), and then press the menu button labeled 1. Make the following changes to the front panel setup:

Select VERTICAL MODE
Set: CH 2 Off

Select CH 1 COUPLING/INVERT
Set: 50 Ω ON/OFF OFF

Select CH 2 COUPLING/INVERT
Set: 50 Ω ON/OFF OFF

b. Connect the Calibration Generator STD AMPLITUDE output to the CH 1 OR X input connector via a 50 Ω cable. Do not use a termination.

c. Set the Calibration Generator STD AMPLITUDE output level to 0.2 V.

d. Use the CH 1 POSITION control to center the waveform vertically around the center horizontal graticule line.

e. Use the generator VARIABLE control to adjust the waveform for exactly 2 vertical divisions on screen (discount trace width).

f. Use the CH 1 POSITION control to align the top of the waveform to the top horizontal graticule line.

g. CHECK—That the amplitude of the displayed waveform is between 1.88 and 2.12 divisions.

h. Use the CH 1 POSITION control to align the bottom of the waveform to the bottom horizontal graticule line.

i. CHECK—That the amplitude of the displayed waveform is between 1.88 and 2.12 divisions.

j. Select STORAGE ACQUIRE and set ENVELOPE on.

k. Repeat parts d through i to check the LF Linearity for the ENVELOPE mode. Discount the noise and the envelope "fill" when performing parts g and i and use 1.84 and 2.16 divisions as limits for those parts.

l. Set the STORAGE ACQUIRE mode to NORMAL on.

m. Move the cable from the CH 1 OR X input to the CH 2 OR Y input.

n. Select VERTICAL MODE and set CH 2 on and CH 1 off.

o. Repeat parts d through k to check CH 2 using CH 2 control settings and menus.

p. Disconnect the test setup.

5. Check CH 1 and CH 2 Position Range.

a. Recall the Initial Front Panel Setting by performing the following sequence: Select SAVE/RECALL SETUP, press the menu button labeled RECALL (menu will change), and then press the menu button labeled 1. Make the following changes to the front panel setup:

Set: CH 1 and CH 2 VOLTS/DIV 50 mV
A SEC/DIV 10 μs

Select VERTICAL MODE
Set: CH 2 Off

b. Connect a 50 kHz reference frequency signal from the Leveled Sine-Wave Generator to the CH 1 OR X input connector via a 50 Ω BNC cable and a 5X attenuator.

c. Adjust the generator output level for a 4 division display on screen.

d. Remove the 5X attenuator and connect the cable directly to the CH 1 input.

e. Rotate the CH 1 POSITION control full clockwise and hold until the waveform no longer moves up screen.

f. CHECK—That the bottom of the waveform is within +0.7 to −0.4 division of the center horizontal graticule line.

g. Rotate the CH 1 POSITION control full counterclockwise and hold until the waveform no longer moves down screen.

h. CHECK—That the top of the waveform is within +0.4 to −0.7 division of the center horizontal graticule line.

i. Reinstall the 5X attenuator and move the cable to the CH 2 OR Y input.

j. Select VERTICAL MODE and set CH 2 on and CH 1 off.

k. Repeat parts c through h to check CH 2 position range, using the CH 2 input connector and controls.

l. Disconnect the test setup.

6. Check CH 1 and CH 2 Bandwidth and Bandwidth Limit (20 MHz and 50 MHz).

a. Recall the Initial Front Panel Setting by performing the following sequence: Select SAVE/RECALL SETUP, press the menu button labeled RECALL (menu will change), and then press the menu button labeled 1. Make the following changes to the front panel setup:

Set:	CH 1 VOLTS/DIV	2 mV
	CH 2 VOLTS/DIV	2 mV
	A SEC/DIV	200 ns

Select VERTICAL MODE

Set:	CH 2	Off

b. Connect the output of the Leveled Sine-Wave Generator to the CH 1 OR X input connector via a precision 50 Ω BNC cable, a 10X Attenuator, and a 2X Attenuator.

c. Set the generator output level for a 6 division display at the 3 MHz reference frequency, then change the output frequency to 150 MHz.

d. Set A SEC/DIV to 5 ns.

e. CHECK—The display amplitude is 4.2 divisions or greater.

f. Return the A SEC/DIV control to 200 ns and set the CH 1 VOLT/DIV control to the next higher setting.

g. Repeat parts c through f for all CH 1 VOLTS/DIV settings through 500 mV, removing and/or adding attenuators as necessary to allow adjusting the generator output level to 6 divisions.

h. Select VERTICAL MODE and set CH 2 on and CH 1 off.

i. Repeat parts b through g to check CH 2 bandwidth, substituting CH 2 controls and input connector.

j. Set A SEC/DIV to 10 μs.

k. Set the generator to a 50 kHz reference frequency and adjust the output level for a 6 division display (change attenuators as required).

l. Select VERTICAL BANDWIDTH and set to 20 MHz on. Set the A SEC/DIV to 20 ns.

m. Increase the generator output frequency until the display amplitude is 4.2 divisions.

n. CHECK—That the generator output frequency is from 13 MHz to 24 MHz.

o. Set the VERTICAL BANDWIDTH to 50 MHz on and increase the generator output frequency until the display amplitude is 4.2 divisions.

p. CHECK—That the generator output frequency is from 40 MHz to 55 MHz.

q. Set the VERTICAL BANDWIDTH to FULL. Move the 50 Ω cable from the CH 2 input to the CH 1 input connector.

r. Select VERTICAL MODE and set CH 1 on.

s. Repeat parts j through p to check bandwidth limit for CH 1.

t. Disconnect the test setup.

7. Check Common Mode Rejection Ratio (CMRR).

a. Recall the Initial Front Panel Setting by performing the following sequence: Select SAVE/RECALL SETUP, press the menu button labeled RECALL (menu will change), and then press the menu button labeled 1. Make the following changes to the front panel setup:

Set:	A SEC/DIV	10 μs
Select VERTICAL MODE		
Set:	CH 2	Off
	ADD	On
Select CH 1 COUPLING/INVERT		
Set:	INVERT ON:OFF	ON
Select TRIGGER SOURCE		
Set:	CHAN 1:2	1
Select CURSOR FUNCTION		
Set:	VOLTS	On
Menu displayed: ATTACH CURSORS TO:		
Set:	ADD	On
Select STORAGE ACQUIRE		
Set:	AVG	On

NOTE

When the Initial Front Panel Setup is recalled in part a, the CH 1 and CH 2 traces will be centered vertically. DO NOT adjust the CH 1 or CH 2 POSITION controls during the remainder of this CMRR check to avoid exceeding the dynamic range of the CH 1 and/or CH 2 Vertical systems. If the controls are accidently adjusted, go back to part a and repeat this check.

b. Connect a 50 kHz reference frequency signal from the Leveled Sine-Wave Generator to the CH 1 OR X and CH 2 OR Y input connectors via a 50 Ω BNC cable and a Dual-Input Coupler.

c. Set the generator output level for a 5-division display of the reference signal on CH 1.

d. Set the CH 1 and CH 2 VOLT/DIV controls to 50 mv.

e. Select VERTICAL MODE and set CH 1 off.

f. Select CH 2 VARIABLE and, using the menu buttons under the arrow symbols, adjust for minimum ADD display amplitude.

g. Set the A SEC/DIV control to 20 ns.

h. Set the generator output frequency to 50 MHz.

i. Using the CURSOR/DELAY control, align the movable cursor (segmented) to the bottom of the ADD waveform.

j. Press CURSOR/SELECT to enable the alternate cursor.

k. Use the CURSOR/DELAY control to align this cursor to the top of the ADD waveform. Take care to use the same reference points (top edge, bottom edge, or center) of the waveform and cursor as in part i.

l. CHECK—That the cursor readout (upper right corner of display) indicates 50.0 mV or less.

m. Set the generator output frequency back to 50 kHz.

n. Set the VARIABLE menu back to CAL and return the A TIME/DIV control to 10 μs.

o. Select CH 1 COUPLING/INVERT and set INVERT ON:OFF to OFF.

p. Select CH 2 COUPLING/INVERT and set INVERT ON:OFF to ON.

q. Repeat parts f through l to check CMRR with CH 2 inverted. Be sure to use the CH 2 VARIABLE for part f (cursor readout will be in DIV instead of V units if CH 1 VARIABLE is used).

r. Remove the test setup.

8. Check Channel Isolation.

a. Recall the Initial Front Panel Setting by performing the following sequence: Select SAVE/RECALL SETUP, press the menu button labeled RECALL (menu will change), and then press the menu button labeled 1. Make the following changes to the front panel setup:

Set:	A SEC/DIV	5 ns

Select CURSOR FUNCTION

Set:	VOLTS	On

(The ATTACH CURSOR menu will be displayed.)

NOTE

When the Initial Front Panel Setup is recalled in part a, the CH 1 and CH 2 traces will be centered vertically. DO NOT adjust the CH 1 or CH 2 POSITION controls during the remainder of this Channel Isolation check to avoid exceeding the dynamic range of the CH 1 and/or CH 2 Vertical systems. If the controls are accidently adjusted, go back to part a and repeat this check.

b. Connect the Leveled Sine-wave Generator to the CH 1 OR X input connector via a 50 Ω BNC cable.

c. Set the generator frequency to 100 MHz and adjust the output level for a 5-division display.

d. Set the CH 1 and CH 2 VOLTS/DIV controls to 50 mV.

e. Using the CURSOR/DELAY control, align the movable cursor (segmented) to the bottom of the CH 2 waveform.

f. Press CURSOR/SELECT to enable the alternate cursor.

g. Use the CURSOR/DELAY control to align this cursor to the top of the CH 2 waveform. Take care to use the same reference points (top edge, bottom edge, or center) of the waveform and cursor as in part e.

h. CHECK—That the cursor readout (upper right corner of display) indicates 5.00 mV or less.

i. Change the CH 1 VOLTS/DIV control to 100 mV, increase the generator frequency to 150 MHz, and readjust the output level for a 5-division display. Return the CH 1 VOLTS/DIV control to 50 mV.

j. Repeat parts e through h (using 10.00 mV as the limit for part h) to check 150 MHz Channel Isolation.

k. Move the cable to CH 2.

l. Select TRIGGER SOURCE and set CHAN 1⁝2 to 2.

m. Return both VOLTS/DIV controls to 100 mV.

n. Repeat parts c through j, using the cursors to measure the CH 1 waveform. Use the CH 2 VOLTS/DIV control instead of CH 1's for part i.

o. Disconnect the test setup.

9. Check the CH 2 Output Voltage Accuracy and Bandwidth.

a. Recall the Initial Front Panel Setting by performing the following sequence: Select SAVE/RECALL SETUP, press the menu button labeled RECALL (menu will change), and then press the menu button labeled 1. Make the following changes to the front panel setup:

Set:	CH 1 VOLTS/DIV	20 mV

Select CH 2 COUPLING/INVERT

Set:	50 Ω ON⁝OFF	OFF

Select TRIGGER SOURCE

Set:	CHAN1⁝2	2

Select CURSOR FUNCTION

Set:	VOLTS	On

Menu displayed: ATTACH CURSORS TO:

Set:	CH 1	On

b. Connect the Calibration Generator STD AMPLITUDE output to the CH 2 OR Y input connector via a 50 Ω cable. Do not use a termination.

c. Set the Calibration Generator STD AMPLITUDE output level to 0.5 V.

d. Use the CH 2 VERTICAL POSITION control to align the bottom of the displayed waveform to the graticule line three divisions below graticule center.

e. Use the generator VARIABLE AMPLITUDE control to adjust the CH 2 display for precisely 5 divisions amplitude.

f. Connect the CH 2 OUT connector (on the rear panel) to the CH 1 OR X input connector via a 50 Ω BNC cable. Do not use a terminator.

g. Select VERTICAL MODE and set CH 2 off.

h. Use the CH 1 VERTICAL POSITION control to align the bottom of the displayed waveform to the graticule line three divisions below graticule center.

i. Using the CURSOR/DELAY control, align the movable cursor (segmented) to the bottom of the CH 1 waveform.

j. Press CURSOR/SELECT to enable the alternate cursor.

k. Use the CURSOR/DELAY control to align this cursor to the top of the CH 1 waveform. Take care to use the same reference points (top edge, bottom edge, or center) of the waveform and cursor as in part i.

l. CHECK—That the cursor readout (upper right corner of display) indicates 45.00-55.00 mV.

m. Select CH 1 COUPLING/INVERT and set 50 Ω ON/OFF to OFF.

n. Align the cursors to the displayed waveform as in parts i and k.

o. CHECK—That the cursor readout indicates 90.00-110.00 mV. Set 50 Ω ON/OFF back to ON.

p. Disconnect the 50 Ω cable from the Calibration Generator output and connect it to the output of a Leveled Sine-Wave Generator.

q. Select CH 2 COUPLING/INVERT and set 50 Ω ON/OFF to ON.

r. Set the A SEC/DIV control to 200 ns.

s. Set the generator output level for a 6 division display at the 3 MHz reference frequency, then change the output frequency to 50 MHz. Adjust the CH 1 VERTICAL POSITION control as required to view the display.

t. Set the A SEC/DIV control to 5 ns.

u. CHECK—The display amplitude is 4.2 divisions or greater.

v. Disconnect the 50 Ω cable from the CH 2 input.

w. Select CH 1 COUPLING/INVERT and set GND on. Set the A SEC/DIV control to 500 μs.

x. Use the CH 1 VERTICAL POSITION control to align the grounded trace to the center horizontal graticule line.

y. Set the CH 1 VOLTS/DIV to 5 mV and the CH 1 COUPLING to DC.

z. VERIFY—That the trace is within ±2 divisions of the center graticule line.

aa. Disconnect test setup.

10. Check Display Versus Graticule Centering and Dot Versus Vector Display Offset. Check VECTOR Response for NORMAL and ENVELOPE Acquisition Modes.

a. Recall the Initial Front Panel Setting by performing the following sequence: Select SAVE/RECALL SETUP, press the menu button labeled RECALL (menu will change), and then press the menu button labeled 1. Make the following changes to the front panel setup:

Select VERTICAL MODE		
Set:	CH 2	Off
Select CH 1 COUPLING/INVERT		
Set:	50 Ω ON/OFF	OFF

a. Press the front-panel button labeled SELECT.

b. Set VECTORS ON/OFF to OFF for the displayed menu.

c. CHECK—That the CH 1 trace is no more 0.1 division above or below the center horizontal graticule line.

d. Select CURSOR FUNCTION and set TIME on. Note that one cursor is displayed 4 divisions left, one 4 divisions right of the center graticule line. Do NOT adjust the placement of the time cursors displayed.

e. CHECK—That each cursor is within ±0.1 division of the vertical graticule line at which it is located.

f. Press the menu button labeled TIME to turn off the cursors.

g. Connect the STD AMPL OUTPUT of a Calibration Generator to the CH 1 OR X input connector via a 50 Ω BNC cable.

h. Set the AMPLITUDE control of the generator for a 0.2 V setting.

i. Select STORAGE ACQUIRE and set AVG on.

j. Press the front-panel button labeled SELECT.

k. Toggle the VECTORS ON¦OFF menu button between the ON¦OFF settings while making the check in the following part.

l. CHECK—That the display shifts no more that ±0.05 division while performing part k.

m. Disconnect the Calibration Generator from CH 1 connector.

n. Select SAVE/RECALL SETUP and press the menu button labeled INIT PANEL.

o. Select TRIGGER MODE and set AUTO on.

p. Select STORAGE ACQUIRE and set ENVELOPE on. Repeatedly press the ENVELOPE menu button down until CONT (Continuous) appears above the label.

q. Use the CH 1 VERTICAL POSITION control to move the displayed trace up 3 divisions and down 3 divisions to create a 6-division "filled" envelope on screen.

r. Press the SELECT button (next to the INTENSITY control).

s. CHECK—For no more than 0.06 division change in amplitude between the "filled" envelope and the non-filled envelope as VECTORS ON¦OFF is switched between the ON and OFF settings for the displayed menu.

TRIGGERING SYSTEM

NOTE

The CH 1 and CH 2 Trigger Level Readout Accuracies are checked in the Vertical System subsection.

In this procedure, a "stable trigger" refers to a consistent trigger; that is, one that results in a uniform, regular display triggered on the selected slope (±). A stably-triggered display should NOT have the trigger point switch between opposite slopes on the waveform, nor should it "roll" across the screen, as successive acquisitions occur. At TIME/DIV setting of 2 ms/DIV and faster, the TRIG'D LED is constantly lit if display is stably triggered (note that for Tables 4-3 and 4-4, the LED will flash for the 10 ms/DIV checks).

Equipment Required (See Table 4-1):

Leveled Sine-Wave Generator (Item 1)	Termination (Item 11)
Time-Mark Generator (Item 3)	5X Attenuator (Item 13)
Function Generator (Item 4)	10X Probe (Item 16)
Coaxial Cable (Item 9)	Dual-Input Coupler (Item 18)
Precision Coaxial Cable (Item 10)	

1. Check A and B Internal Source Trigger Sensitivity.

NOTE

This step checks the CH 1 trigger source for all trigger coupling settings for both A and B Horizontal Modes. The other sources are checked for DC coupling only. Normally, checking all coupling modes for one trigger source is adequate since all the sources share common coupling circuitry; other sources need only be checked in the DC trigger coupling setting to verify their signal paths. However, if a source's trigger sensitivity is very near the limits specified in Table 4-3, this procedure will specify additional checks for the other trigger coupling settings.

a. Recall the Initial Front Panel Setting by performing the following sequence: Select SAVE/RECALL SETUP, press the menu button labeled RECALL (menu will change), and then press the menu button labeled 1. Make the following changes to the front panel setup:

Select VERTICAL MODE
Set: CH 2 Off

Select CH 1 COUPLING/INVERT
Set: 50 Ω ON/OFF OFF

Select CH 2 COUPLING/INVERT
Set: 50 Ω ON/OFF OFF

b. Connect the sine-wave output of the appropriate generator through a 50 Ω cable and a 50 Ω terminator to the CH 1 input connector. Use the Function Generator (item 4) for Test Frequencies below 50 MHz; use the Leveled Sine-Wave Generator (item 1) for Test Frequencies 50 MHz and higher.

c. Adjust the generator output frequency to the first Test Frequency setting specified in Table 4-3.

d. Set the SEC/DIV control to the setting used with the Test Frequency.

e. Set the output amplitude of the specified Test Frequency to the level given in Table 4-3 for the A Trigger System with DC Trigger Coupling.

NOTE

When amplitudes of less than 1 division are required, adjust the generator for 10X the specified amplitude with the CH 1 VOLT/DIV set to 100 mV and change the setting to 1 V before making the checks. For amplitudes ⩾ 1 division, simply adjust for the required amplitude with the VOLTS/DIV set to 100 mV.

f. Select TRIGGER CPLG to display the A COUPLING menu.

Table 4-3

Minimum Display Level for CH 1 or CH 2 Triggering (in divisions)

Trigger System	Test Frequency	SEC/DIV Setting	TRIGGER COUPLING				
			DC	AC	NOISE REJ	HF REJ	LF REJ
A	60 Hz	10 ms	0.35	0.35	a	a	(0.35)[b]
B	60 Hz	10 ms	0.70	0.70	a	a	(0.70)[b]
A	30 kHz	20 μs	0.35	0.35	a	0.5	a
B	30 kHz	20 μs	0.70	0.70	a	1.0	a
A	80 kHz	10 μs	0.35	0.35	a	a	0.5
B	80 kHz	10 μs	0.70	0.70	a	a	1.0
A	50 MHz	20 ns	0.35	0.35	1.2	(1.2)[b]	0.5
B	50 MHz	20 ns	0.70	0.70	2.4	(2.4)[b]	1.0
A	150 MHz	5 ns	1.0	1.0	3.0	(3.0)[b]	1.0
B	150 MHz	5 ns	1.0	1.0	6.0	(6.0)[b]	2.0
ADD Vertical Mode							
A	150 MHz	5 ns	1.5	1.5	4.5	a	1.5
B	150 MHz	5 ns	3.0	3.0	9.0	a	3.0

[a]Not necessary to check.
[b]Not triggered at the specified amplitude.

g. CHECK—For a stable, triggered display on both + and − slopes for all TRIGGER COUPLING settings that are specified at the present Test Frequency.

h. CHECK—For no stable trigger (display free-runs) for any TRIGGER COUPLING setting in Table 4-3 specifying footnote b, "Not Triggered at specified amplitude."

i. Change the generator output amplitude as necessary and repeat parts g through h for any Trigger Coupling setting specifying a different Minimum Display Level for triggering other that the initial setting for that row. (For example, NOISE, HF, and LF settings usually—but not always—require different amplitudes than the initial setting.)

j. Set the generator output to the next Test Frequency in Table 4-3.

k. Repeat parts d through j (skip part f) to check A Triggers for each test frequency setting in Table 4-3. Change generators (as specified in part a) as needed to obtain the test frequency required. Return the TRIGGER COUPLING menu to DC when completed.

l. Select VERTICAL MODE and set CH 1 off and CH 2 on.

m. Repeat parts b through k to check CH 2 triggers, using CH 2 control settings and input connector. Skip parts f, h and i and check only for DC trigger coupling in part g if the DC trigger sensitivity is NOT near the specified limits; otherwise, check as for CH 1.

n. Select VERTICAL MODE and set ADD on and CH 2 off.

o. Repeat parts b through k to check ADD triggers, using CH 2 control settings and input connector. Skip parts h and i and check only for DC trigger coupling in part g if the DC trigger sensitivity is NOT near the specified limits; otherwise, check as for CH 1.

p. Select VERTICAL MODE and set ADD off and CH 1 on.

q. Set TRIGGER CPLG back to DC and set the HORIZONTAL MODE to B.

r. Press A/B TRIG to select the B Trigger System (the B COUPLING menu will be displayed).

s. Repeat part b through o to check B triggers, using the TRIGGER LEVEL control to trigger the display. Use the generator amplitude settings specified in the Trigger System "B" rows of Table 4-3.

NOTE

When checking 50 MHz and 150 MHz Triggers for the B Trigger System, the REPET mode acquisitions can require a long time to complete. When setting the B SEC/DIV control for those Test Frequencies, set the HORIZONTAL MODE to A and set the A SEC/DIV control to the SEC/DIV setting specified in the table. This adjustment will set BOTH A and B Acquisition Systems to the specified SEC/DIV setting and reduce the time required to complete the B REPET acquisition sequence. Set the HORIZONTAL MODE back to B.

t. Disconnect the test setup.

2. Check Trigger Sensitivity for A and B External Sources.

NOTE

This step checks the trigger sensitivity of the external sources for the DC trigger coupling setting only. Normally, checking all coupling modes for one trigger source (checked in step 1 of this subsection) is adequate since all the sources share common coupling circuitry; other sources need only be checked in the DC trigger coupling setting to verify their signal paths. However, if a source's trigger sensitivity is very near the limits specified in Table 4-4, this procedure will specify additional checks for the other trigger coupling settings.

a. Recall the Initial Front Panel Setting by performing the following sequence: Select SAVE/RECALL SETUP, press the menu button labeled RECALL (menu will change), and then press the menu button labeled 1. Make the following changes to the front panel setup:

Select VERTICAL MODE
Set: CH 2 Off

Select CH 1 COUPLING/INVERT
Set: 50 Ω ON:OFF OFF

Select CH 2 COUPLING/INVERT
Set: 50 Ω ON:OFF OFF

b. Connect the sine wave output of the appropriate generator through a 50 Ω cable, a 5X attenuator, a 50 Ω terminator (install terminator between the 5X attenuator and the Dual-Input Coupler), and a Dual-Input Coupler to the CH 1 and the EXT TRIG 1 input connectors. Use the Function Generator (item 4) for test frequencies below 50 MHz; use the Leveled Sine-Wave Generator (item 1) for test frequencies 50 MHz and higher.

c. Select TRIGGER SOURCE and set EXT 1:2 to 1.

d. Press the A/B TRIG button to select the B Trigger System (the B TRIG SOURCE menu will be displayed) and set EXT 1:2 to 1. Press the A/B TRIG button to return to the A Trigger System.

e. Adjust the generator output frequency to the first Test Frequency setting specified in Table 4-4.

f. Set the A SEC/DIV control to the setting used with that Test Frequency.

g. Set the CH 1 VOLTS/DIV control to the setting used with that Test Frequency setting.

h. Select TRIGGER CPLG to display the A COUPLING menu.

NOTE

The Minimum Signal Amplitude Level for Triggering for EXT TRIG GAIN = 5 are 5X the levels listed in Table 4-4. This procedure obtains the 5X levels by removing a 5X attenuator from the test setup after setting the generator output level as specified in Table 4-4.

Table 4-4

Minimum Signal Level for EXT1 or EXT2 Triggering (in millivolts)

Trigger System	Test Frequency	VOLTS/DIV Setting	SEC/DIV Setting	TRIGGER COUPLING				
				DC	AC	NOISE REJ	HF REJ	LF REJ
A	60 Hz	5 mV	10 ms	17.5	17.5	[a]	[a]	(17.5)[b]
B	60 Hz	5 mV	10 ms	35.0	35.0	[a]	[a]	(35.0)[b]
A	30 kHz	5 mV	20 μs	17.5	17.5	[a]	25	[a]
B	30 kHz	5 mV	20 μs	35.0	35.0	[a]	50	[a]
A	80 kHz	10 mV	10 μs	17.5	17.5	[a]	[a]	25
B	80 kHz	10 mV	10 μs	35.0	35.0	[a]	[a]	50
A	50 MHz	10 mV	20 ns	17.5	17.5	60	(60)[b]	25
B	50 MHz	10 mV	20 ns	35.0	35.0	120	(120)[b]	50
A	150 MHz	50 mv	5 ns	50.0	50.0	150	(150)[b]	50
B	150 MHz	50 mV	5 ns	100.0	100.0	300	(300)[b]	100

[a]Not necessary to check.
[b]Not triggered at specified amplitude.

i. Set the output amplitude of the specified Test Frequency to the level given in Table 4-4 for the A Trigger System with DC Trigger Coupling.

j. CHECK—For a stable, triggered display at the DC trigger coupling setting. Press TRIGGER SLOPE to check for both + and − slopes.

k. Remove the 5X attenuator from the test setup and reconnect the setup as in part b.

l. Set CH 1 VOLTS/DIV for an on-screen display.

m. Select EXT TRIG GAIN and set EXT1 ÷ 5 on.

n. Select TRIGGER CPLG and repeat part j to check A EXT1 ÷ 5 coupling.

o. If trigger sensitivity was near the specified limits for the EXT1 or EXT1 ÷ 5 sources with the trigger coupling set to DC on, repeat parts i through n for all other coupling settings in that test-frequency row, changing the trigger coupling settings and generator amplitude as required.

p. Set the generator output to the next Test Frequency in Table 4-4.

q. Select EXT TRIG GAIN and set EXT 1 back on. Reinstall the 5X attenuator in the test setup.

r. Repeat parts f through q to check the trigger sensitivity for each test frequency in Table 4-4. Use the Function Generator for frequencies below 50 MHz; use a Leveled Sine-Wave Generator for frequencies equal to or above 50 MHz.

s. Move the leg of the Dual-Input Connector from the EXT TRIG 1 input to the EXT TRIG 2 input.

t. Select TRIGGER SOURCE and set EXT 1:2 to 2. Select TRIGGER CPLG.

u. Repeat parts e through r to check the EXT 2 trigger source, setting EXT2 ÷ 5 and EXT 2 in parts m and q, respectively.

v. Select TRIGGER SOURCE and set VERT on (the VERT source will ensure that the A Acquisition System is stably triggered—required for the following B Trigger checks).

w. Press A/B TRIG to select the B Trigger System and set the HORIZONTAL MODE to B.

x. Repeat parts b to u to check B Trigger System sensitivity. Use generator amplitude levels in the Trigger System—B rows for checking the B Trigger sensitivity.

NOTE

When checking 50 MHz and 150 MHz Triggers for the B Trigger System, the REPET mode acquisitions can require a long time to complete. When setting the B SEC/DIV control for those Test Frequencies, set the HORIZONTAL MODE to A and set the A SEC/DIV control to the SEC/DIV setting specified in the table. This adjustment will set BOTH A and B Acquisition Systems to the specified SEC/DIV setting and reduce the time necessary to complete the B REPT acquisition sequence. Set the HORIZONTAL MODE back to B.

y. Disconnect the test setup.

3. Check A*B Trigger Source.

a. Recall the Initial Front Panel Setting by performing the following sequence: Select SAVE/RECALL SETUP, press the menu button labeled RECALL (menu will change), and then press the menu button labeled 1. Make the following changes to the front panel setup:

Set:	A SEC/DIV	10 μs
Select TRIGGER MODE		
Set:	AUTO	On
Select TRIGGER SOURCE		
Set:	A*B:WORD	A*B
Press A/B TRIG to display the B TRIG SOURCE menu		
Set:	CHAN 1:2	2

b. Ensure that the B Trigger Level Readout is set to 0.0 V. Adjust if necessary using the TRIGGER LEVEL control.

c. Press the A/B TRIG button to select the A Trigger System.

d. Select VERTICAL MODE and set CH 2 off.

e. Connect the output of a Leveled Sine-Wave Generator through a 50 Ω cable and a Dual-Input Coupler to the CH 1 and CH 2 input connectors. Do not use a terminator.

f. Set the generator frequency to 50 kHz and its amplitude for a 4 division display.

g. Use the TRIGGER LEVEL control to adjust the A Trigger Level Readout while performing parts h through n.

h. VERIFY—That for Trigger Level Readout settings of approximately ⩽ 0 V the display is stably triggered with the Trigger indicator (a small "T") approximately centered vertically on the waveform.

i. VERIFY—That for Trigger Level settings between approximately 0 V and 200 mV the display is stably triggered and the Trigger Indicator moves along the upper positive-going slope of the waveform.

j. VERIFY—That for settings greater (more positive) than approximately 200 mV the display is not triggered (free-runs). Press A/B TRIG to select the B Trigger System and set SLOPE to − (negative).

k. Press A/B TRIG to select the A Trigger System and set SLOPE to − (negative).

l. VERIFY—That for Trigger Level Readout settings of approximately ⩾ 0 V, the display is stably triggered with the Trigger indicator approximately centered vertically on the waveform.

m. VERIFY—That for Trigger Level settings between approximately 0 mV and −200 mV, the display is stably triggered and the Trigger Indicator moves along the lower negative-going slope of the waveform.

n. VERIFY—That for settings less (more negative) than approximately 200 mV the display is not triggered (free-runs).

o. Set the A Trigger Level Readout for a reading of 0.0 V and set SLOPE to + (positive).

p. Press A/B TRIG to select the B Trigger System and set SLOPE to + (positive).

q. Repeat parts h through o to verify the B Trigger System as a source for the A*B composite trigger. Do NOT change the HORIZONTAL MODE to B. Note that the Trigger Level Readout will indicate B Trigger Level settings for parts h through o and that performance of part j will select the A Trigger System, while part k will select the B Trigger System.

r. Disconnect the test setup.

4. Verify the Normal and Single Sequence Trigger Functions.

a. Recall the Initial Front Panel Setting by performing the following sequence: Select SAVE/RECALL SETUP, press the menu button labeled RECALL (menu will change), and then press the menu button labeled 1. Make the following changes to the front panel setup:

Select VERTICAL MODE		
Set:	CH 2	Off
Set:	A SEC/DIV	10 μs

b. Connect the Leveled Sine-Wave Generator output to CH 1 input through a 50 Ω cable.

c. Set the generator frequency and amplitude for a 50 kHz, 4 division display.

d. Select TRIGGER MODE and set NORMAL on.

e. Using the TRIGGER LEVEL control, VERIFY that the display can be triggered on the positive-going slope of the ac waveform for the + (plus) selection of the SLOPE button and on the negative-going slope for the − (minus) selection of the SLOPE button.

f. VERIFY—That for TRIGGER LEVEL settings outside the range of the display (approximately ±200 mV), the acquisition stops and the waveform is saved on screen.

g. Trigger the display and set SINGLE SEQUENCE on.

h. VERIFY—That for each press of the STORAGE ACQUIRE button, a waveform is acquired and saved on screen.

i. Disconnect the test setup.

5. Check Trigger Noise Rejection.

a. Recall the Initial Front Panel Setting by performing the following sequence: Select SAVE/RECALL SETUP, press the menu button labeled RECALL (menu will change), and then press the menu button labeled 1. Make the following changes to the front panel setup:

Select VERTICAL MODE		
Set:	CH 2	Off
Set:	A SEC/DIV	10 μs

b. Connect the sine wave output of the Function Generator through a 50 Ω cable and a 50 Ω terminator to the CH 1 input connector.

c. Set the generator frequency to 50 kHz and its amplitude for a 4 division display.

d. Change CH 1 VOLTS/DIV to 1 V (yields a 0.4 division display).

e. Select TRIGGER COUPLING and set NOISE REJECT on.

f. CHECK—For a non-triggered, free-running display for both the + (positive) and − (negative) settings of the SLOPE button.

g. Set the A COUPLING menu back to DC on.

h. Press the A/B TRIG button to select the B Trigger System (the B COUPLING menu will be displayed) and set the HORIZONTAL MODE to B.

i. Set the B COUPLING menu to NOISE REJECT on.

j. CHECK—That the display cannot be stably triggered with the TRIGGER LEVEL control for either positive or negative setting of the SLOPE button.

k. Set the B COUPLING menu to DC on and disconnect the test setup.

6. Check Slope Selection and Verify Line Trigger.

a. Recall the Initial Front Panel Setting by performing the following sequence: Select SAVE/RECALL SETUP, press the menu button labeled RECALL (menu will change), and then press the menu button labeled 1. Make the following changes to the front panel setup:

Select VERTICAL MODE		
Set:	CH 2	Off
Select CH 1 COUPLING/INVERT		
Set:	50 Ω ON/OFF	OFF
Set:	CH 1 VOLTS/DIV	5 V
	A SEC/DIV	5 ms
Select TRIGGER SOURCE		
Set:	LINE	On

CAUTION

DO NOT connect the probe ground lead to the ac (line) power source when performing this step.

b. Connect a 10X probe to the CH 1 input connector and connect the probe tip to an ac (line) source.

c. Using the TRIGGER LEVEL control, VERIFY that the display can be triggered on the positive-going slope of the ac waveform for the + (plus) selection of the SLOPE button and on the negative-going slope for the − (minus) selection of the SLOPE button.

NOTE

The Trigger Point Indicator, a small "T" riding on the displayed waveform, indicates the point the instrument is triggered on for the displayed waveform.

d. Disconnect the test setup.

7. Verify A and B Trigger Position Function.

a. Recall the Initial Front Panel Setting by performing the following sequence: Select SAVE/RECALL SETUP, press the menu button labeled RECALL (menu will change), and then press the menu button labeled 1. Make the following changes to the front panel setup:

Select VERTICAL MODE		
Set:	CH 2	Off
Set:	CH 1 VOLTS/DIV	1 V

b. Connect the MARKER output of the Time Mark Generator to the CH 1 input through a 50 Ω cable.

c. Set the generator marker period to 1 ms.

d. Position the start of the display to the extreme left graticule line.

e. Select TRIG POSITION and set 1/8 on.

f. VERIFY—That the Trigger Point Indicator (a "T" symbol on screen) is positioned on a time marker approximately 2.5 divisions to the right of the extreme left graticule line.

g. Set the TRIGGER POSITION menu to 1/4 and verify that the Trigger Point Indicator moves to a time marker that is approximately at center screen.

h. Use the HORIZONTAL POSITION control to position the time marker with superimposed Trigger Point Indicator to the extreme left graticule line.

i. Set the TRIGGER POSITION menu to 1/2 and verify that the Trigger Point Indicator moves to a time marker that is approximately at center screen.

j. Use the HORIZONTAL POSITION control to position the time marker with superimposed Trigger Point Indicator to the extreme left graticule line.

k. Set the TRIGGER POSITION menu to 3/4 and verify that the Trigger Point Indicator moves to a time marker that is approximately at center screen.

l. Set the TRIGGER POSITION menu to 7/8 and verify that the Trigger Point Indicator is positioned on a time marker approximately 2.5 divisions to the right of the center graticule line.

m. Press A/B TRIG to select the B Trigger System and set the HORIZONTAL mode to B. Use the TRIGGER LEVEL control to trigger the display as required.

n. Repeat parts d through k to check the B TRIGGER POSITION function.

o. Disconnect the test setup.

HORIZONTAL SYSTEM

Equipment Required (See Table 4-1):

Time-Mark Generator (Item 3)	Termination (Item 11)
Coaxial Cable (Item 9)	10X Probe (Item 16)
Precision Coaxial Cable (Item 10)	1X Probe (Item 17)

1. Verify the Sample Rate of the A and B Time Bases.

a. Recall the Initial Front Panel Setting by performing the following sequence: Select SAVE/RECALL SETUP, press the menu button labeled RECALL (menu will change), and then press the menu button labeled 1. Make the following changes to the front panel setup:

Select VERTICAL MODE

Set:	CH 2	Off
Set:	CH 1 VOLTS/DIV	1 V
	A SEC/DIV	500 ns
	A/B TRIG	B

b. Select TRIGGER MODE and set RUNS AFTER on. Set A/B TRIG to A.

c. Connect the MARKER OUT signal of a Time Mark Generator to the CH 1 input through a 50 Ω cable. Do not use a terminator.

d. Set the generator marker period to 0.5 μs.

e. VERIFY—That one time marker per horizontal division is displayed.

f. Set HORIZONTAL MODE to B and set the B SEC/DIV control to 500 ns.

g. VERIFY—That one marker per horizontal division is displayed.

h. Rotate the A and B SEC/DIV control counterclockwise one position to set both acquisition systems one speed slower.

i. Set the generator marker period to match the acquisition rate set in the last part.

j. VERIFY—That one marker per horizontal graticule line is displayed.

k. Set HORIZONTAL MODE to A.

l. VERIFY—That one marker per horizontal division is displayed.

m. Set HORIZONTAL MODE to B.

n. Repeat parts h through m to verify all A and B acquisition rate settings down to 500 ms.

o. Disconnect the test setup.

2. Verify the DELAY TIME and Δ DELAY TIME Functions and Check DELAY TIME and Δ DELAY TIME Resolution.

a. Recall the Initial Front Panel Setting by performing the sequence: Select SAVE/RECALL SETUP, press the menu button labeled RECALL (menu will change), and then press the menu button labeled 1. Make the following changes to the front panel setup:

Select VERTICAL MODE

Set:	CH 2	Off
Set:	CH 1 VOLTS/DIV	1 V
	A SEC/DIV	50 μs
	HORIZONTAL MODE	A INTEN
	B SEC/DIV	500 ns
	A/B TRIG	B

b. Select TRIGGER MODE and set RUNS AFTER on. Set A/B TRIG to A.

c. Use the HORIZONTAL POSITION control to align the Trigger Point Indicator (a small "T" on the displayed trace) to the vertical graticule line 3 divisions left of center screen.

d. Connect the MARKER OUT signal of a Time Mark Generator to the CH 1 input through a 50 Ω cable. Do not use a terminator.

e. Set the generator marker period to 50 μs.

f. Select DELAY TIME and use the CURSOR/DELAY control to adjust the DELAY TIME Readout for a reading of 300.00 μs.

g. VERIFY—That the intensified zone is on the time marker that is 3 divisions right of center screen.

h. Set the HORIZONTAL MODE to B. VERIFY—The B Trigger Point Indicator is on the rising edge of the displayed time marker.

i. Set the HORIZONTAL MODE to A INTEN and use the HORIZONTAL POSITION control to position the A Trigger Point Indicator to the graticule line 4 divisions left of center screen.

j. Use the CURSOR/DELAY control to adjust the DELAY TIME Readout for a reading of 50.00 μs (the intensified zone will be aligned to the time marker 3 divisions left of center screen).

k. Press the Δ TIME ON/OFF menu button to set Δ TIME ON.

l. Press the DELAY TIME button (toggles between DELAY and Δ DELAY TIME on the displayed menu) to enable the Δ DELAY intensified zone. The DELAY TIME button is located to the right of the CURSOR/DELAY control.

m. Using the CURSOR/DELAY control, adjust the Δ DELAY TIME Readout for a reading of 300.00 μs.

n. VERIFY—That the Δ DELAY intensified zone is on the marker that is three divisions right of center screen.

o. Set the HORIZONTAL MODE to B. VERIFY—That two superimposed time markers are displayed, one with two Trigger Point Indicators on its rising edge. Slightly adjust the CURSOR/DELAY control as necessary to see both markers.

p. Slightly rotate the CURSOR/DELAY control to increase the Δ DELAY TIME reading the least amount possible.

q. CHECK—That the readout can be advanced in increments at least as small as 0.02 μs.

r. Press the CURSOR SELECT button to enable the Δ DELAY TIME readout. Repeat parts p and q to check that readout.

s. Disconnect the test setup.

3. Verify the DELAY EVENTS function.

a. Recall the Initial Front Panel Setting by performing the following sequence: Select SAVE/RECALL SETUP, press the menu button labeled RECALL (menu will change), and then press the menu button labeled 1. Make the following changes to the front panel setup:

Select CH 2 COUPLING/INVERT

Set:	50 Ω ON/OFF	OFF
Set:	CH 1 VOLTS/DIV	1 V
	CH 2 VOLTS/DIV	2 V
	A SEC/DIV	5 ms
	A/B TRIG	B

b. Select TRIGGER MODE and set RUNS AFTER on. Set A/B TRIG to A.

c. Connect the MARKER OUT signal of a Time Mark Generator to the CH 1 input through a 50 Ω cable. Do not use a terminator.

d. Set the generator marker period to 5 ms.

e. Connect the A TRIG (TTL) output at the 2430 rear panel to the CH 2 input connector with a 50 Ω BNC cable. Do not use a terminator.

f. Use the VERTICAL POSITION controls to position the CH 1 and CH 2 displays for easy viewing.

g. Select EXT TRIG GAIN and set EXT1 ÷ 5 on.

h. Press the A/B TRIG button to select the B Trigger System.

i. Select TRIGGER SOURCE and set EXT 1:2 to 1. Press the A/B TRIG button to return to the A Trigger System.

j. Connect the output of a Leveled Sine-Wave Generator to the EXT TRIG 1 input via a 50 Ω BNC cable and a 50 Ω terminator.

k. Set the Leveled Sine-Wave Generator amplitude to 3 volts and its frequency to 2 MHz.

l. Set the HORIZONTAL MODE to B and set the B SEC/DIV control to 50 μs.

m. Use the HORIZONTAL POSITION control to align the Trigger Point Indicators to the graticule line 3 divisions right of center screen.

n. Set the HORIZONTAL MODE to A.

o. Select DELAY EVENTS and set EVENTS ON/OFF to ON. Use the CURSOR/DELAY control to set the EVENTS COUNT to 60001 B TRIGS.

p. VERIFY—That the falling edge of the A Trigger signal displayed in CH 2 is 3 divisions left of center screen.

q. Set the HORIZONTAL MODE to B.

r. VERIFY—That the rising edge of the displayed time marker can be aligned to the Trigger Point Indicator, approximately 3 divisions right of center screen.

s. Disconnect test setup.

4. Check A and B Time Base Cursor Readout Accuracies

a. Recall the Initial Front Panel Setting by performing the following sequence: Select SAVE/RECALL SETUP, press the menu button labeled RECALL (menu will change), and then press the menu button labeled 1. Make the following changes to the front panel setup:

Set:	CH 1 VOLTS/DIV	1 V
	CH 2 VOLTS/DIV	2 V

Select CURSOR FUNCTION

Set:	TIME	On

b. Use the CURSOR/DELAY control to align the movable cursor (it will have more dots than the alternate cursor) to the third graticule line to the left of center screen.

c. Press CURSOR SELECT to enable the alternate cursor.

d. Use the CURSOR/DELAY control to align cursor to the third graticule line to the right of center screen.

e. CHECK—That the Cursor Time Readout indicates 2.9700 to 3.0300 ms.

f. Set the HORIZONTAL MODE to B.

g. CHECK—That the Cursor Time Readout indicates 2.9700 to 3.0300 ms.

ADDITIONAL VERIFICATIONS AND CHECKS

NOTE

"Equipment Required" Items 21 through 25 are used to check the 2430 TV Option 05 only.

Equipment Required (See Table 4-1):

Calibration Generator (Item 2)	1X Probe (Item 17)
Digital Voltmeter (DMM) (Item 6)	BNC Female-to-Dual Adapter (Item 19)
GPIB Controller (Item 7)	Pulse Generator (Item 21)
GPIB Interface Cable (Item 8)	Sync and Linearity Test Generator (Item 22)
Coaxial Cable (Qty 2) (Item 9)	Sine-Wave Oscillator (Item 23)
Termination (Item 11)	Coaxial Cable (Qty 2) (Item 24)
10X Attenuator (Qty 2) (Item 12)	Termination (Item 25)

1. Verify the XY Display Mode and Plot Output.

a. Recall the Initial Front Panel Setting by performing the following sequence: Select SAVE/RECALL SETUP, press the menu button labeled RECALL (menu will change), and then press the menu button labeled 1. Make the following changes to the front panel setup:

Select VERTICAL MODE
Set: YT:XY XY

b. Press the MENU OFF/EXTENDED FUNCTIONS button twice to display the EXTENDED FUNCTION menu. Press the menu button labeled SYSTEM (menu will change) and set BELL ON:OFF to ON for the displayed menu.

c. Connect the PLOTTER X OUTPUT connector (at the rear of the instrument) to the input of a DMM via a 50 Ω cable and a BNC female-to-dual banana adapter. When inputting the adapter to the DMM, put the side with the bump marked 'GND' to the LOW or (−) input jack.

d. Connect a second 50 Ω cable to the PLOTTER Y OUTPUT connector (this cable will connect the PLOTTER Y OUTPUT to the DMM input later).

e. Select OUTPUT and press the menu button labeled FORMAT (menu will change).

f. Press the menu button labeled PLOT (the menu will change and the instrument will enter the SAVE acquisition mode). Immediately press the menu button labeled ABORT to return the X and Y outputs to their HOME position voltage levels.

g. CHECK—That the DMM reads −2.000 V ±100 mV.

h. Disconnect the X OUTPUT connected cable from the BNC female-to-dual banana adapter and connect the Y OUTPUT connected cable to the BNC female-to-dual banana adapter. Repeat parts f and g.

i. Press the menu button labeled FORMAT and set GRAT off for the XY FORMAT menu.

j. Press the menu button labeled PLOT. CHECK—That the DMM reads 0.000 V ±30 mV for a period of approximately 30 seconds. The menu label ABORT will change to PLOT and the bell will chime at the end of the period.

NOTE

Near the end of the 30-second plot period, the DMM reading will exceed (by approximately 5-80 mV) the 0.000 V ±30 mV limits and then change to approximately −2.0 V when the plot period is over. The 5-80 mV change is normal (the 2430 is actually outputting the voltages necessary for plotting the GND and TRIGGER POINT INDICATORS) and is not a failure to meet Performance Requirements specified for the CHECK performed in part j and repeated for part k.

k. Disconnect the Y OUTPUT connected cable from the BNC female-to-dual banana adapter and connect the X OUTPUT connected cable to the BNC female-to-dual banana adapter. Repeat part j.

l. Rotate and hold (for at least 3 seconds) the CH 1 OR X VERTICAL POSITION control clockwise to position the displayed dot to the extreme right of the screen.

m. Rotate and hold (for at least 3 seconds) the CH 2 OR Y VERTICAL POSITION control clockwise to position the displayed dot to the extreme top of the screen.

n. Press the menu button labeled PLOT. CHECK—That the DMM reads 2.000 V ±100 mV for a period of approximately 30 seconds.

o. Disconnect the X OUTPUT connected cable from the BNC female-to-dual banana adapter and connect the Y OUTPUT connected cable to the BNC female-to-dual banana adapter. Repeat part n.

p. Rotate and hold (for at least 3 seconds) the CH 1 OR X VERTICAL POSITION control counterclockwise to position the displayed dot to the extreme left of the screen.

q. Rotate and hold (for at least 3 seconds) the CH 2 OR Y VERTICAL POSITION control counterclockwise to position the displayed dot to the extreme bottom of the screen.

r. CHECK—That the DMM reads −2.000 V ±100 mV for a period of approximately 30 seconds.

s. Disconnect the Y OUTPUT connected cable from the BNC female-to-dual banana adapter and connect the X OUTPUT connected cable to the BNC female-to-dual banana adapter. Repeat part r.

t. Disconnect the test setup.

2. Check Gain Match Between NORMAL and Save Acquisition Modes.

a. Recall the Initial Front Panel Setting by performing the following sequence: Select SAVE/RECALL SETUP, press the menu button labeled RECALL (menu will change), and then press the menu button labeled 1. Make the following changes to the front panel setup:

Select CH 1 COUPLING/INVERT
Set: 50 Ω ON:OFF OFF

Select STORAGE ACQUIRE
Set: AVG On

Select VERTICAL MODE
Set: CH 2 Off

b. Connect the Calibration Generator STD AMPLITUDE output to the CH 1 input connector. Set the generator output level to 0.5 V and center the displayed square wave on screen.

c. Select CURSOR FUNCTION and set VOLTS on.

d. Using the CURSOR/DELAY control, align the enabled cursor (segmented) to the top of the displayed square wave.

e. Press CURSOR SELECT to enable the alternate cursor (it will change from solid to segmented). Align the cursor to the bottom of the square wave.

f. Note the CURSOR VOLTS readout value.

g. Select STORAGE SAVE to save the display. Realign the cursors to the saved square wave if required.

h. CHECK—That the CURSOR VOLTS readout value is within 12 mV of the value noted in part f.

i. Disconnect the test setup.

3. Verify the Cursor Units and Functions.

NOTE

This check VERIFIES the functionality of the cursors. The accuracy of the cursor readout is checked in the Vertical and Horizontal Systems subsections of this procedure.

a. Recall the Initial Front Panel Setting by performing the following sequence: Select SAVE/RECALL SETUP, press the menu button labeled RECALL (menu will change), and then press the menu button labeled 1. Make the following changes to the front panel setup:

Select VERTICAL MODE		
Set:	CH 2	Off
Select CH 1 COUPLING/INVERT		
Set:	50 Ω ON¦OFF	OFF
Select TRIGGER MODE		
Set:	AUTO	On
Select CURSOR FUNCTION		
Set:	TIME	On

b. Use the CURSOR/DELAY control to align the enabled time cursor to the vertical graticule line 2 divisions left of center screen.

c. Press the CURSOR SELECT button to enable the alternate cursor (realign the Trigger Point Indicator (small "T") to center screen if necessary) and align it to the graticule line 2 divisions right of center screen.

d. VERIFY—That the cursor readout indicates approximately 2.00 ms.

e. Select CURSOR UNITS and set Δ¦ABS to ABS. VERIFY—That the cursor readout indicates approximately 1.00 ms.

f. Return Δ¦ABS to Δ and set DEGREES on. Press the NEW REF menu button.

g. VERIFY—That the cursor readout indicates approximately 360.00° and that TIME CURSOR REF = indicates approximately 2.00 ms.

h. Set Δ¦ABS to ABS. VERIFY—That the cursor readout indicates approximately 180.00°.

i. Set % on. VERIFY—That the cursor readout indicates approximately 50.00%.

j. Set SEC on and Δ¦ABS to Δ.

k. Select CURSOR FUNCTION and set 1/TIME on. VERIFY—That the cursor readout indicates approximately 500.00 Hz.

l. Set VOLTS on. Select CURSOR UNITS and set dB on.

m. Use the CURSOR/DELAY control to align one VOLTS cursor to the graticule line 2 divisions above center screen and the other VOLTS cursor to the line 2 divisions below center screen. Use the CURSOR SELECT button to toggle between cursors.

n. Press the NEW REF menu button. VERIFY—That the cursor readout indicates 0.0 dB.

o. Align the enabled cursor to the center horizontal graticule line. VERIFY—That the cursor readout indicates approximately −6.00 dB.

p. Connect the CALIBRATOR signal to the CH 1 input connector through a 1X probe.

q. Vertically center the display (do not position horizontally). Use the TRIGGER LEVEL control to trigger the display.

r. Set the CURSOR UNITS menu to VOLTS and select the CURSOR FUNCTION menu. Set V@T on.

s. Position one TIME cursor to 1 division left of center screen; position the other TIME cursor to 1 division right of center screen. VERIFY—That the cursor readout indicates approximately 400.00 mV.

t. Set the CURSOR FUNCTION menu to SLOPE. VERIFY—That the cursor readout indicates approximately 400.00 V/s.

u. Disconnect test setup.

4. Verify STORAGE SAVE Functions.

a. Recall the Initial Front Panel Setting by performing the following sequence: Select SAVE/RECALL SETUP, press the menu button labeled RECALL (menu will change), and then press the menu button labeled 1. Make the following changes to the front panel setup:

Select TRIGGER MODE		
Set:	AUTO	On

b. Use the VERTICAL POSITION controls to place the CH 1 trace 2 divisions above graticule center and the CH 2 trace 2 divisions below graticule center.

c. Select VERTICAL MODE and set ADD on (ADD trace will be at graticule center).

d. Select STORAGE SAVE and press the menu button labeled CH 1 (the menu will change from SAVEREF SOURCE to SAVEREF DESTINATION).

e. Press the menu button labeled REF1 (the menu will change back to SAVEREF SOURCE). Press CH2, REF2, ADD, REF3, REF, REF1, and REF4 in that order (menu will change for each button push) to store CH2 in REF2, ADD in REF3, and REF1 in REF4.

f. Select VERTICAL MODE and set CH 1, CH 2, and ADD off.

g. Select STORAGE DISPLAY REF and press the REF1, REF2, and REF3 buttons. VERIFY—That the REF1 trace is displayed 2 divisions above, the REF2 trace 2 divisions below, and the REF3 trace at center screen.

h. Press the HORIZ POS REF menu button (menu will change) and set REF1 on for the displayed menu. VERIFY—That the HORIZONTAL POSITION control can position the REF1 trace horizontally. Repeat verification for REF2 and REF3.

i. Press the DISPLAY REF menu button to return to that menu. Set REF1 off and REF4 on. VERIFY—That the REF4 trace replaces the REF1 trace.

5. GPIB Functionality Verification.

a. Recall the Initial Front Panel Setting by performing the following sequence: Select SAVE/RECALL SETUP, press the menu button labeled RECALL (menu will change), and then press the menu button labeled 1.

b. Select OUTPUT (the button to the lower right of SEC/DIV control) and press the menu button labeled GPIB SETUP (menu will change).

c. Press the menu button labeled MODE to display that menu.

d. Set T/L on. VERIFY—That the ADDR light is off.

e. Set L/ONLY on. VERIFY—That the ADDR light is on.

f. Set T/ONLY on. VERIFY—That the ADDR light remains on.

g. Set T/L back on.

h. Select OUTPUT and press the menu button labeled GPIB SETUP.

i. Press the menu button labeled ADDR to select that menu.

j. Press the menu button labeled ↑ or ↓ to set the GPIB ADDRESS to 1. The ↑ increments the address and the ↓ decrements it.

k. Select OUTPUT and press the menu button labeled GPIB SETUP. Press the menu button labeled TERM (menu will change).

l. Set either EOI or LF/EOI on according to the specification of the controller.

m. Turn on the controller and enter a program that can deliver commands and queries to, as well as receive response from, the 2430.

n. Connect the GPIB controller to the oscilloscope rear-panel GPIB CONNECTOR using the GPIB cable.

o. Run the program entered in step m.

p. Enter 1 in response to the controller's prompt for the oscilloscope's address (the controller may or may not issue an error code and event number in response).

q. Enter the command RQS ON.

r. Press the instrument POWER button twice to power the instrument OFF and then ON.

s. VERIFY—That all three GPIB STATUS lights illuminate during the power-up sequence.

t. VERIFY—The GPIB STATUS SRQ light is still illuminated when the power-up sequence is finished.

u. Enter a carriage return at the controller.

v. VERIFY—That the GPIB STATUS SRQ light is no longer illuminated.

w. Enter the command LLO. VERIFY—That the LOCK light is illuminated.

x. Enter the following commands on the controller:

1. VMOde ADD:ON
2. CH1 VOLts:1E-1,VARiable:50,POSition:2, COUpling:GND,FIFty:OFF, INVert:ON
3. CH2 VOLts:1E-1,VARiable:50,POSit-2, COUpling:GND,FIFty:OFF, INVert:ON
4. BWLimit TWEnty
5. HORizontal ASEC:1E-3,BSEC:1E-4
6. DLTime DELta:ON,DLY1:1E-3,DLY2:1E-3

y. Enter the command RTL to the controller. VERIFY—That the LOCK light is extinguished.

z. Select BEAMFIND. VERIFY—That front panel STATUS readout indicates the control setting changes sent over the controller in part I have been performed.

aa. Press the MENU OFF/EXTENDED FUNCTIONS button.

ab. VERIFY—That the CH 1 trace is displayed 2 divisions above the center graticule line, with an intensified zone 1 division right of center screen.

ac. VERIFY—That the CH 2 trace is displayed 2 divisions below the center graticule line with an intensified zone 2 divisions right of center screen.

ad. Enter the command VMOde? to the controller.

ae. VERIFY—That the controller display indicates that the oscilloscope VERTICAL MODE setting is CH 1 on, CH 2 on, and ADD on.

af. Disconnect the test setup.

6. Check A TRIGGER and RECORD TRIGGER Outputs for Logic Polarity and Minimum HI/LO (50 Ω loads).

a. Recall the Initial Front Panel Setting by performing the following sequence: Select SAVE/RECALL SETUP, press the menu button labeled RECALL (menu will change), and then press the menu button labeled 1. Make the following changes to the front panel setup:

Set:	CH 1 VOLTS/DIV	200 mV
	CH 2 VOLTS/DIV	200 mV

Select TRIGGER SOURCE

Set:	LINE	On

b. Connect the RECORD TRIGGER OUTPUT (rear panel) to the CH 1 input connector via a 50 Ω cable and a 50 Ω terminator.

c. Connect the TRIGGER OUTPUT (rear panel) to the CH 2 input connector via a 50 Ω cable.

d. Using the CH 1 and CH 2 VERTICAL POSITION controls, position the CH 1 waveform to the top half of the screen and the CH 2 waveform to the bottom half for easy viewing.

e. CHECK—That both of the waveforms are displayed with their falling edges aligned to the Trigger Point Indicator (a small "T" riding on each waveform).

f. Select CURSORS FUNCTION and set VOLTS on.

g. Select CURSOR UNITS and set Δ/ABS to ABS.

h. Use the CURSOR/DELAY control to align the Voltage cursor to the top flat portion of the CH 1 waveform.

i. CHECK—That the Cursor Readout indicates a voltage ⩾ 450 mV.

j. Align the Voltage cursor to the bottom flat portion of the CH 1 waveform.

k. CHECK—That the Cursor Readout indicates a voltage ≤ 150 mV.

l. Press the CURSOR FUNCTION button twice to display the ATTACH CURSORS menu and set CH 2 on for the displayed menu.

m. Repeat parts h through k, aligning the cursor to the CH 2 waveform instead of the CH 1 waveform.

n. Disconnect the test setups.

7. Check Square-Wave Flatness (TV Option 05 only).

NOTE

For this step, use a PG 506 Calibration Generator (Item 2) listed in the equipment required at the beginning of "ADDITIONAL VERIFICATIONS AND CHECK" procedure.

a. Recall the Initial Front Panel Setting by performing the following sequence: Select SAVE/RECALL SETUP, press the menu button labeled RECALL (menu will change), and then press the menu button labeled 1. Make the following changes to the front panel setup:

Select CH 1 COUPLING/INVERT

Set:	50 Ω ON/OFF	OFF

Select CH 2 COUPLING/INVERT

Set:	50 Ω ON/OFF	OFF
Set:	CH 1 VOLTS/DIV	200 mV
	CH 2 VOLTS/DIV	50 mV
	A SEC/DIV	2 ms

Select VERTICAL MODE

Set:	CH 2	Off

b. Connect the fast-rise, positive going square-wave output to the CH1 input connector via a 50-Ω cable and a 50-Ω terminator. The square wave should step from -1 V to 0 V.

c. Set the generator to produce a 60 Hz, five-division display and use the CH 1 POSITION control to center the display as required.

d. Set the CH 1 VOLTS/DIV control to 50 mV.

e. CHECK—Display front-corner aberrations are within 1% (0.2 division or less). Exclude the first 20 ns immediately following the positive-going transition from the measurement.

f. Set CH 2 on and CH 1 off.

g. Move the cable from the CH 1 input connector to the CH 2 input connector.

h. CHECK—Display front-corner aberrations are within 1% (0.2 division or less). Exclude the first 20 ns immediately following the positive-going transition from the measurement.

i. Set the CH2 VOLTS/DIV control to 5 mV.

j. Install a 10X attenuator between the 50 Ω cable and the terminator and reconnect the setup.

k. CHECK—Display front-corner aberrations are within 1% (0.2 division or less). Exclude the first 20 ns immediately following the positive-going transition from the measurement.

l. First set the CH 2 VOLTS/DIV control to 50 mV, then set CH 1 on and CH 2 off.

m. Move the cable from the CH2 input connector to the CH1 input connector. Set the CH1 VOLTS/DIV control to 5 mV.

n. CHECK—Display front-corner aberrations are within 1% (0.2 division or less). Exclude the first 20 ns immediately following the positive-going transition from the measurement.

o. Set the CH 1 VOLTS/DIV control to 200 mV and set the A SEC/DIV control to 10 μs.

p. Remove the 10X attenuator and reconnect the test setup.

q. Set the generator to produce a 15 kHz, 5 division display.

r. Repeat parts d through n to check square-wave flatness at 15 kHz.

s. Disconnect test setup.

8. Check Frequency Response Flatness (FULL and 20 MHz BANDWIDTH Modes) (TV Option 05 only).

a. Recall the Initial Front Panel Setting by performing the following sequence: Select SAVE/RECALL SETUP, press the menu button labeled RECALL (menu will change), and then press the menu button labeled 1. Make the following changes to the front panel setup:

Select CH 1 COUPLING/INVERT		
Set:	50 Ω ON/OFF	OFF
Select CH 2 COUPLING/INVERT		
Set:	50 Ω ON/OFF	OFF
Set:	CH 1 VOLTS/DIV	10 mV
	CH 2 VOLTS/DIV	10 mV
	A SEC/DIV	20 μs
Select VERTICAL MODE		
Set:	CH 2	Off
Select BANDWIDTH		
Set:	20 MHz	On

b. Connect the output of a Leveled Sine-Wave Generator to the CH 1 input connector via a 50 Ω cable, two 10X attenuators, and a 50 Ω terminator.

c. Set the generator to produce a 50 kHz, five- division display.

d. Increase the generator output frequency to 5 MHz and set the A SEC/DIV control to 200 ns.

e. CHECK—Display amplitude is between 4.80 and 5.05 divisions.

f. Set the BANDWIDTH LIMIT menu to FULL. Set the A SEC/DIV control back to 20 μs.

g. Repeat parts c and d.

h. CHECK—Display amplitude is between 4.95 and 5.05 divisions.

i. Increase the generator frequency to 10 MHz and set the A SEC/DIV control to 50 ns.

j. CHECK—Display amplitude is between 4.90 and 5.05 divisions.

k. Increase the generator frequency to 30 MHz and set the A SEC/DIV control to 20 ns.

l. CHECK—Display amplitude is between 4.85 and 5.10 divisions.

m. Set the CH 1 VOLTS/DIV control to 50 mV and the A SEC/DIV control to 20 μs. Set 20 MHz on for the displayed BANDWIDTH menu.

n. Remove one of the 10X attenuators from the test setup.

o. Repeat parts c through l.

p. Set the CH 1 VOLTS/DIV control to 200 mV and the A SEC/DIV control to 20 μs. Set 20 MHz on for the displayed BANDWIDTH menu.

q. Remove the last 10X attenuator from the test setup.

r. Repeat parts c through l.

s. Move the cable from the CH 1 input connector to the CH 2 input connector. Insert the two 10X attenuators back into the test setup.

t. Select VERTICAL MODE and set CH 2 on and CH 1 off. Return the A SEC/DIV control to 20 μs.

u. Select BANDWIDTH and set 20 MHz on.

v. Repeat parts c through r using the CH 2 VOLTS/DIV control.

w. Disconnect the test setup.

9. Check TV Back-Porch Clamp (CH 2 only) (TV Option 05 only).

a. Recall the Initial Front Panel Setting by performing the following sequence: Select SAVE/RECALL SETUP, press the menu button labeled RECALL (menu will change), and then press the menu button labeled 1. Make the following changes to the front panel setup:

Select CH 1 COUPLING/INVERT		
Set:	50 Ω ON:OFF	OFF
Select CH 2 COUPLING/INVERT		
Set:	50 Ω ON:OFF	OFF
Set:	CH 1 VOLTS/DIV	500 mV
	CH 2 VOLTS/DIV	50 mV
	A SEC/DIV	5 ms
Select TRIGGER SOURCE		
Set:	LINE	On
Select BANDWIDTH		
Set:	20 MHz	On

b. Connect the output of a Sine-Wave RC Oscillator to the CH 2 input connector via a 75 Ω cable.

c. Connect the composite sync output of a TV Sync Generator to the CH 1 input connector via a 75 Ω cable and a 75 Ω termination. Select VERTICAL MODE and set CH 1 off.

d. Set the oscillator to produce a 60 Hz, six-division display. Slightly adjust the output frequency of the oscillator to stabilize the 60 Hz display.

e. Set the A SEC/DIV control to 100 μs. Select TRIGGER SOURCE and set CH 1 on.

f. Select SET TV and set CLAMP ON:OFF to ON and TV LINE on.

g. CHECK—The amplitude of the sine wave is 1 division or less.

NOTE

An easy method of checking the expanded 60 Hz sine wave amplitude is to observe the vertical "jitter" of the top of the Trigger Point Indicator (a small "T" riding on the sine wave). The top of the "T" should not jitter more than 1 division.

h. Set the CH 2 VOLTS/DIV control to 100 mV and the A SEC/DIV control back to 5 ms.

i. Set TV CLAMP off for the displayed menu. Select TRIGGER SOURCE and set LINE on.

j. Repeat parts d through g.

k. Set the CH 2 VOLTS/DIV control to 200 mV and the A SEC/DIV control back to 5 ms.

l. Set TV CLAMP off for the displayed menu. Select TRIGGER SOURCE and set LINE on.

m. Repeat parts d through g.

n. Disconnect the test setup.

10. Check TV Back-Porch Clamp Reference (CH 2 only) (TV Option 05 only).

a. Recall the Initial Front Panel Setting by performing the following sequence: Select SAVE/RECALL SETUP, press the menu button labeled RECALL (menu will change), and then press the menu button labeled 1. Make the following changes to the front panel setup:

Select VERTICAL MODE		
Set:	CH 1	Off
Set:	CH 2 VOLTS/DIV	50 mV
	A SEC/DIV	1 μs
Select BANDWIDTH		
Set:	20 MHz	On
Select CH 2 COUPLING/INVERT		
Set:	50 Ω ON:OFF	OFF

b. Connect a 100% modulated, composite video signal to the CH 2 input connector via a 75 Ω cable and a 75 Ω termination. Do NOT adjust the CH 2 POSITION control.

c. Select SET TV and set TV CLAMP on.

d. CHECK—That the back-porch level is within 1 division of the center graticule line.

e. Disconnect the test setup.

11. Check Sync Separation (± SLOPE) (TV Option 05 only).

a. Recall the Initial Front Panel Setting by performing the following sequence: Select SAVE/RECALL SETUP, press the menu button labeled RECALL (menu will change), and then press the menu button labeled 1. Make the following changes to the front panel setup:

Select VERTICAL MODE

Set:	CH 2	Off

Set:	CH 1 VOLTS/DIV	50 mV
	A SEC/DIV	2 μs
	TRIGGER SLOPE	– (Minus)

Select BANDWIDTH

Set:	20 MHz	On

Select CH 1 COUPLING/INVERT

Set:	50 Ω ON/OFF	OFF

b. Connect the square-wave output of a Pulse Generator to the CH 1 input connector via a 50 Ω cable and a 50 Ω termination.

c. Set the amplitude for a 3 division pulse, stepping negative from ground.

d. Use the HORIZONTAL POSITION control to position the Trigger Point Indicator (small "T" riding on the waveform) to the vertical graticule line 4 divisions left of graticule center.

e. Adjust the generator PERIOD control for a 7.5 division (approximately 15 μs) period for the displayed square wave.

f. Adjust the generator PULSE DURATION control until the negative-going portion of the square wave is approximately 1 horizontal division in duration.

g. Switch the A SEC/DIV control to 500 ns.

h. Select CURSOR FUNCTION and set TIME on.

i. Use the CURSOR/DELAY control to align the left-most cursor to the falling edge of the negative-going pulse (aligned to the graticule line in part d).

j. Press CURSOR SELECT to select the right-most cursor and adjust it for a readout of 2.000 μs.

k. Adjust the generator PULSE DURATION until the negative-going portion of the square wave is aligned to the two cursors (i.e., is equal to 2.000 μs).

l. Select TRIGGER CPLG and set TV on.

m. Select SET TV and set TV LINE on.

n. Return the A SEC/DIV control to 2 μs. Press CURSOR SELECT and use the CURSOR/DELAY control to realign the left-most cursor to the falling edge of the pulse.

o. Press CURSOR SELECT and use the CURSOR/DELAY control to adjust the right-most cursor for a readout value of 13.000 μs.

p. Set the CH 1 VOLTS/DIV control to 200 mV.

q. Adjust the generator to reduce the PERIOD of the waveform. Reduce the period until the display is stably triggered, but any further decrease in period causes an unstable display.

r. CHECK—That the negative-going edge of the second negative pulse is located between the two cursors.

s. Adjust the generator to return the waveform PERIOD to 7 1/2 divisions.

t. Select CH 1 COUPLING/INVERT and set INVERT ON/OFF to ON. Switch TRIGGER SLOPE to + (plus).

u. Adjust the generator to reduce the PERIOD of the waveform. Reduce the period until the display is stably triggered, but any further decrease in period causes an unstable display.

v. CHECK—That the positive-going edge of the second negative pulse is located between the two cursors.

w. Disconnect the test setup.

12. Check TV Trigger Modes.

a. Recall the Initial Front Panel Setting by performing the following sequence: Select SAVE/RECALL SETUP, press the menu button labeled RECALL (menu will change), and then press the menu button labeled 1. Make the following changes to the front panel setup:

Select VERTICAL MODE		
Set:	CH 2	Off
Set:	CH 1 VOLTS/DIV	200 mV
	A SEC/DIV	100 μs
	TRIGGER SLOPE	– (Minus)
Select BANDWIDTH		
Set:	20 MHz	On
Select CH 1 COUPLING/INVERT		
Set:	50 Ω ON/OFF	OFF
Select TRIGGER CPLG		
Set:	TV	On
Select SET TV		
Set:	FIELD 1	On

b. Connect the composite sync output of a Sync Generator to the CH 1 input connector via a 75 Ω cable and a 75 Ω termination.

NOTE

For NTSC composite sync input signals, the first field will have 263 lines, while the second field will have 262. The 2430 will display the line number in the extreme upper-right corner of the screen and the TVF (TV Field) number immediately to the right of the line number.

c. Adjust the TRIGGER LEVEL control for a line number reading of 1 and a field number reading of TVF1.

d. CHECK—That the readout Trigger Point Indicator (small "T" riding on the displayed waveform) indicates the 2430 is triggered on the first line of field 1.

e. Rotate the TRIGGER LEVEL control slightly counterclockwise while performing the CHECK during the following part.

f. CHECK—That the readout indicates the highest line number of the previous field for the multi-field input signal. For example, using an NTSC signal, the readout should indicate "TVF2 262."

g. CHECK—That the readout Trigger Point Indicator (small "T" riding on the displayed waveform) indicates the 2430 is triggered on the last line of field 2.

h. Continue to rotate the TRIGGER LEVEL control counterclockwise while performing the CHECK during the following part.

i. CHECK—That the readout indicates progressively lower line numbers are being displayed for field 2, and that eventually the readout indicates the highest line number of the previous field for the multi-field input is being displayed. For example, using an NTSC signal, the readout should indicate "TVF1 263."

j. CHECK—That the readout Trigger Point Indicator (small "T" riding on the displayed waveform) indicates the 2430 is triggered on the last line of field 2.

k. Set the A TV COUPLING (SET TV menu) to ALT.

l. Use the TRIGGER LEVEL control to set the readout to "TVFLD 1," indicating that the first lines of both fields are displayed.

m. CHECK—That the readout Trigger Point Indicator (small "T" riding on the displayed waveform) indicates the 2430 is triggered on the first lines of both fields.

NOTE

By switching A TV COUPLING (SET TV menu) between FIELD 1, FIELD 2, and ALT, it is easier to see which line of which field the 2430 is triggered on for ALT TV COUPLING.

n. Rotate the TRIGGER LEVEL control slightly counterclockwise while performing the CHECK during the following part.

o. CHECK—That the readout indicates the highest line number common to both fields for the multi-field input signal. For example, using an NTSC signal, the readout should indicate "TVFLD 262."

p. CHECK—That the readout Trigger Point Indicator (small "T" riding on the displayed waveform) indicates the 2430 is triggered on the last line COMMON to both fields. See the NOTE following part m above.

q. Disconnect the test setup.

ADJUSTMENT PROCEDURE

INTRODUCTION

IMPORTANT—PLEASE READ BEFORE USING THIS PROCEDURE

This procedure is used to return the instrument to conformance with its "Performance Requirements" as listed in the "Specification" (Section 1). It can also be used to optimize the performance of the instrument. As a general rule, these adjustments should be performed every 2000 hours of operation or once a year if used infrequently.

The Adjustment Procedure consists of three subsections. The first subsection is "Internal Adjustments." Step 1 of this subsection, "Display Adjustments," uses display test patterns generated internally by the instrument. Steps 2 through 5 require external generators to provide signals for the test displays. In all steps of "Internal Adjustments" internal controls must be adjusted (cabinet removal is required). An internal jumper must also be pulled off to enable the menu choices for the Extended Calibration menu. This menu must be enabled to perform "Display Adjustments" as well as the Attenuators and Triggers adjustments called out in the "External Calibration" subsection of this procedure.

The second subsection is "Self Calibration." SELF CAL is a fully automatic procedure initiated by the user from the front panel. No external signals or internal adjustments are required, and beyond starting the procedure, no further action is needed for the user to do a SELF CAL. The instrument cabinet must be installed to obtain a proper SELF CAL, and the Self Calibration subsection must be done and passed before going on to the third subsection of the Adjustment Procedure.

Subsection three is "External Calibration." Here, the user inputs test signals for the Attenuator and Trigger calibration and initiates the semiautomatic routines that use those signals. The internal jumper disabling the Extended Calibration (EXT CAL) menu must be removed to enable the EXT CAL menu choices (as was necessary for the Display Adjustments in "Internal Adjustments" subsection). The instrument cabinet must be installed and the instrument operating at an ambient temperature between +20°C and +30°C for valid calibration of the Attenuators and Trigger circuits.

CALIBRATION SEQUENCE AND PARTIAL PROCEDURES

To completely calibrate this instrument, all steps of this procedure should be performed, completely and in sequence. Individual steps in either the Internal Adjustments or External Calibration subsections can be omitted if a complete calibration is not needed. Individual substeps (parts) in "Display Adjustments" (Internal Adjustments subsection) can be skipped by advancing to the next display.

While a Self Calibration must be performed before doing the External Adjustments, it can also be performed any time the instrument is installed in its cabinet, optimizing the instrument's performance for the existing environment. The internal jumper removed for performance of the Internal Adjustments and External Calibration does not affect Self Calibration.

WARM-UP TIME REQUIREMENTS

The 2430 Oscilloscope requires adequate warm-up time in a 20°C to 30°C environment before performing the calibration routines and adjustments in this procedure. Calibration performed before the operating temperature has stabilized may cause an erroneous calibration. The adjustment procedure indicates the duration of the warm-up periods and the points in the procedure they should be allowed.

PRESERVATION OF INSTRUMENT CALIBRATION

Both the Internal Adjustments and External Calibration subsections require enabling the EXTENDED CALIBRATION menu. Since the internal calibration constants stored by the 2430 can be altered by the user if the EXTENDED CALIBRATION menu is enabled, this menu is disabled by the installation of an internal jumper. REINSTALLATION OF THE INTERNAL JUMPER TO PREVENT INADVERTENT ALTERING OF INTERNAL CALIBRATION CONSTANTS BY USERS IS RECOMMENDED. Performance of a Self Calibration only, without performance of either of the other two subsections, does not require the removal of the jumper or cabinet.

NOTE

The Extended Calibration menu can also be accessed via the GPIB (General Purpose Interface Bus). See "Extended Calibration" in Appendix B and the GPIB information in Appendix A of the 2430 Operators Manual for further information.

INTERNAL ADJUSTMENTS

Equipment Required (See Table 4-1):

- Leveled Sine-Wave Generator (Item 1)
- Calibration Generator (Item 2)
- Coaxial Cable (Item 9)
- Precision Coaxial Cable (Item 10)
- 50 Ω Termination (Item 11)
- 10X Attenuator (Item 12)
- Alignment Tool (Item 15)
- Dual-Input Coupler (Item 18)
- Normalizer (Item 20)

1. Display Adjustments.

a. Remove the cabinet from the instrument (see "Removal and Replacement Procedure" in the "Maintenance" section of this manual). Remove jumper J156 from P156 on the Side Board (on right side of instrument near the front).

NOTE

Operation (for more than a few minutes) of the 2430 without its cabinet installed requires that cooling be provided for the components on the Main board. Use a small fan to direct air across the finned heatsinks on that board. The fan used should have the same airflow capability as the fan used in the 2430. The CFM (cubic feet per minute) specification for the instrument's fan is 35 CFM at 0 H_2O (essentially, open air). Do NOT remove the fan from the 2430 for use in cooling the Main board, as critical components in other sections of the instrument may overheat.

b. Connect the instrument to a suitable power source and power it ON. Allow a 10 minute warm up before performing the rest of this subsection.

c. Press the MENU OFF/EXTENDED FUNCTIONS button once or twice (two presses are necessary if any menu is presently displayed, one press if no menu is displayed) to display the EXT FUNCT Functions menu.

d. Press the menu button labeled CAL/DIAG (menu will change).

e. Press the menu button labeled EXT CAL to display the EXT CAL menu.

f. Press the menu button labeled DISPLAY (Display 1 will appear). (Menu label is ADJUSTS in Version 2.0 firmware.)

g. ADJUST—The ASTIG and FOCUS front panel controls for best definition of the displayed dot.

h. Press any menu button to advance to Display 2.

NOTE

All adjustment controls associated with Displays 2 and 3 that are not designated front panel controls are located between the fan and the high-voltage shield on the left side board of the instrument.

i. ADJUST—R100 (Grid Bias control) as necessary to display two dots. Continue to adjust R100 just until one dot disappears, leaving the other dot displayed.

j. Press any menu button to advance to Display 3.

k. ADJUST—The ASTIG and FOCUS front panel controls and R30 (Edge Focus control) for most uniform focus over the entire displayed pattern.

l. ADJUST—The TRACE ROTATION front panel control to align the horizontal lines of the displayed pattern parallel to the horizontal graticule lines.

m. ADJUST—R305 (the Y-AXIS control) to align the vertical lines of the displayed pattern parallel to the vertical graticule lines.

n. REPEAT—Parts l and m to obtain best overall alignment.

o. ADJUST—R200 (Geometry control) for the least curvature overall of the display lines at the vertical and horizontal edges of the crt screen.

p. ADJUST—R30 (Edge Focus control) for best focus along the edges of the crt screen.

q. Set the INTENSITY control (front panel) for maximum brightness of the display. ADJUST—R400 (Hi-Drive Focus) for best overall focus of the displayed pattern.

r. Return the INTENSITY control to approximately the same setting in effect prior to part p and repeat parts p and q for best focus compromise between the two intensity settings.

s. Press any menu button to advance to Display 4. Note that all adjustment controls associated with this display are located on the top circuit board near the rear of the instrument (see Figure 5-1).

t. ADJUST—R583 (Vertical Spot-wobble control) and R584 (Horizontal Spot-wobble control) for maximum overall definition of the displayed dot pattern (only one dot visible at each graticule line intersection where a dot is displayed).

NOTE

When the Spot-wobble compensation is badly out of adjustment, three dots will be visible at each of the 33 dot locations. ADJUST—R588 or R584 to align the dots in either a vertically or horizontally oriented line, then use the other control to adjust for only one dot at each dot location (all three dots superimposed).

u. Press any menu button to advance to Display 5. Note that all adjustment controls associated with this display are located on the top circuit board near the rear of the instrument (see Figure 5-1).

NOTE

The display generated by performing part s is composed of a "rectangle" of dots, a small "cross" of 5 dots, and a large "cross" of 2 vectors. Calibration for this display consists of aligning the small cross to the large one (parts v and w), then aligning both crosses to the center graticule lines (parts x and y), and finally, adjusting the horizontal sides of the rectangle for 6 divisions of separation and the vertical sides for 8 divisions of separation (parts z and aa). See Figure 5-2 (a and b).

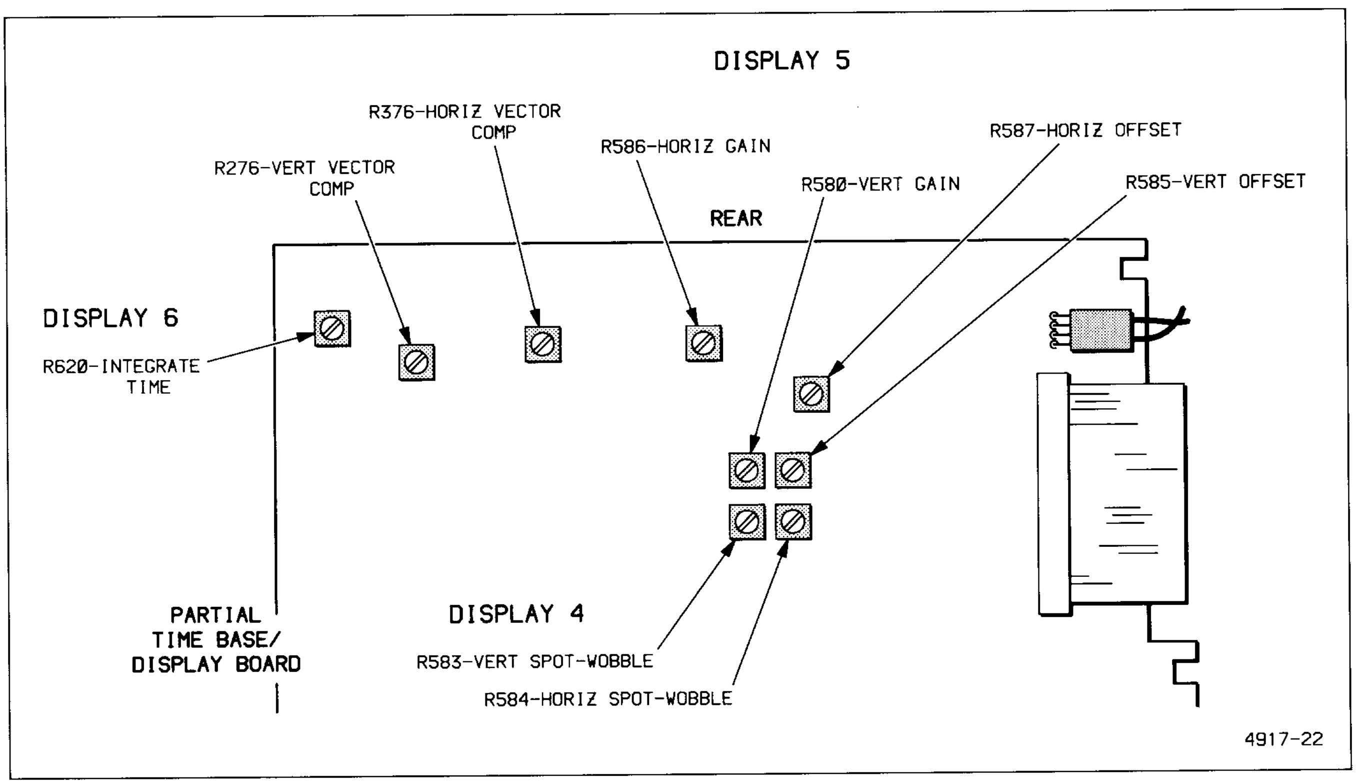
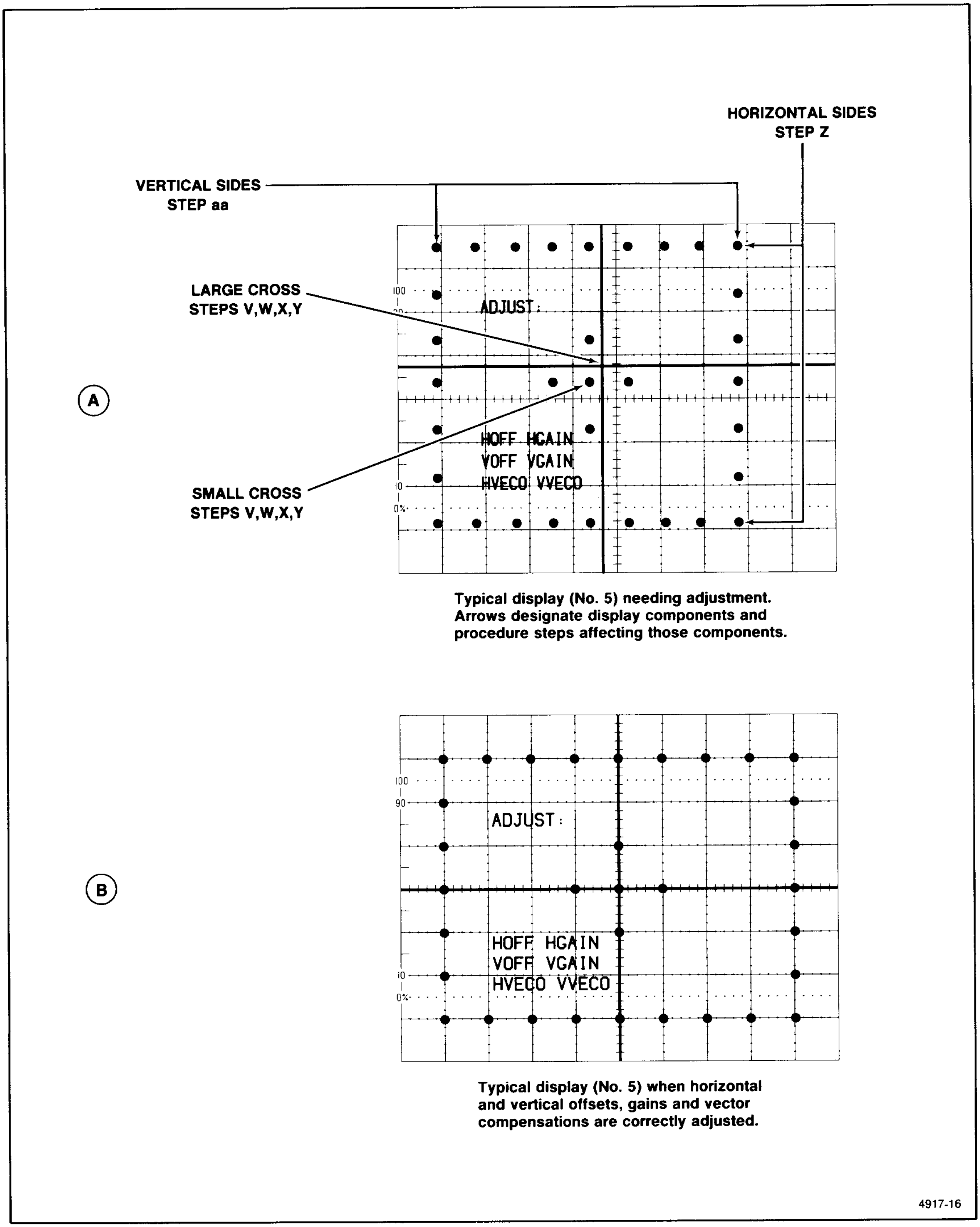


Figure 5-1. Adjustment locations for Displays 4 through 6.



Typical display (No. 5) needing adjustment. Arrows designate display components and procedure steps affecting those components.

Typical display (No. 5) when horizontal and vertical offsets, gains and vector compensations are correctly adjusted.

Figure 5-2 (a and b). Display 5—Vertical and Horizontal Gain, Offset, and Vector Compensation adjustments pattern.

v. ADJUST—R376 (Vertical Vector Compensation control) to align the 3 vertically oriented dots of the small cross pattern to the vertical vector of the large cross pattern.

w. ADJUST—R276 (Horizontal Vector Compensation control) to align the 3 horizontally oriented dots of the small cross pattern to the horizontal vector of the large cross pattern.

x. ADJUST—R585 (Vertical Offset control) to precisely align the horizontal vector of the displayed pattern to the center horizontal graticule line.

y. ADJUST—R587 (Horizontal Offset control) to precisely align the vertical vector of the displayed pattern to the center vertical graticule line.

z. ADJUST—R580 (Vertical Gain control) to space the horizontal sides of the rectangle exactly 6 divisions apart.

aa. ADJUST—R586 (Horizontal Gain control) to space the vertical sides of the rectangle exactly 8 divisions apart.

ab. Press any menu button to advance to Display 6. Note that the adjustment control associated with this display is located on the top circuit board near the left rear corner of the instrument (see Figure 5-1).

ac. ADJUST—R620 (Integrator Time control) for best front corner (minimum roll-up or roll-off) of the high-frequency (filled) portion of the display. See Figure 5-3 for further detail.

ad. Exit the ADJUSTS display by pressing the MENU OFF button and reinstall jumper J156 if an External Calibration is not to be performed.

ae. Skip to Step 2 Sample Skew Adjustment unless the instrument did not meet the LF linearity requirements as specified in the Performance Check and Functional Verification Procedure.

IMPORTANT

READ THE FOLLOWING NOTE BEFORE CONTINUING WITH THIS PROCEDURE

NOTE

The CCD gain adjustments (R768, R769, R877, & R688) as called out in the following steps should only be performed if the instrument did not meet the LF linearity specifications as checked in the Performance Check and Functional Verification Procedure. These adjustments were preset at the factory to their optimum setting and further adjustment may result in reduced instrument performance.

If it has been determined that the CCD gains need to be adjusted, jumper J156 will need to be removed and a COLD START of the instrument will have to be done to preset the CM11, CM13, CM21, and CM23 DAC values to 1400. If a COLD START is performed, this ADJUSTMENT PROCEDURE must be followed with the SELF CAL and EXT Calibration procedures.

af. Push the MENU OFF button once or twice to bring the CRT Display Menus on screen. Perform a COLD START on the instrument and then return to the ADJUSTS displays. Advance through the displays to reach the first CCD gain adjust display, (Display #7).

ag. Adjust the Channel 1 CCD gains (R768 and R769) for approximately four-divisions of each display.

ah. Press any menu button to advance to the Channel 2 CCD gain adjust display.

ai. Adjust the Channel 2 CCD gains (R877 and R688) for approximately four-divisions of each display.

aj. Recheck the LF linearity as described in the Performance Check procedure to see if the instrument now meets specifications. If the instrument passes this check, continue with this Adjustment Procedure. If LF linearity still fails, decrease the CCD gains of the failing channel by approximately one minor division and recheck linearity.

NOTE

For best instrument performance, keep the CCD gains adjusted as close to 4 divisions as possible while meeting the LF linearity checks.

2. Sample Skew Adjustment.

a. If a menu is displayed press the MENU OFF/EXTENDED FUNCTIONS button to remove it from the screen. Select SAVE/RECALL SETUP and press the menu button labeled INIT PANEL. Make the following changes to the front panel setup:

Set: A SEC/DIV 500 ns

Select CH 1 COUPLING/INVERT
Set: 50 Ω ON/OFF ON

Select CH 2 COUPLING/INVERT
Set: 50 Ω ON/OFF ON

b. Connect the output of the Leveled Sine-wave Generator to the CH 1 and CH 2 input connectors via a precision 50 Ω BNC cable and a Dual-Input Coupler.

c. Set the generator output level for a 5 division display at a frequency of 1 MHz, then change the output frequency to 100 MHz.

NOTE

Part a sets the A SEC/DIV control to an acquisition rate (500 ns) lower than required to properly display the 100 MHz sine wave set in part c. Part d requires that the generator output frequency be varied slightly to create an "aliased" display. The aliased sine wave appears as if untriggered and as if its frequency is much lower than the 100 MHz sine wave set in part c. Vary the generator output frequency (part d) until only one or two cycles of the untriggered sine wave are displayed (about ±100 kHz). Use a generator with a highly stable frequency output, such as the TEKTRONIX SG 503.

d. Vary the generator output frequency slightly (if required) to alias the display as outlined in the previous NOTE.

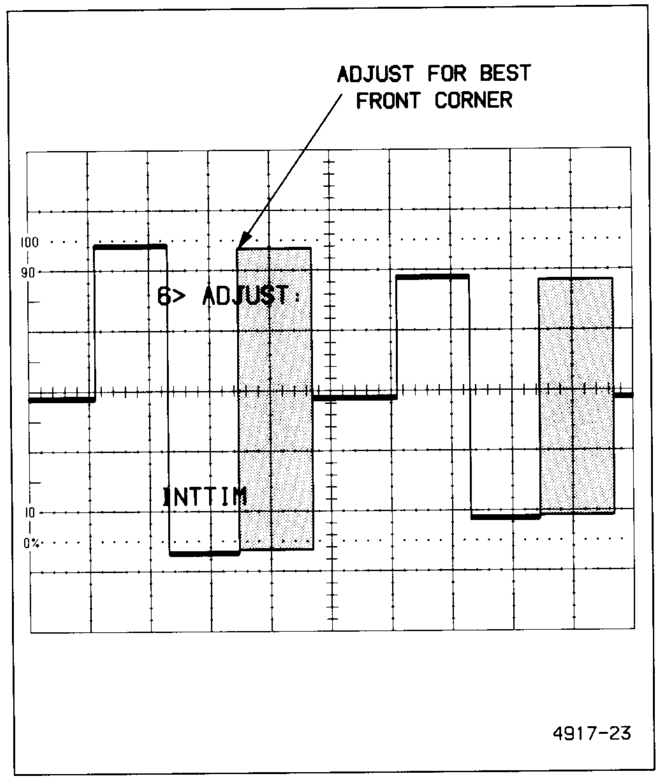


Figure 5-3. Display 6—Integrator Time adjustment pattern.

e. ADJUST—SAM-SKEW (R475) (located near the center-rear edge of the Main board) for best definition (least width or fuzziness) of the rising and falling portions of the sine wave. Adjust for best compromise between the definition of the rising and falling portions of the sine wave.

NOTE

When performing parts e and g, it may be helpful to toggle between the STORAGE ACQUIRE (while making the adjustment) and SAVE (while checking for best definition) modes.

f. Select VERTICAL MODE and set CH 2 on. Use the VERTICAL POSITION controls to position the CH 1 and CH 2 displays for easiest viewing.

g. ADJUST—R475 for best compromise between best definition of the CH 1 and CH 2 displays.

h. Disconnect the test setup.

3. CH 1 and CH 2 Input Capacitance Adjustment (C414 and C311).

a. If a menu is displayed, press the MENU OFF/EXTENDED FUNCTIONS button to remove it from the screen. Select SAVE/RECALL SETUP and press the menu button labeled INIT PANEL. Make the following change to the front panel setup:

Set:	A SEC/DIV	100 μs

b. Connect the HIGH AMPLITUDE output of the Calibration Generator to the CH 1 input connectors via a precision 50 Ω BNC cable, a 50 Ω terminator, and an adjustable normalizer.

c. Set the generator output level for a 6 division display at a frequency of 1 kHz.

d. Set the normalizer for a square front corner over approximately the first 40 μs (0.4 division) of the positive portion of the waveform.

e. Change the CH 1 VOLTS/DIV control to 50 mV and adjust the generator amplitude for a 6 division display.

f. ADJUST—C414 (near the front edge of the Main board) for the same waveform front corner as noted in part d.

g. Repeat parts c through f until no change is observed in the waveform front corner between the 50 mV and 100 mV settings for the CH 1 VOLTS/DIV control.

h. Move the input signal to CH 2. Select VERTICAL MODE and set CH 2 on and CH 1 off.

i. Repeat parts c through g to adjust the CH 2 input capacitance, adjusting C311 in part f and using the CH 2 VOLTS/DIV control for parts e and g.

j. Disconnect the test setup.

4. 50 MHz Bandwidth Limit Filter Adjustment (Non-TV Options Only).

a. If a menu is displayed, press the MENU OFF/EXTENDED FUNCTIONS button to remove it from the screen. Select SAVE/RECALL SETUP and press the menu button labeled INIT PANEL. Make the following changes to the front panel setup:

Set:	A SEC/DIV	50 ns
	CH 1 VOLTS/DIV	10 mV
Select BANDWIDTH		
Set:	50 MHz	On
Select CH 1 COUPLING/INVERT		
Set:	50 Ω ON/OFF	ON
Select STORAGE ACQUIRE		
Set:	REPET ON/OFF	ON
	AVG	On (8)

b. Connect the positive-going, FAST RISE output of the Calibration Generator to the CH 1 input via a precision 50 Ω cable and a 10X attenuator.

c. Set the generator output level for a 5 division display at a frequency of 100 kHz.

d. ADJUST—C431 for as flat a response as possible. This capacitor is located on the Main circuit board.

e. Move the test setup to the CH 2 input connector.

f. Select VERTICAL MODE and set CH 2 on and CH 1 off.

g. Set CH 2 VOLTS/DIV to 10 mv.

h. Repeat parts c and d, adjusting C235 for part d.

i. Disconnect the test setup.

5. 20 and 50 MHz Bandwidth Limit Filter Adjustment (TV-Option 05 Only)

a. If a menu is displayed, press the MENU OFF/EXTENDED FUNCTIONS button to remove it from the screen. Select SAVE/RECALL SETUP and press the menu button labeled INIT PANEL. Make the following changes to the front panel setup:

Set:	A SEC/DIV	50 ns
	CH 1 VOLTS/DIV	10 mV
Select BANDWIDTH		
Set:	20 MHz	On
Select CH 1 COUPLING/INVERT		
Set:	50 Ω ON/OFF	ON
Select STORAGE ACQUIRE		
Set:	REPET ON/OFF	ON
	AVG	On (8)

b. Connect the positive-going, FAST RISE output of the Calibration Generator to the CH 1 input via a precision 50 Ω cable and a 10X attenuator.

c. Set the generator output level for a 5 division display at a frequency of 100 kHz.

NOTE

Adjust the coils in the following parts so their slugs are out approximately the same amount.

d. ADJUST—L431 for as flat a response as possible. This coil is located on the Main circuit board.

e. Move the test setup to the CH 2 input connector.

f. Select VERTICAL MODE and set CH 2 on and CH 1 off.

g. Set the CH 2 VOLTS/DIV control to 10 mV.

h. Repeat parts c and d for CH 2, adjusting L531 for part d.

i. Set the A SEC/DIV control to 100 μs.

j. Connect the Leveled Sine-wave Generator output via a 50 Ω precision cable and two 10X attenuators to the CH 2 input connector.

k. Set the generator to produce a 50 kHz, 5 division display.

l. Increase the generator output to 5 MHz and set the SEC/DIV control to 500 ns.

m. Check that the display amplitude is between 4.80 and 5.05 divisions.

n. Select BANDWIDTH and set 50 MHz on. Set the A SEC/DIV control back to 50 ns.

o. Select VERTICAL MODE and set CH 1 on and CH 2 off.

p. Repeat parts b through h to adjust the 50 MHz bandwidth limit, adjusting C431 and C235 in part d (adjust C431 when adjusting for CH 1, C235 for CH 2). These capacitors are located on the Main board.

q. Disconnect the test setup.

SELF CALIBRATION

Equipment Required:

None

1. Self Calibration

a. Turn the instrument POWER ON and allow a 10 minute warm-up period. Note that the instrument's cabinet should be in place when performing this subsection of this procedure. (If an Internal Calibration was performed and J156 removed, do not reinstall J156 prior to reinstalling the cabinet unless an External Calibration is NOT to be performed after execution of a Self Calibration.)

b. Press the MENU OFF/EXTENDED FUNCTIONS button once or twice (two presses are necessary if any menu is presently displayed, one press if no menu is displayed) to display the Extended Functions menu.

c. Press the menu button labeled CAL/DIAG (menu will change).

d. Press the menu button labeled SELF CAL. "RUNNING" will be displayed in the lower right corner of the crt screen for approximately 10 seconds as the instrument performs its automatic calibration routine.

NOTE

After successful completion of the automatic calibration routine, "RUNNING" will disappear from the crt screen and "PASS" will be displayed above the SELF CAL menu button label. Press the MENU OFF/EXTENDED FUNCTIONS button to return the instrument to control settings in effect before the Self Calibration was initiated. If the automatic calibration routine is NOT successful (errors are detected), the EXTENDED DIAGNOSTICS menu will be displayed with accompanying error messages. Perform the following parts only if the instrument fails the Self Calibration; otherwise, Self Calibration has been completed.

e. Press the MENU OFF/EXTENDED FUNCTIONS button to turn off the EXTENDED DIAGNOSTICS menu.

f. Repeat parts b through d. If the instrument displays the EXTENDED DIAGNOSTICS menu again, refer the instrument to qualified personnel for servicing; otherwise, Self Calibration has been successfully completed.

EXTERNAL CALIBRATION

Equipment Required (See Table 4-1):

Calibration Generator (Item 2)

NOTE

J156 must be removed (see step 1, part a of Internal Adjustments) and a Self Calibration executed before this subsection can be performed. After performance (or partial performance) of this subsection, the cabinet should be removed and J156 reinstalled. Installation of this jumper will prevent inadvertent loss of the Calibration constants established by performance of this procedure. See the introduction of this procedure for further detail.

1. Attenuator Adjustments.

a. Press the MENU OFF/EXTENDED FUNCTIONS button once or twice (two presses are necessary if any menu is presently displayed, one press if no menu is displayed) to display the Extended Functions menu.

b. Press the menu button labeled CAL/DIAG (menu will change).

c. Press the menu button labeled EXT CAL to display the EXT CAL menu.

d. Connect the STD OUTPUT of a Calibration Generator to the CH 1 and CH 2 input connectors through a 50 Ω cable and a dual input coupler.

e. Set the Calibration Generator for a DC output (see the generator Operators manual).

f. Press the menu button labeled ATTEN ("CONNECT CH1 AND CH2 TO 0.2V" will be displayed) and set the generator output to 0.200 volts.

g. Press the ATTEN BUTTON again ("RUNNING" will be displayed near the lower right corner of the screen).

h. When the display changes from "CONNECT ... TO 0.2V" to "CONNECT ... TO 2.0V" change the generator output to 2.000 volts and press the ATTEN button.

i. When the display changes from "CONNECT ... TO 2.0V" to "CONNECT ... TO 20.V" change the generator output to 20.00 volts and press the ATTEN button.

NOTE

After successful completion of the Attenuator Calibration sequence, "RUNNING" will disappear from the crt screen and "PASS" will be displayed above the ATTEN menu button label. If the calibration routine is NOT successful, "FAIL" will be displayed above the ATTEN button label. Perform the following parts only if the instrument fails the Attenuator Calibration sequence; otherwise, Attenuator Calibration is complete.

j. Recheck the test setup and ensure that the Calibration Generator is set for a DC output. Reperform the Self Calibration subsection of this procedure.

k. Repeat parts d through i. If the instrument fails the Attenuator Calibration sequence again, refer the instrument to qualified personnel for servicing; otherwise, Attenuator Calibration has been successfully completed.

l. Disconnect the test setup.

2. Trigger Adjustments.

a. Press the MENU OFF/EXTENDED FUNCTIONS button once or twice (two presses are necessary if any menu is presently displayed, one press if no menu is displayed) to display the Extended Functions menu.

b. Press the menu button labeled CAL/DIAG (menu will change).

c. Press the menu button labeled EXT CAL to display the EXT CAL menu.

d. Connect the STD OUTPUT of a Calibration Generator to the EXT TRIG 1 and EXT TRIG 2 input connectors through a 50 Ω cable and a dual input coupler.

e. Set the Calibration Generator for a DC output (see the generator Operators manual).

f. Press the menu button labeled TRIGGER ("CONNECT TRIGS TO GND" will be displayed) and set the generator output to 0.2 mV (~GND).

g. Press the TRIGGER button again ("RUNNING" will be displayed near the lower right corner of the screen).

h. When the display changes from "CONNECT ... TO GND" to "CONNECT ... TO 0.5V" change the generator output to 0.5 V and press the TRIGGER button.

i. When the display changes from "CONNECT ... TO 0.5V" to "CONNECT ... TO 2.0V" change the generator output to 2 V and press the TRIGGER button.

NOTE

After successful completion of the Trigger Calibration sequence, "RUNNING" will disappear from the crt screen and "PASS" will be displayed above the TRIGGER menu button label. If the calibration routine is NOT successful, "FAIL" will be displayed above the TRIGGER button label. Perform the following parts only if the instrument fails the Trigger Calibration sequence; otherwise, Trigger Calibration is complete.

j. Recheck the test setup and ensure that the Calibration Generator is set for a DC output. Reperform the Self Calibration subsection of this procedure.

k. Repeat parts d through i. If the instrument fails the Trigger Calibration sequence again, refer the instrument to qualified personnel for servicing; otherwise, Trigger Calibration has been successfully completed.

l. Disconnect the test setup.

3. Ramp (REPET) Calibration.

a. Press the MENU OFF/EXTENDED FUNCTIONS button once or twice (two presses are necessary if any menu is presently displayed, one press if no menu is displayed) to display the Extended Functions menu.

b. Press the menu button labeled CAL/DIAG (menu will change).

c. Press the menu button labeled EXT CAL to display the EXT CAL menu.

d. Press the menu button labeled REPET. The EXT CAL menu will display "RUNNING" momentarily and then display "PASS" or "FAIL." The calibration for REPET is then complete.

MAINTENANCE

This section contains useful information on the calibration of the 2430 and for conducting preventive maintenance, troubleshooting, and corrective maintenance on the 2430 Oscilloscope. Circuit board removal procedures are included in the "Corrective Maintenance" subsection. An extensive diagnostic procedures table (Table 6-6) is provided in the "Diagnostics" subsection at the back of this section.

CALIBRATION IN THE 2430 DIGITAL OSCILLOSCOPE

The 2430 Digital Oscilloscope is designed to provide as near total automatic calibration as practical. Automatic procedures minimize manufacturing and end-user costs associated with calibration and enhance the accuracy of the instrument during use.

Instead of the usual numerous manual potentiometer "tweeks" that require extensive servicing, the 2430 makes wide use of digital calibration techniques. The extensive digital-to-analog (DAC) subsystem of the scope and the built-in computer firmware are used to calculate and adjust more than 100 voltages that control gain, offset, and other parameters of circuit operation affecting accuracy. The automatic SELF CAL uses no external test equipment and takes less than 10 seconds to complete. The ease of use of SELF CAL allows it to be done at any time to assure the user of an accurate measurement in the present testing environment.

Adjustments that remain for the display system and CCD output amplifiers and those requiring external standard test signals are not automatic, but they are aided by the built-in programming. The 2430 supplies the test signals for the display system and CCD output amplifier adjustments and does the actual calibration of the vertical attenuators and trigger amplifiers once the standard voltage calibration signals are provided.

Calibration Levels

Calibration of the 2430 occurs at several levels. These levels are the fully automatic SELF CAL, the semiautomatic EXTENDED CAL, the manual adjustments, and dynamic calibration.

Self Calibration

Almost all of the measurement systems within the 2430 are calibrated with the SELF CAL procedure. These automatic adjustments include the gain and offset settings for the vertical acquisition system and the internal trigger system. No adjustments are required for the time base or horizontal subsystems.

Maximum instrument accuracy can be assured by doing a SELF CAL just before making critical measurements. Continued accuracy is maintained by running SELF CAL whenever the operating temperature has changed more than five degrees Celsius since the last SELF CAL.

Extended Calibration

Semiautomatic calibration of the vertical attenuators (ATTEN) and external trigger amplifiers (TRIGGER) is supported by this level of calibration. The technician must supply the dc voltage levels required for calibration to the input connectors, and the scope then performs the actual calibration of the gain of the vertical input attenuators and gain and offset of the external trigger amplifier using the supplied dc voltages. During the ATTEN calibration, the accuracy of the internal 10 V Calibration Reference is verified against the standard amplitude voltage applied to the attenuators.

The EXT CAL routines also provide the automatic REPET calibration and the display signals for the manual ADJUSTS needed for the Display System and CCD output amplifier calibrations. REPET calibration adjusts the timing of the jitter correction ramps. The jitter correction ramps are used measure the time between the randomly acquired samples and the trigger point. That time difference is used to place the waveform samples correctly with respect to the trigger point in the repetitive acquisition mode waveform record.

Manual Adjustments

Adjustments made by the technician involving access to the internal portions of the scope are limited to the Display System, the crt adjustments, the CCD output amplifier gains, the attenuator input capacitance, the 50 MHz bandwidth limiter (and 20 MHz bandwidth limiter with the Video Option), and the charge-coupled device (CCD) sampling clock skew. These adjustments are made during factory calibration of the 2430 and should not require readjustment during normal operation. Replacement of parts during repair of the instrument that affect these calibrations will, however, require readjustment of the affected circuitry. The ADJUSTS (DISPLAY in version 1.7 firmware) calibration routine in the EXTENDED CALIBRATION procedures provides display patterns and brief instructions for the technician to follow in calibrating the Display System and CCD output amplifier gains.

Dynamic Adjustments

As the 2430 operates, continuous adjustments are made to correct for minor offsets in the acquisition system and jitter correction ramp timing. The dynamic adjustments are totally automatic and require no user action.

Recommended Adjustment Intervals

The recommended interval for doing the Extended Calibration ATTEN and external TRIGGER calibrations is every 2000 hours, or once a year if the instrument is used infrequently. Readjustment of the Display System and rerunning the REPET calibration step will not normally be needed unless parts are replaced that affect those calibrations. It is NOT necessary to reperform any portion of the Extended Calibration to maintain maximum measurement accuracy over the specified operating temperature range of the instrument.

NATIONAL BUREAU OF STANDARDS TRACEABILITY

Traceability to the National Bureau of Standards (NBS) requires that the stated accuracy of an instrument has been established through calibration with equipment whose accuracies have been established either directly or indirectly by NBS certified references.

For the 2430, traceability is established in the Extended Calibration routine by calibrating the attenuators (ATTEN) and external trigger amplifiers (TRIGGER) with an NBS traceable voltage reference. As the fine gain adjustment of the attenuators is made, the relative accuracy of the internal 10 V Calibration Reference is also checked by normalizing it to the external voltage source provided by the technician. If the fine gain of the attenuators requires an adjustment of more than approximately 2%, the ATTEN calibration fails. Barring 2430 component problems, a failure indicates either that the internal reference is faulty or that the applied voltage is not a valid standard reference voltage.

Passing the ATTEN calibration step using an NBS traceable voltage standard ensures that the internal, nonadjustable 10 V Calibration Reference is also traceable. Subsequently passing the SELF CAL procedure (which uses the traceable 10 V Calibration Reference to provide the calibration voltages) then makes the 2430 an NBS traceable instrument. Traceability is maintained for subsequent performances of SELF CAL by referencing all calibration calculations to the traceable internal voltage reference of the 2430.

VOIDING CALIBRATION

Factory calibration of the 2430 is done using NBS traceable sources. An internal jumper installed at the time of calibration prevents the user from inadvertently running the EXT CAL routines and voiding the traceable calibration of the instrument. Removing the jumper and attempting to do the ATTEN and TRIGGER calibration without an accurate standard amplitude voltage source will result in a failed calibration. In the case of a failure, the stored constants for the attenuator gain calibration are not replaced; therefore, the previous degree of accuracy is maintained by the instrument. However, a FAIL label remains displayed over the affected EXT CAL menu choice, and the scope will fail subsequent power-on tests and enter Extended Diagnostics (EXT DIAG) until the calibration is passed.

Power-on or Self Diagnostics (SELF DIAG) tests that detect a system, subsystem, or device failure that may affect instrument calibration are noted by a FAIL label on the test along with the calibration status of UNCALD in the EXT DIAG menu display. Calibration failures are of two types: soft errors caused by gain or offset parameter drifts beyond tolerance—usually caused by a large change in operating temperature since the last SELF CAL was done, or hard failures caused by component problems in the 2430 circuitry that prevent calibration.

Soft Errors

These errors appear as a loss of SELF CAL and are noted by the UNCALD label appearing above the SELF CAL choice in the main CAL/DIAG menu. Running the SELF CAL routine and obtaining a PASS status clears up any soft calibration errors and revalidates the instrument calibration.

Hard Failures

A hard failure affecting calibration may also be indicated by the loss of SELF CAL, but running the SELF CAL routine does not produce a PASS status for SELF CAL or any failed test in EXT DIAG. Loss of ATTEN or external TRIGGER calibration is noted by the UNCALD label appearing above those choices in the EXT CAL menu. A loss of calibration for either ATTEN or TRIGGER indicates a possible nonvolatile memory failure. In either case, instrument calibration should be considered void, and the 2430 must be referred to a qualified service person for servicing.

STATIC-SENSITIVE COMPONENTS

The following precautions apply when performing any maintenance involving internal access to the instrument.

CAUTION

Static discharge can damage any semiconductor component in this instrument.

This instrument contains electrical components that are susceptible to damage from static discharge. Table 6-1 lists the relative susceptibility of various classes of semiconductors. Static voltages of 1 kV to 30 kV are common in unprotected environments.

When performing maintenance, observe the following precautions to avoid component damage:

1. Minimize handling of static-sensitive components.

2. Transport and store static-sensitive components or assemblies in their original containers or on a metal rail. Label any package that contains static-sensitive components or assemblies.

3. Discharge the static voltage from your body by wearing a grounded antistatic wrist strap while handling these components. Servicing static-sensitive components or assemblies should be performed only at a static-free work station by qualified service personnel.

4. Nothing capable of generating or holding a static charge should be allowed on the work station surface.

5. Keep the component leads shorted together whenever possible.

6. Pick up components by their bodies, never by their leads.

Table 6-1

Relative Susceptibility to Static-Discharge Damage

Semiconductor Classes	Relative Susceptibility Levels[a]
MOS or CMOS microcircuits or discretes, or linear microcircuits with MOS inputs (Most Sensitive)	1
ECL	2
Schottky signal diodes	3
Schottky TTL	4
High-frequency bipolar transistors	5
JFET	6
Linear microcircuits	7
Low-power Schottky TTL	8
TTL (Least Sensitive)	9

[a]Voltage equivalent for levels (voltage discharged from a 100 pF capacitor through a resistance of 100 ohms):

1 = 100 to 500 V	**4 = 500 V**	**7 = 400 to 1000 V (est)**
2 = 200 to 500 V	**5 = 400 to 600 V**	**8 = 900 V**
3 = 250 V	**6 = 600 to 800 V**	**9 = 1200 V**

7. Do not slide the components over any surface.

8. Avoid handling components in areas that have a floor or work-surface covering capable of generating a static charge.

9. Use a soldering iron that is connected to earth ground.

10. Use only approved antistatic, vacuum-type desoldering tools for component removal.

PREVENTIVE MAINTENANCE

INTRODUCTION

Preventive maintenance consists of cleaning, visual inspection, and checking instrument performance. When performed regularly, it may prevent instrument malfunction and enhance instrument reliability. The severity of the environment in which the instrument is used determines the required frequency of maintenance. An appropriate time to perform preventive maintenance is just before instrument adjustment.

GENERAL CARE

The cabinet minimizes accumulation of dust inside the instrument and should normally be in place when operating the oscilloscope. The instrument's front cover protects the front panel and crt from dust and damage. It should be installed whenever the instrument is stored or transported.

INSPECTION AND CLEANING

The 2430 should be visually inspected and cleaned as often as operating conditions require. Accumulation of dirt in the instrument can cause overheating and component breakdown. Dirt on components acts as an insulating blanket, preventing efficient heat dissipation. It also provides an electrical conduction path that could result in instrument failure, especially under high-humidity conditions.

CAUTION

Avoid the use of chemical cleaning agents which might damage the plastics used in this instrument. Use a nonresidue-type cleaner, preferably isopropyl alcohol or a solution of 1% mild detergent with 99% water. Before using any other type of cleaner, consult your Tektronix Service Center or representative.

Exterior

INSPECTION. Inspect the external portions of the instrument for damage, wear, and missing parts; use Table 6-2 as a guide. Instruments that appear to have been dropped or otherwise abused should be checked thoroughly to verify correct operation and performance. Repair deficiencies that could cause personal injury or lead to further damage to the instrument immediately.

CAUTION

To prevent getting moisture inside the instrument during external cleaning, use only enough liquid to dampen the cloth or applicator.

CLEANING. Loose dust on the outside of the instrument can be removed with a soft cloth or small soft-bristle brush. The brush is particularly useful for dislodging dirt on and around the controls and connectors. Dirt that remains can be removed with a soft cloth dampened in a mild detergent-and-water solution. Do not use abrasive cleaners.

Two plastic light filters, one blue and one clear, are provided with the oscilloscope. Clean the light filters and the crt face with a soft lint-free cloth dampened with either isopropyl alcohol or a mild detergent-and-water solution.

Interior

To access the inside of the instrument for inspection and cleaning, refer to the "Removal and Replacement Procedure" in the "Corrective Maintenance" part of this section.

INSPECTION. Inspect the internal portions of the 2430 for damage and wear, using Table 6-3 as a guide. Deficiencies found should be repaired immediately. The corrective procedure for most visible defects is obvious; however, particular care must be taken if heat-damaged components are found. Overheating usually indicates other trouble in the instrument; it is important, therefore, that the cause of overheating be corrected to prevent recurrence of the damage.

If any electrical component is replaced, conduct a Performance Check for the affected circuit and for other closely related circuits (see Section 4). If repair or replacement work is done on any of the power supplies, verify that the affected power supply meets the voltage and ripple tolerance requirements under Specification in Section 1 of this manual.

CAUTION

To prevent damage from electrical arcing, ensure that circuit boards and components are dry before applying power to the instrument.

CLEANING. To clean the interior, blow off dust with dry, low-pressure air (approximately 9 psi). Remove any remaining dust with a soft brush or a cloth dampened with a solution of mild detergent and water. A cotton-tipped applicator is useful for cleaning in narrow spaces and on circuit boards. If these methods do not remove all the dust or dirt, the instrument may be spray washed using a solution of 5% mild detergent and 95% water as follows:

CAUTION

Exceptions to the following cleaning procedure are the CH 1 and CH 2 Attenuator assemblies. Clean these assemblies only with isopropyl alcohol as described in Step 4 of the cleaning procedure. In addition, all other Front Panel controls are sealed and require no maintenance.

1. Gain access to the parts to be cleaned by removing easily accessible shields and panels (see "Removal and Replacement Procedure").

2. Spray wash dirty parts with the detergent-and-water solution; then use clean water to thoroughly rinse them.

3. Dry all parts with low-pressure air.

4. Clean switches with isopropyl alcohol and wait 60 seconds for the majority of the alcohol to evaporate. Then complete drying with low-pressure air.

5. Dry all components and assemblies in an oven or drying compartment using low-temperature (125°F to 150°F) circulating air.

Table 6-2

External Inspection Check List

Item	Inspect For	Repair Action
Cabinet, Front Panel, and Cover	Cracks, scratches, deformations, damaged hardware or gaskets.	Touch up paint scratches and replace defective components.
Front-panel Controls	Missing, damaged, or loose knobs, buttons, and controls.	Repair or replace missing or defective items.
Connectors	Broken shells, cracked insulation, and deformed contacts. Dirt in connectors.	Replace defective parts. Clear or wash out dirt.
Carrying Handle	Correct operation.	Replace defective parts.
Accessories	Missing items or parts of items, bent pins, broken or frayed cables, and damaged connectors.	Replace damaged or missing items, frayed cables, and defective parts.

Table 6-3

Internal Inspection Check List

Item	Inspect For	Repair Action
Circuit Boards	Loose, broken, or corroded solder connections. Burned circuit boards. Burned, broken, or cracked circuit-run plating.	Clean solder corrosion with an eraser and flush with isopropyl alcohol. Resolder defective connections. Determine cause of burned items and repair. Repair defective circuit runs.
Resistors	Burned, cracked, broken, blistered.	Replace defective resistors. Check for cause of burned component and repair as necessary.
Solder Connections	Cold solder or rosin joints.	Resolder joint and clean with isopropyl alcohol.
Capacitors	Damaged or leaking cases. Corroded solder on leads or terminals.	Replace defective capacitors. Clean solder connections and flush with isopropyl alcohol.
Semiconductors	Loosely inserted in sockets. Distorted pins.	Firmly seat loose semiconductors. Remove devices having distorted pins. Carefully straighten pins (as required to fit the socket), using long-nose pliers, and reinsert firmly. Ensure that straightening action does not crack pins, causing them to break off.
Wiring and Cables	Loose plugs or connectors. Burned, broken, or frayed wiring.	Firmly seat connectors. Repair or replace defective wires or cables.
Chassis	Dents, deformations, and damaged hardware.	Straighten, repair, or replace defective hardware.

LUBRICATION

There is no periodic lubrication required for this instrument.

SEMICONDUCTOR CHECKS

Periodic checks of the transistors and other semiconductors in the oscilloscope are not recommended. The best check of semiconductor performance is actual operation in the instrument.

PERIODIC READJUSTMENT

To ensure accurate measurements, check the performance of this instrument every 2000 hours of operation, or if used infrequently, once each year. In addition, replacement of components may necessitate readjustment of the affected circuits.

Complete Performance Check and Adjustment procedures are given in Sections 4 and 5. The Performance Check Procedure can also be helpful in localizing certain troubles in the instrument. In some cases, minor problems may be revealed or corrected by readjustment.

TROUBLESHOOTING

INTRODUCTION

Preventive maintenance performed on a regular basis should reveal most potential problems before an instrument malfunctions. However, should troubleshooting be required, the following information is provided to facilitate location of a fault. In addition, the material presented in the "Theory of Operation" and "Diagrams" sections of this manual may be helpful while troubleshooting.

TROUBLESHOOTING AIDS

Diagnostic Firmware

The operating firmware in this instrument contains diagnostic routines that aid in locating malfunctions. When instrument power is applied, power-up tests are performed to verify proper operation of the instrument. If a failure is detected, this information is passed on to the operator in the form of a crt readout error message. The failure information directs the troubleshooter to the area of failing circuitry. If the failure is such that the processor can still execute the diagnostic routines, the user can call up specific tests to further check the failing circuitry. The specific diagnostic routines are explained later in this section.

Schematic Diagrams

Complete schematic diagrams are located on tabbed foldout pages in the "Diagrams" section. Heavy black lines that enclose portions of the circuitry represent the circuit board on which the enclosed circuitry is mounted. The assembly number and name of the circuit board are shown near either the top or the bottom edge of the diagram.

Functional blocks on schematic diagrams are outlined with a wide grey line. Components within the outlined area perform the function designated by the block label. The "Detailed Block Diagram Description" in the "Theory of Operation" uses these functional block names when describing circuit operation, aiding in cross-referencing between the two circuit descriptions and the schematic diagrams.

Component numbers and electrical values of components in this instrument are shown on the schematic diagrams. Refer to the first page of the "Diagrams" section for the reference designators and symbols used to identify components. Important voltages and waveform reference numbers (enclosed in hexagonally-shaped boxes) are also shown on each diagram. Waveform illustrations are located adjacent to their respective schematic diagram.

Circuit Board Illustrations

Circuit board illustrations showing the physical location of each component are provided for use in conjunction with each schematic diagram. Each board illustration is found in the "Diagrams" section on the back of a foldout page, preceding the first schematic diagram(s) to which it relates.

The locations of waveform test points are marked on the circuit board illustrations with hexagonally outlined numbers corresponding to the waveform numbers on both the schematic diagram and the waveform illustrations.

Circuit Board Locations

The placement of each circuit board in the instrument is shown in a board locator illustration. This illustration is located on the foldout page along with the circuit board illustration.

Circuit Board Interconnections

A circuit board interconnection diagram is provided in the "Diagrams" section to aid in tracing a signal path or power source between boards. All wire, plug, and jack numbers are shown along with their associated wire or pin numbers.

Power Distribution

Power distribution is traceable through the schematic diagrams in the "Diagrams" section. The low-voltage power supplies originate on the Power Supply board and are schematically illustrated in diagrams 22 and 23. The high-voltage and +61 V power supplies, originating on the High Voltage board, are shown in diagram 19. Any power supply can be tracked back to its diagram and forward to other circuitry illustrated on different diagrams.

Power is distributed to the different circuit boards through interconnect assemblies consisting of one or more connectors. The diagrams showing these assemblies (or partial assemblies) provide the interconnecting assembly (wire, plug, and/or jack) numbers, as well as the number for the individual pins or wires distributing the supplies. By referencing the numbers for the assembly and its connector wire(s), the diagram showing that section of the power distribution path immediately preceding the section illustrated (on a given diagram) can be determined.

If power is carried to another interconnect assembly and on to another circuit board, that distribution is shown. The other interconnect assembly and conductors are labeled as previous described, except the an individual connector number indicates the diagram showing the succeeding distribution path section rather than the preceding section. This method allows the tracing of power distribution either up the path towards the originating supply, or away (further down the distribution path) from that supply.

In some cases, the diagram showing an interconnect assembly carrying power to a circuit board may not illustrate all of that circuit board. Arrows pointing to diagram numbers indicate other schematic diagrams (illustrating other parts of the circuit board) where the supplies are routed. Further, any diagram showing a partial circuit board will indicate the number of the diagram where the interconnect assembly(ies) routing power supplies to that board is illustrated. This method allows tracing power distribution back to an interconnect assembly, at which point further distribution tracing can occur.

As a further aid to power supply distribution, the "Diagrams" section contains an interconnect diagram. This diagram shows all of the interconnections between the various circuit board assemblies, including the power supplies. This diagram can also be an aid in power distribution tracing.

Grid Coordinate System

Each schematic diagram and circuit board illustration has a grid border along its left and top edges. A table located adjacent to each diagram lists the grid coordinates of each component shown on that diagram. To aid in physically locating components on the circuit board, this table also lists the grid coordinates of each component on the circuit board illustration.

Near each circuit board illustration is an alphanumeric listing of all components mounted on that board. The second column in each listing identifies the schematic diagram in which each component can be found. These component-locator tables are especially useful when more than one schematic diagram is associated with a particular circuit board.

Troubleshooting Charts

The troubleshooting charts contained in the "Diagrams" section are to be used in conjunction with the Extended Diagnostics of Table 6-6 (at the back of this section) as an aid in locating malfunctioning circuitry. To use the charts, begin with the Initial Troubleshooting Guide shown in Figure 6-6. This guide will help identify problem areas and will direct you to the appropriate procedures for further troubleshooting.

Component Color Coding

Information regarding color codes and markings of resistors and capacitors is located on the color-coding illustration (Figure 9-1) at the beginning of the "Diagrams" section.

Semiconductor Lead Configurations

Figure 9-2 in the "Diagrams" section shows the lead configurations for most types of semiconductor devices used in the instrument. Vendor changes and performance improvement changes may result in changes of case styles or lead configurations. If the device in question does not appear to match a configuration shown in Figure 9-2, examine the associated circuitry or consult a manufacturer's data sheet to obtain the pin nomenclature.

Multipin Connectors

Multipin connector orientation is indexed by two triangles; one on the holder and one on the circuit board. Slot numbers are usually molded into the holder. When a connection is made to circuit board pins, ensure that the index on the holder is aligned with the index on the circuit board (see Figure 6-1).

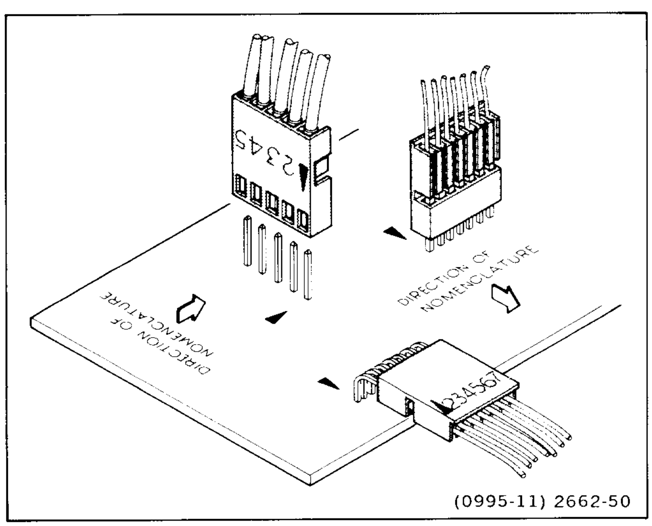


Figure 6-1. Multipin connector.

TROUBLESHOOTING EQUIPMENT

The equipment listed in Table 4-1 of this manual, or equivalent equipment, may be useful when troubleshooting this instrument.

TROUBLESHOOTING TECHNIQUES

In the following list of troubleshooting procedures, the first two steps use diagnostic aids inherent in the instrument's operating firmware. These built-in tests can locate many circuit faults to aid in isolating the problem circuitry. The next four procedures are check steps that ensure proper control settings, connections, operation, and adjustment. If the trouble is not located by these checks, the remaining steps will aid in locating the defective component. When the defective component is located, replace it using the appropriate replacement procedure given under "Corrective Maintenance" in this section.

CAUTION

Before using any test equipment to make measurements on static-sensitive, current-sensitive, or voltage-sensitive components or assemblies, ensure that any voltage or current supplied by the test equipment does not exceed the limits of the component to be tested.

1. Power-up Tests

The 2430 performs automatic verification of the instrument. If a failure occurs, refer to the "Calibration and Diagnostics" discussion later in this section for interpreting the failure.

If a problem is found, the associated troubleshooting procedure may be used to isolate the problem. The troubleshooting procedures are found in Table 6-6 (located in the "Diagnostics" subsection). See Figure 6-6 (also in the Diagnostics subsection) for the Initial Troubleshooting Guide.

2. Diagnostic Test Routines.

The instrument firmware contains diagnostic routines that may be selected by the user from the front panel to further clarify the nature of a suspected failure. The desired test is selected using the MENU buttons after entering the Extended Diagnostics Mode. Entry into the Diagnostic Mode and its uses are explained in the "Calibration and Diagnostics" discussion later in this section.

3. Check Control Settings

Incorrect control settings can give a false indication of instrument malfunction. If there is any question about the correct function or operation of any control, refer to either the "Operating Information" in Section 2 of this manual or to the 2430 Operators Manual.

4. Check Associated Equipment

Before proceeding, ensure that any equipment used with the 2430 is operating correctly. Verify that input signals are properly connected and that the interconnecting cables are not defective. Check that the ac-power-source voltage to all equipment is correct.

5. Visual Check

WARNING

To avoid electrical shock, disconnect the instrument from the ac power source before making a visual inspection of the internal circuitry.

Perform a visual inspection. This check may reveal broken connections or wires, damaged components, semiconductors not firmly mounted, damaged circuit boards, or other clues to the cause of an instrument malfunction.

6. Check Instrument Performance and Adjustment

Check the performance of those areas where trouble appears to exist. The trouble condition observed may be the result of a lack of calibration. Complete Performance Check and Adjustment procedures are given in Sections 4 and 5 of this manual respectively.

7. Isolate Trouble to a Circuit

To isolate problems to a particular area, use any symptoms noticed to help locate the trouble. Refer to the Extended Diagnostics table (Table 6-6) in the "Calibration and Diagnostics" discussion in this section as an aid in locating a faulty circuit.

8. Check Power Supplies

WARNING

For safety reasons, an isolation transformer must be connected whenever troubleshooting in the Preregulator and Inverter Power Supply sections of the instrument.

When trouble symptoms appear in more than one circuit, first check the power supplies; then check the affected circuits by taking voltage and waveform readings. Check first for the correct output voltage of each individual supply; then measure ac ripple to check that it is within the Total Peak-to-Peak Ripple specification. Table 6-4 lists the power supply voltage level and ripple limits for each supply.

These voltages are measured between the power supply test points (most of which are located on the Side Board near the Front Panel μP) and ground. Voltage ripple amplitudes must be measured using an oscilloscope. Before measuring ac ripple, set the STORAGE ACQUIRE mode of the 2430 to SAVE. Use a 1X probe having as short a ground lead as possible to minimize stray pickup.

NOTE

The oscilloscope used to measure ripple must be bandwidth limited to 20 MHz. Use of a higher bandwidth oscilloscope without 20 MHz bandwidth limiting will result in higher readings.

Table 6-4

Power Supply Voltage and Ripple Limits[a]

Power Supply	Reading (Volts)	P-P Ripple (mV)
+61 V	59.05 to 62.95	100
+15 V	14.74 to 15.26	10
+10 V Ref	9.97 to 10.03	10
+8 V	7.85 to 8.15	10
+5 V	4.91 to 5.09	10
+5 VD (digital)	4.83 to 5.17	150
−5 V	−4.95 to −5.05	10
−8 V	−7.85 to −8.15	10
−15 V	−14.74 to −15.26	10
−15 V unreg		350
−1900 V	−1855 to −1945	

[a]At 25 °C.

If the power-supply voltages and ripple are within the listed ranges in Table 6-4, the supply can be assumed to be working correctly. If the supply is not within specified ranges, the fault may or may not be located in the power supply circuitry. A defective component elsewhere in the instrument can create the appearance of a power-supply problem and may also affect the operation of other circuits. Use the power supply troubleshooting charts to aid in locating the problem.

9. Check Circuit Board Interconnections

After the trouble has been isolated to a particular circuit, again check for loose or broken connections, improperly seated semiconductors, and heat-damaged components.

10. Check Voltages and Waveforms

Often the defective component can be located by checking circuit voltages or waveforms. Typical voltages are listed on the schematic diagrams. Waveforms indicated on the schematic diagrams by hexagonally outlined numbers are shown adjacent to the diagrams. Waveform test points are shown on the circuit board illustrations.

NOTE

Voltages and waveforms indicated on the schematic diagrams are not absolute and may vary slightly between instruments. To establish operating conditions similar to those used to obtain these readings, set up the Test scope and the 2430 under test as indicated near the waveform illustrations for a schematic diagram.

11. Check Individual Components

WARNING

To avoid electric shock, always disconnect the instrument from the ac power source before removing or replacing components.

CAUTION

When checking semiconductors, observe the static-sensitivity precautions located at the beginning of this section.

To accurately check components, it is often necessary to remove or partially disconnect the component from the circuit board, in order to isolate it from surrounding circuitry. Partial specifications (resistor tolerance, transistor type, etc.) for most components can be found by referencing the component designation number in the "Replaceable Electrical Parts." Also see Figure 9-1 for component value identification and Figure 9-2 for semiconductor lead configurations.

12. Repair and Adjust the Circuit

If any defective parts are located, follow the replacement procedures given under "Corrective Maintenance" in this section. After any electrical component has been replaced, the performance of that circuit and any other closely related circuit should be checked. If work has been done on the power supplies, a complete check of the regulated voltages should be done to verify that the supply voltages are in tolerance. A check of the Display ADJUSTS calibration and a SELF CAL should verify that the instrument meets Performance Requirements if the voltages are all correct.

CORRECTIVE MAINTENANCE

INTRODUCTION

Corrective maintenance consists of component replacement and instrument repair. This part of the manual describes special techniques and procedures required to replace components in this instrument. If it is necessary to ship your instrument to a Tektronix Service Center for repair or service, refer to the "Repackaging for Shipment" information in Section 2 of this manual.

MAINTENANCE PRECAUTIONS

To reduce the possibility of personal injury or instrument damage, observe the following precautions:

1. Disconnect the instrument from the ac-power source before removing or installing components.

2. Verify that the line-rectifier filter capacitors are discharged prior to performing any servicing.

3. Use care not to interconnect instrument grounds which may be at different potentials (cross grounding).

4. When soldering on circuit boards or small insulated wires, use only a 15-watt, pencil-type soldering iron.

5. Use an isolation transformer to supply power to the 2430 if removing the shield and troubleshooting in the power supply.

OBTAINING REPLACEMENT PARTS

Most electrical and mechanical parts can be obtained through your local Tektronix Field Office or representative. However, many of the standard electronic components can usually be obtained from a local commercial source. Before purchasing or ordering a part from a source other than Tektronix, Inc., please check the "Replaceable Electrical Parts" list for the proper value, rating, tolerance, and description.

NOTE

Physical size and shape of a component may affect instrument performance, particularly at high frequencies. Always use direct-replacement components, unless it is known that a substitute will not degrade instrument performance.

Special Parts

In addition to the standard electronic components, many special parts are used in the 2430. These components are manufactured or selected by Tektronix, Inc. to meet specific performance requirements, or are manufactured for Tektronix, Inc. in accordance with our specifications. The various manufacturers can be identified by referring to the "Cross Index—MFR Code Number to Manufacturer" at the beginning of the "Replaceable Electrical Parts" list. Most of the mechanical parts used in this instrument were manufactured by Tektronix, Inc. Order all special parts directly from your local Tektronix Field Office or representative.

Ordering Parts

When ordering replacement parts from Tektronix, Inc., be sure to include all of the following information:

1. Instrument type (include modification or option numbers).

2. Instrument serial number.

3. A description of the part (if electrical, include its full circuit component number).

4. Tektronix part number.

SELECTABLE COMPONENTS

Several components in the 2430 are selectable to obtain optimum circuit operation. Value selection of these components is done during the initial factory adjustment procedure. Further selection is not usually necessary for subsequent adjustments unless a component has been changed that affects circuitry for which a selected component has been specifically chosen.

Specifically, selected components are A10R767, A10R867, A10R679, A10R878, A10R1015, and A10R1016. All the components are located on the Main board. Resistors A10R1015 and A10R1016 are shown on schematic diagram 9, while the remaining resistors are on schematic diagram 14.

It may be necessary to select A10R1015 if the CH 1 Preamp (U420), Peak Detector (U440), and/or CCD/Clock Driver (U450) is changed. Selection of A10R1016 may be necessary if the same components associated with CH 2 (U100, U340, and U350, respectively) are changed. Upon changing any of those components, the vertical performance checks associated with the affected channel should be made. If the bandwidth and rise time performance requirements are met and the front-corner aberrations are within approximately ±6% and 6% peak-to-peak, the resistor associated with the affected channel should not be changed. If these conditions are not met, selecting the resistor changes circuit response as follows:

1. Increasing the resistance reduces the front-corner aberrations while decreasing bandwidth and rise time.

2. Decreasing the resistance increases bandwidth and rise time while increasing front-corner aberrations.

3. The change in front-corner aberrations for changing the resistor is less than or equal to 1%.

Do not increase the value of the resistor to the point where the bandwidth and rise-time performance requirements are not met; the ±6%, 6% peak-to-peak guideline is maintenance information only, not a performance requirement. The bandwidth, rise time, and aberrations should be measured with the affected channel set to 200 mV per division.

Selection of A10R767 and A10R867 may be necessary if the CH 1 CCD (U450) is changed; selection of R679 and R878 may be necessary if CH 2 CCD (U350) is changed. These resistor pairs affect the gain of their associated CCD. To determine if resistors require selecting, perform "Check LF Linearity," Step 4 of the Performance Check procedure in this manual. If the instrument passed this check, no resistor change is necessary.

If the instrument is outside the tolerance limits for the linearity check, the resistors should be changed to the next higher value in the following list. Change only that resistor pair for the out-of-limit channel, unless both channels fail the linearity check. Always replace both resistors in the pair with the same value resistor.

After replacement of the resistor pair(s), repeat the linearity check. If the instrument still fails that check, change the resistor pair of the affected channel(s) to the next higher value in the list. Repeat the check, changing the resistor pair(s) to the next higher range until the affected channel(s) pass the linearity check. This method for resistor pair selection insures the lowest value allowing the instrument to pass the LF linearity test is used. Using the lowest possible value for the resistor pair prevents other performance characteristic from being compromised.

Selectable resistors for A11R767/A11R867 and A11R679/A11R878 resistor pairs are:

Value	Tektronix Part No.
2.0 kΩ	321-0222-00
2.26 kΩ	321-0277-00
2.61 kΩ	321-0233-00
2.74 kΩ	321-0235-00
2.8 kΩ	321-0236-00

MAINTENANCE AIDS

The maintenance aids listed in Table 6-5 include items required for performing most of the maintenance procedures in this instrument. Equivalent products may be substituted for the examples given, provided their characteristics are similar.

Table 6-5

Maintenance Aids

Description	Specification	Usage	Example
1. Soldering Iron	15 to 25 W.	General soldering and unsoldering.	Antex Precision Model C.
2. Torx Screwdrivers	Torx tips #T7, #T9, #T10, #T15, and #T20.	Assembly and disassembly.	Tektronix Part Numbers: 003-1293-00 003-0965-00 003-0814-00 003-0966-00 003-0866-00.
3. Nutdrivers	1/4 inch, 7/32 inch, 5/16 inch, 1/2 inch, and 9/16 inch.	Assembly and disassembly.	Xcelite #7, #8, #10, #16, and #18.
4. Open-end Wrench	9/16 inch and 1/2 inch.	Channel Input and Ext Trig BNC Connectors.	Tektronix Part Numbers: 9/16 in. 003-0502-00 1/2 in. 003-0822-00.
5. Hex Wrenches	0.050 inch, 1/16 inch.	Assembly and disassembly.	Allen Wrenches.
6. Long-nose Pliers		Component removal and replacement.	Diamalloy Model LN55-3.
7. Diagonal Cutters		Component removal and replacement.	Diamalloy Model M554-3.
8. Vacuum Solder Extractor	No static charge retention.	Unsoldering static sensitive devices and components on multilayer boards.	Pace Model PC-10.
9. Contact Cleaner and lubricant	No-Noise R.	Switch and pot cleaning and lubrication.	Tektronix Part Number: 006-0442-02.
10. Pin-Replacement Kit		Replace circuit board connector pins.	Tektronix Part Number: 040-0542-00.
11. IC-Removal Tool		Removing DIP IC packages.	Augat T114-1.
12. Isopropyl Alcohol	Reagent grade.	Cleaning attenuator and front-panel assemblies.	2-Isopropanol.
13. Isolation Transformer[a]		Isolate the instrument from the ac power source for safety.	Tektronix Part Number 006-5953-009.
14. 1X Probe		Power supply ripple check.	TEKTRONIX P6101 Probe (1X) Part Number 010-6101-03.

[a]The isolation transformer (item 13) is an important SAFETY item. The switching power supply of the 2430 has areas that float at the ac-source potential, and a serious shock hazard exists when the power supply safety shield is removed to permit trouble-shooting if power is applied directly from the ac-source.

INTERCONNECTIONS

Interconnections in this instrument are made with pins soldered onto the circuit boards. Several types of mating connectors are used for the interconnecting pins. The following information provides the replacement procedures for the various types of connectors.

End-Lead Pin Connectors

Pin connectors used to connect the wires to the interconnect pins are factory assembled. They consist of machine-inserted pin connectors mounted in plastic holders. If the connectors are faulty, the entire wire assembly should be replaced.

Multipin Connectors

When pin connectors are grouped together and mounted in a plastic holder, they are removed, reinstalled, or replaced as a unit. If any individual wire or connector in the assembly is faulty, the entire cable assembly should be replaced. To provide correct orientation of a multipin connector, an index arrow is stamped on the circuit board, and either a matching arrow is molded into or the numeral 1 is marked on the plastic housing as a matching index. Be sure these index marks are aligned with each other when the multipin connector is reinstalled.

TRANSISTORS AND INTEGRATED CIRCUITS

Transistors and integrated circuits should not be replaced unless they are actually defective. If removed from their sockets or unsoldered from the circuit board during routine maintenance, return them to their original board locations. Unnecessary replacement or transposing of semiconductor devices may affect the adjustment of the instrument. When a semiconductor is replaced, check the performance of any circuit that may be affected.

Any replacement component should be of the original type or a direct replacement. Bend transistor leads to fit their circuit board holes, and cut the leads to the same length as the original component. See Figure 9-2 in the "Diagrams" section for lead-configuration illustrations.

CAUTION

After replacing a power transistor, check that the collector is not shorted to the chassis before applying power to the instrument.

The chassis-mounted power supply transistor is insulated from the chassis by a heat-transferring mounting block. Reinstall the mounting block and bushings when replacing these transistors. Use a thin layer of heat-transferring compound between the insulating block and chassis when reinstalling the block.

To remove socketed dual-in-line packaged (DIP) integrated circuits, pull slowly and evenly on both ends of the device. Avoid disengaging one end of the integrated circuit from the socket before the other, since this may damage the pins.

To remove a soldered DIP IC when it is going to be replaced, clip all the leads of the device and remove the leads from the circuit board one at a time. If the device must be removed intact for possible reinstallation, do not heat adjacent conductors consecutively. Apply heat to pins at alternate sides and ends of the IC as solder is removed. Allow a moment for the circuit board to cool before proceeding to the next pin.

SOLDERING TECHNIQUES

The reliability and accuracy of this instrument can be maintained only if proper soldering techniques are used to remove or replace parts. General soldering techniques, which apply to maintenance of any precision electronic equipment, should be used when working on this instrument.

WARNING

To avoid an electric-shock hazard, observe the following precautions before attempting any soldering: turn the instrument off, disconnect it from the ac power source, and wait at least three minutes for the line-rectifier filter capacitors to discharge.

Use rosin-core wire solder containing 63% tin and 37% lead. Contact your local Tektronix Field Office or representative to obtain the names of approved solder types.

When soldering on circuit boards or small insulated wires, use only a 15-watt, pencil-type soldering iron. A higher wattage soldering iron may cause etched circuit conductors to separate from the board base material and melt the insulation on small wires. Always keep the soldering-iron tip properly tinned to ensure best heat transfer from the iron tip to the solder joint. Apply only enough solder to make a firm joint. After soldering, clean the area around the solder connection with an approved flux-removing solvent (such as isopropyl alcohol) and allow it to air dry.

CAUTION

Only an experienced maintenance person, proficient in the use of vacuum-type desoldering equipment should attempt repair of any circuit board in this instrument. Many integrated circuits are static sensitive and may be damaged by solder extractors that generate static charges. Perform work involving static-sensitive devices only at a static-free work station while wearing a grounded antistatic wrist strap. Use only an antistatic vacuum-type solder extractor approved by a Tektronix Service Center.

CAUTION

Attempts to unsolder, remove, and resolder leads from the component side of a circuit board may cause damage to the reverse side of the circuit board.

The following techniques should be used to replace a component on a circuit board:

1. Touch the vacuum desoldering tool to the lead at the solder connection. Never place the iron directly on the board; doing so may damage the board.

NOTE

Some components are difficult to remove from the circuit board due to a bend placed in the component leads during machine insertion. To make removal of machine-inserted components easier, straighten the component leads on the reverse side of the circuit board.

2. When removing a multipin component, especially an IC, do not heat adjacent pins consecutively. Apply heat to the pins at alternate sides and ends of the IC as solder is removed. Allow a moment for the circuit board to cool before proceeding to the next pin.

CAUTION

Excessive heat can cause the etched circuit conductors to separate from the circuit board. Never allow the solder extractor tip to remain at one place on the board for more than three seconds. Solder wick, spring-actuated or squeeze-bulb solder suckers, and heat blocks (for desoldering multipin components) must not be used. Damage caused by poor soldering techniques can void the instrument warranty.

3. Bend the leads of the replacement component to fit the holes in the circuit board. If the component is replaced while the board is installed in the instrument, cut the leads so they protrude only a small amount through the reverse side of the circuit board. Excess lead length may cause shorting to other conductive parts.

4. Insert the leads into the holes of the board so that the replacement component is positioned the same as the original component. Most components should be firmly seated against the circuit board.

5. Touch the soldering iron to the connection and apply enough solder to make a firm solder joint. Do not move the component while the solder hardens.

6. Cut off any excess lead protruding through the circuit board (if not clipped to the correct length in Step 3).

7. Clean the area around the solder connection with an approved flux-removing solvent. Be careful not to remove any of the printed information from the circuit board.

REMOVAL AND REPLACEMENT PROCEDURE

Read these instructions completely before attempting any corrective maintenance.

WARNING

To avoid electric shock, disconnect the instrument from the ac power source before removing or replacing any component or assembly.

The exploded view drawing in the "Replaceable Mechanical Parts" list at the rear of this manual may be helpful during the removal and installation of individual components or subassemblies. Figure 6-2 illustrates the locations of the circuit boards referred to in this procedure. Individual circuit boards are illustrated in the "Diagrams" section of this manual; those illustrations are useful in location of the components referred to in this procedure.

As a further aid in component location, this procedure specifies the location of most of the components to be disconnected. The component side of a circuit board is referred to as the "top" side of the board; the edge nearest the Front Panel is the front edge. The remaining sides and edges follow from this orientation.

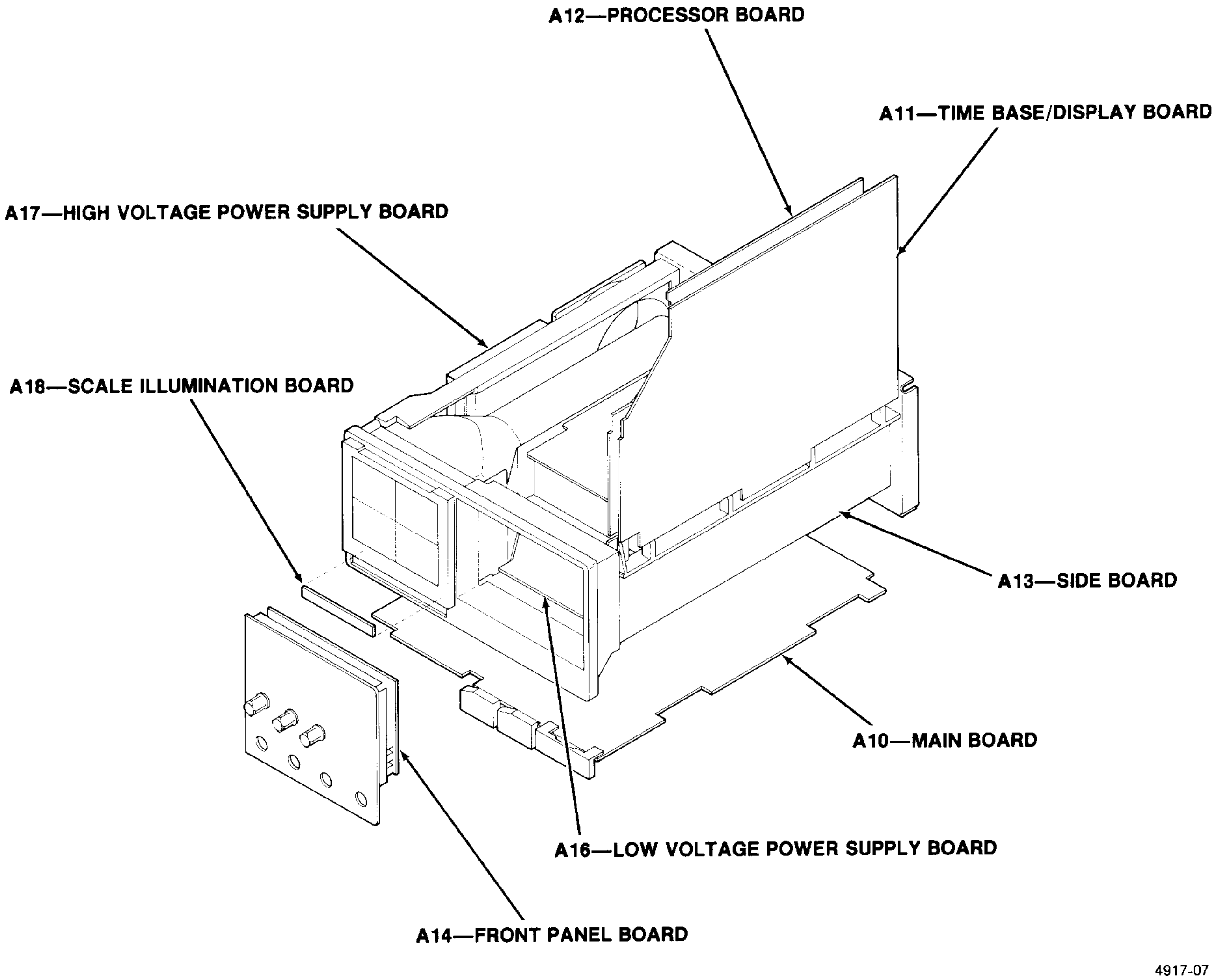


Figure 6-2. 2430 circuit boards.

1. Cabinet Removal

a. Disconnect the power cord from any ac power source.

b. Disconnect the power cord from its receptacle at the instrument's Rear panel.

c. Grasp the power cord plug (female end), rotate the power cord retainer 1/4 turn, and pull it to remove the cord from the Rear panel.

d. Grasp the handle hubs (at right and left side of the instrument) and pull outward. Rotate the hubs to position the front of the handle away from the front of the instrument.

e. Install the protective Front cover over the Front panel. Push on the cover to lock the cover's side tabs around the Front panel's trim band.

f. Set the instrument so it rests on the Front cover.

g. Remove the four screws inside the four rear feet at the instrument's back panel.

WARNING

Dangerous potentials exist at several points throughout this instrument. If it is operated with the cabinet removed, do not touch exposed connections or components. Some transistors may have elevated case voltages. Disconnect the ac power source from the instrument and verify that the line-rectifier filter capacitors have discharged before cleaning the instrument or replacing parts (see label on the Low Voltage Power Supply cover).

h. Grasp the handle hubs (at right and left sides of the instrument) and pull outward. While holding the hubs outward, pull straight up from the rear of the cabinet to remove the cabinet from the instrument.

Reverse parts a through h to install the cabinet.

WARNING

The line-rectifier capacitors normally retain a charge for several minutes after the instrument is powered off and can remain charged for a longer period if a bleeder resistor or other power supply problem occurs. Before beginning any cleaning or work on the internal circuitry of the instrument, discharge the capacitors by connecting a shorting strap in series with a 1 kΩ, 5 watt resistor across the capacitors. Connect one end of the shorting strap/resistor combination to upper-most terminal of S1020 (the terminal connected through a wire to W310). Connect the other end to pin 11 of T117 (the pin protruding from the side of the transformer, near its right-rear corner). Measure across those two connections with a voltmeter to ensure the capacitors are discharged.

2. Timebase/Display Board Removal

a. Perform Step 1 to remove the cabinet.

b. Set the instrument on a flat, smooth surface, with its underside facing down and the Front panel facing forward.

c. Disconnect the ribbon-cable connector from J100 of the Timebase/Display board. J100 is located at the right-front corner of the Timebase/Display board.

d. Disconnect the ribbon cable connector at J141 of the Main board. J141 is located at the lower right-rear corner of the instrument.

e. Disconnect the ribbon cable connector at J121 of the Timebase/Display board. J121 is located at the right-rear corner of the board, under the ribbon cable disconnected in part d.

f. Disconnect P117 and P148 from J117 and J148. J117 and J148 are located on the Timebase/Display board, at the right-rear corner and center-rear edge, respectively.

g. Remove the three mounting screws securing the Timebase/Display board to the Center chassis and Power Supply.

h. Using a 7/32 inch nutdriver, rotate the two black plastic retaining latches counterclockwise 1/4 turn to unlock them. The two retaining latches are located near the left-front and left-rear corners of the Timebase/Display board.

i. Grasp the left edge of the Timebase/Display board and rotate it (and the Top chassis) upward about 45 degrees. While supporting the Top chassis, disconnect the ribbon cable connector at J131 (left-front corner of the Timebase/Display board) and the flex cable at J125 (right-rear corner of the Processor board on the underside of the Top chassis).

j. Continue to rotate the Top chassis until it is at a 90 degree angle to the top of the instrument.

k. Rotate the black retaining latch (center-left edge of the Timebase/Display board) 1/4 turn counterclockwise to release the board from the Top chassis.

l. Grasp the left edge of the board and pull it slightly away from the Top chassis until it clears the head of the retaining latch unlocked in part k. Pull up on the board until the right edge of the board slips out of the four channel notches on the Top chassis.

Reverse parts a through l to install the board to the Top chassis and to secure the Top chassis to the Center chassis. Take care to fit the right edge of the board to the four channel notches when installing the board on the Top chassis.

3. Processor Board Removal

a. Perform Step 1 to remove the cabinet.

b. Set the instrument on a flat, smooth surface, with its underside facing down and the Front panel facing forward.

c. Remove the three mounting screws securing the Timebase/Display board to the Center chassis and Power Supply.

d. Using a 7/32 inch nutdriver, rotate the two black retaining latches counterclockwise 1/4 turn to unlock them. The two retaining latches are located near the left-front and left-rear corners of the Timebase/Display board.

e. Grasp the left edge of the Timebase/Display board and rotate it (and the Top chassis) upward about 45 degrees. While supporting the Top chassis, disconnect the ribbon cable connector at J131 (left-front corner of the Timebase/Display board) and the flex cable at J125 (right rear corner of the Processor board on the underside of the Top chassis).

f. Continue to rotate the Top chassis until it is at a 180 degree angle to the top of the instrument. The top of the Processor board is now exposed.

g. Disconnect the ribbon-cable connector from J103 and the flex cable connector from J207 of the Processor board. J103 and J207 are located at the left-front corner of the board.

h. Disconnect the ribbon cable connector at J123 of the Processor board (instruments with Option 05 installed only). J123 is located at the rear quarter section of the board near the center.

i. Disconnect the ribbon cable connectors at J181 and J120 of the Processor board. J181 and J120 are located at the left rear corner of the board.

j. Rotate the black retaining latch (center-right edge of the Processor board) 1/4 turn counterclockwise to release the board from the Top chassis.

k. Grasp the right edge of the board and pull it slightly away from the Top chassis until it clears the head of the retaining latch unlocked in part j. Pull up on the board until the left edge of the board slips out of the four channel notches on the Top chassis.

Reverse parts a through k to install the board on the Top chassis and to secure the Top chassis to the Center chassis. Take care to fit the edge of the board to the four channel notches when installing it on the Top chassis.

4. Front Panel Board Removal

a. Perform Step 1 to remove the cabinet from the instrument.

b. Set the instrument on a flat, smooth surface, with its underside facing down and the Front panel facing forward.

c. Pull straight out on the INTENSITY control knob to remove it from its shaft.

d. Using a small, flat-bladed screwdriver, gently pry loose and remove the top trim cover.

e. Remove the four screws exposed by part d.

f. Turn the instrument over to expose the bottom of the trim ring and remove the two screws securing the front feet to the instrument. Remove the feet from the trim ring.

g. Remove the two remaining screws securing the trim ring.

h. Grasp the edges of the trim ring and pull forward to remove it from the Front casting.

i. Turn the instrument over so its top side is up.

j. Remove the three mounting screws securing the Timebase/Display board to the Center chassis.

k. Using a 7/32 inch nutdriver, rotate the two black retaining latches counterclockwise 1/4 turn to unlock them. The two retaining latches are located near the left-front and left-rear corners of the Timebase/Display board.

l. Grasp the left edge of the Timebase/Display board and rotate it (and the Top chassis) upward about 45 degrees. While supporting the Top chassis, disconnect the flex cable at J125 (right-rear corner of the Processor board on the underside of the Top chassis).

m. Continue to rotate the Top chassis until it is at a 180 degree angle to the top of the instrument.

n. Disconnect the ribbon cable connector from J166 on the Low Voltage Power Supply board and push it towards the rear of the instrument. J166 is located at the left-front section of the board near the front corner of the Center chassis.

o. Disconnect the ribbon cable connector from J150 at the front of the Side board.

p. Remove the anode lead from its retainer and dress it away from the lower square hole in the Main chassis. Take care not to separate the male end of that lead from the female end.

q. Disconnect the ribbon cable connector from J152 of the Main board. J152 is located in front of the High Voltage shield, at the lower left side of the instrument.

r. Carefully route the connectors disconnected in parts o and q to the inside of the instrument.

s. Gently push the backside of the Front Panel Control assembly until it is removed from the Front casting.

t. To remove the Front Panel Control board from the Front panel, perform the following subparts:

(1) Using a 1/16 inch allen wrench, remove the CH 1 and CH 2 VOLTS/DIV control knobs, as well as the A and B SEC/DIV control knob.

(2) Pull straight out on the remaining five control knobs to remove them from their shafts.

(3) Turn the Front panel face down and remove the four mounting screws from the Front Panel Control board. Separate the Front panel from the board.

Reverse parts a through t to assemble the Front panel assembly and install it on the instrument. Take care to align the GPIB Status indicators to their holes in the trim ring when installing that band.

5. Main Board Removal

a. Perform Step 1 to remove the cabinet from the instrument.

b. Perform parts a through h of Step 4 to remove the Front Panel trim ring.

c. Pull the Front Panel assembly forward until it is clear of the Front casting and the face of the Front casting is accessible (it is not necessary to disconnect the cables connecting the assembly to the main instrument).

d. Remove the six screws securing the Main board to the Front casting. The screws are located on the face of the casting and are adjacent to the four BNC connectors.

e. Disconnect the two flex cable connectors at J104 and J108, and the ribbon cable connector at J105. J104, J105, and J108 are located near the right-front corner of the board.

f. Disconnect the three ribbon cable connectors from J111, J113 (TV Trigger option only), and J141 at the left edge of the board.

g. Disconnect the cable connector from J107, located near the right-rear corner of the board, and from J106, located near center-front edge of the board.

h. Remove the screw securing the end of the Power switch's extension shaft to the Front casting.

i. Grasp the large extension shaft near where it joins to the small shaft of the power switch and pull it upwards from the Main board to disconnect it. Lift up and back (towards the rear of the instrument) to remove the extension shaft from the Front casting.

NOTE

When installing the extension shaft to the Power switch, push the small shaft to put the switch in the IN position. Insert the shaft into the Front casting, align the extension shaft to the small shaft, and push the button end of the switch until the two shafts are coupled.

j. Using a 7/32 inch nutdriver, rotate the seven black retaining latches 1/4 turn counterclockwise to release them.

k. Disconnect the flex cable connector from J114 and the two retaining latches. J114 is located in left-rear corner of the board.

l. Remove the two mounting screws securing the Main board to Main chassis.

m. Lift the board up from the instrument and back from the Front casting to complete the board removal.

Reverse parts a through p to install the Main board.

6. Side Board Removal

a. Perform Step 1 to remove the cabinet from the instrument.

b. Set the instrument on a flat, smooth surface with the Side board facing up and the Front panel facing forward.

c. Disconnect the ribbon cable connectors from J111 and J141 of the Main board.

d. Disconnect the ribbon cable connectors from J100 of the Timebase/Display board and J103 of the Processor board. The two connectors are attached to the same ribbon cable.

e. Disconnect the ribbon cable connectors from J121 of the Timebase/Display board and J120 of the Processor board. The two connectors are attached to the same ribbon cable.

f. Disconnect the ribbon cable connector from J150 of the Side board.

g. Perform parts j through l of Step 4 to access the inside of the instrument.

h. Disconnect the ribbon cable connector from J102 at the right front corner of the Low Voltage Power Supply board and route the cable to the outside of the instrument.

i. Rotate the Top chassis back to the normal (installed) position. Using a 7/32 inch nutdriver, rotate the two retaining latches 1/4 turn clockwise to temporarily secure it to the instrument.

j. Rotate the black retaining latch (near the front of the Side board) 1/4 turn counterclockwise to unlock it.

k. Remove the mounting screw (center of the Side board) securing the Side board to the Main chassis.

l. Lift the front of the Side board up until it clears the retaining latch and then pull the board forward, until it clears the channel notch at its rear edge, to complete the removal.

Reverse parts a through l to install the Side board in the instrument. Take care to fit the rear edge of the board to the channel notch when reinstalling to the chassis.

7. High Voltage Power Supply Board Removal

a. Perform Step 1 to remove the cabinet from the instrument.

b. Set the instrument on a flat, smooth surface with the High Voltage Supply board facing up and the Front panel facing forward.

WARNING

The CRT anode lead may retain a high-voltage charge after the instrument is powered off. To avoid electrical shock, ground the CRT anode lead to the metal chassis after disconnecting the plug. Reconnect and disconnect the anode-lead plug several times, grounding the anode lead to chassis ground each time it is disconnected to fully dissipate the charge.

c. Remove the anode lead from the retaining hook that secures it to the Main chassis.

d. Disconnect the CRT lead (male end) from the High Voltage Module lead.

e. Remove the single screw securing the High Voltage Power Supply and lift the High Voltage shield off.

WARNING

The five mounting posts on the side of the High Voltage module (U565) may retain a high-voltage charge after the instrument is powered off. To avoid electrical shock, discharge these posts to the metal chassis through an appropriate shorting strap.

f. Discharge the five posts on the side of the High Voltage module to the metal chassis.

g. Disconnect the cable connectors from J172 and J173, located at the front edge of the board, and from J162 and J176, located the rear edge of the board.

h. Disconnect the remaining ribbon connector from J105 on the Main board.

i. Pry outward on either one of two retaining latches securing the fan on its mounting posts. As the latch clears the edge of the fan, pull the fan outward and away from the instrument to remove. The latches are located at opposite corners; one at the bottom corner nearest the rear, the other at the top corner nearest the front, of the instrument.

j. Perform parts j through l of Step 4 to access the inside of the instrument.

k. Disconnect the crt connector from the back of the crt.

l. Rotate the two black retaining latches (near the front- and rear-left corners of the High Voltage Power Supply board) 1/4 turn counterclockwise to unlock them.

m. While holding its nut (located between the crt shield and the adjacent Main chassis) stationary, remove the mounting post (near the center of the board) securing the High Voltage Power Supply board to the Main chassis.

n. Lift the left edge of the board up to clear the retaining latches. Pull the board to the left, until its right edge clears the two channel notches, to complete the removal.

Reverse parts a through n to install the High Voltage Power Supply board. Take care to fit the left edge of the board to the channel notches when reinstalling the board.

8. Low Voltage Power Supply Assembly Removal

a. Perform Step 1 to remove the cabinet from the instrument.

b. Remove the mounting screw at the center of the Side board. Note that for instruments with Option 05 installed, it is necessary to disconnect the ribbon cable connector at J113 of the Main board to access the mounting screw.

c. Disconnect the ribbon cable connector at J148 of the Timebase/Display board.

d. Perform parts j through l of Step 4 to access the inside of the instrument.

e. Disconnect the ribbon cable connectors at J102 (right front corner of the Low Voltage Power Supply Supply board) and J166 (left front corner of the same board).

f. Disconnect the flex cable connector from J207 at the left front corner of the Processor board.

g. Remove the six screws and two extension posts securing the Low Voltage Power Supply cover (hereafter referred to as "the cover") to the Low Voltage Power Supply bracket.

h. Remove the screw securing the cover to the Center chassis.

i. Remove the two screws securing the cover to the Rear chassis. One screw is located immediately below the GPIB Connector, the other immediately below the PLOTTER X OUTPUT BNC.

j. Lift the cover off the Low Voltage Power Supply bracket to remove.

k. Disconnect the four cable connectors from P30, P60, P70, and P80 (located near the rear of the Low Voltage Power Supply board). Note the color coding of the cables to guide in reconnection of same.

l. Using a 7/32 inch nutdriver, rotate the two black retaining latches (near the left and right front corners of the Low Voltage Power Supply board) 1/4 turn counterclockwise to unlock them. Repeat for the two latches located near the middle of the right and left edges of the board.

m. Remove the mounting screw securing the Low Voltage Power Supply assembly to the Main chassis. The screw is located near the right-front corner of the board.

n. Carefully route the disconnected cables away from the top side of the Low Voltage Power Supply assembly.

o. Grasp the front of the Low Voltage Power Supply bracket and lift up until the Low Voltage Power Supply board is clear of the retaining latches unlocked in part m.

p. Pull the board towards the front of the instrument (until its rear edge clears the two channel notches) while lifting upwards to complete the removal of the assembly.

Reverse parts a through p to assemble the Low Voltage Power Supply assembly and secure it to the instrument. Take care to fit the board to the channel notches when reinstalling the board.

9. Cathode Ray Tube Removal

WARNING

Use care when handling a crt. Breakage of the crt may cause high-velocity scattering of glass fragments (implosion). Protective clothing and safety glasses (preferably a full-face shield) should be worn. Avoid striking the crt on any object which may cause it to crack or implode. When storing a crt, place it in a protective carton of set it face down on a smooth surface in a protected location. When stored face down, it should be placed on a soft, nonabrasive surface to prevent the crt face plate from being scratched.

a. Perform Step 1 to remove the cabinet from the instrument.

b. Perform parts c through i of Step 4 to remove the trim band from the instrument.

c. Remove the implosion shield from the crt faceplate.

WARNING

The crt anode lead may retain a high-voltage charge after the instrument is powered off. To avoid electrical shock, ground the crt anode lead to the metal chassis after disconnecting the plug. Reconnect and disconnect the anode-load plug several times, grounding the anode lead to chassis ground each time it is disconnected to fully dissipate the charge.

d. Remove the anode lead from the retaining hook that secures it to the Main chassis.

e. Disconnect the crt anode lead (male end) from the high-voltage module lead. Discharge the crt anode lead by grounding its tip to the metal chassis.

f. Disconnect the cable from J172 at the right-front corner of the High Voltage Power Supply board.

g. Perform parts j through l of Step 4 to access the inside of the instrument.

h. Disconnect the crt connector from the back of the crt.

i. Disconnect the single cable from the crt (accessed through a hole in the top of the crt shield).

j. Disconnect the ribbon cable at J148 of the Timebase/Display board.

k. Disconnect the flex cable at J104 of the Main board.

l. Remove the eight screws (two at each corner) securing the crt frame to the Front casting.

m. Remove the crt frame from the Front casting. Guide the flex cable disconnected in part k through its slot in the Front casting while removing the crt frame.

n. Grasp the face of the crt and pull it forward, while guiding the crt anode lead and the other cable (disconnected in part f) through their holes in the crt shield. It may be necessary to reposition the ribbon cable (disconnected in part j) as the removal of the crt is completed.

Reverse parts a through n to install the crt. When installing the crt frame (removed in part m) to the casting, refer to Figure 6-3 for the method of installation.

10. Menu Switch Removal

a. Perform Step 1 to remove the cabinet from the instrument.

b. Disconnect the flex cable at J104 of the Main board.

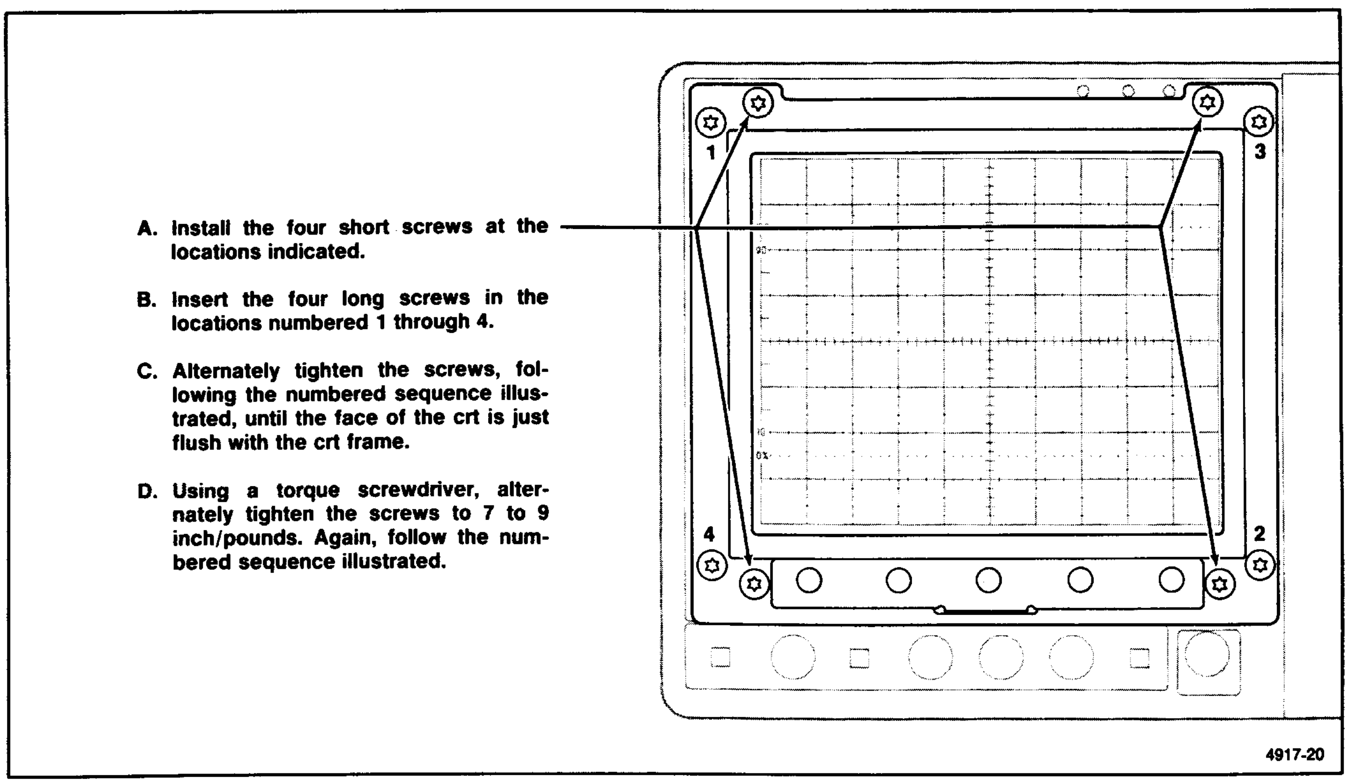


Figure 6-3. Installation sequence for installing the crt frame screws.

c. Perform parts c through i of Step 4 to remove the trim band from the instrument.

d. Perform parts k through m of Step 9 to remove the crt frame from the instrument.

e. Carefully pull the adhesive-backed switch from the front of the crt frame.

f. Pull the switch through the hole in the crt frame to complete the removal.

Reverse parts a through e to install the Menu switch to the crt frame and the frame to the instrument. Use care to align the switch to the locating studs on the crt frame when pressing the switch back on the frame.

11. Scale Illumination Board Removal

a. Perform parts a through e of Step 10.

b. Disconnect the Scale Illumination board cable from J106 (located near the front edge of the Main board).

c. Remove the Scale Illumination board and the attached light reflector while guiding the cable (disconnected in part b) through its hole in the Front casting.

d. Separate the Scale Illumination board from the light reflector to complete the disassembly.

Reverse parts a through d to install the Scale Illumination board to the instrument.

12. Attenuator Removal Procedure

a. Perform Step 1 to remove the cabinet from the instrument.

b. Perform parts b through s of Step 4 to access the inside of the instrument. Skip parts n, p, and q. When performing part r of Step 4, route the cable disconnected in part o.

c. Insert the tip of a short screwdriver through the large slot in the front casting (above and right of the associated input BNC connector). Remove the screw securing the front of the Attenuator to the Main board.

d. Insert the tip of a screwdriver through the hole in the Low Voltage Power Supply board that is directly above the Attenuator to be removed. Remove the screw securing the rear of the Attenuator to the Main Board.

e. Rotate the Timebase/Display board to its mounting position and temporarily secure it by rotating the two black retaining lugs 1/2 turn clockwise to lock them. The two retaining latches are located near the left-front and left-rear corners of the Timebase/Display board.

f. Remove the two screws securing the rear Attenuator shield to the heatsink. Remove the small shield.

g. Unsolder the two Attenuator output leads from the variable-capacitor lead and the resistor-capacitor pair lead exposed in part f.

h. Unplug the multipin connector from the Main board (at P147 for the CH 1 and P146 for the CH 2 Attenuator).

i. Remove the two screws (one is immediately lower left and the other upper right of the associated input BNC connector) securing the Attenuators to the front casting.

j. Remove the two screws securing the small bar to the bottom of the front casting.

k. Grasp the front end of the Attenuator assembly by its BNC connector and the rear end by the rear edge of the Attenuator shield.

l. Gently lift the Attenuator straight up from the Main board until the Attenuator pins clear their Main board plugs underneath the Attenuator assembly. Lift the rear of the Attenuator assembly up and towards the rear of the instrument until the Attenuator clears the braided shield cable mounted in the front casting.

Reverse parts b through l to reinstall the Attenuator. When performing part b, reverse parts b through s of Step 4 to reinstall the front panel and secure the Timebase/Display board and Front Panel assembly to the instrument.

DIAGNOSTICS

CALIBRATION AND DIAGNOSTICS

The SELF DIAG and EXT DIAG routines are layered into three levels for detecting and isolating system operation faults. Fault detection is based on starting at the lowest system level, the kernel, and then testing each additional subsystem with the knowledge that previously tested subsystems were good. When a subsystem fault is detected by one of the diagnostics, it is isolated at that subsystem level. Additional testing then proceeds downward through the remaining tests of that subsystem to the lowest testable level.

The instrument system supports two levels of Internal Calibration routines: SELF CAL and EXT CAL. These routines calibrate the analog subsystems of the 2430 to meet specified performance requirements. Any detected faults in the control system and/or in the self-calibrating hardware are reported by a "FAIL" message displayed with the label of the failed area.

Self Cal and Self Diagnostics Tests

The tests done and calibration performed are subsets of the total EXTENDED DIAGNOSTICS tests.

SELF CAL. Self Calibration generates test voltages to the Peak Detectors via the Cal Amplifier and DAC system. These voltage are used to set the gains, offsets and/or centering, and balance of the CCD Samplers, Peak Detectors, and Preamplifiers. Calibration constants required to obtain calibration are stored in NVRAM (nonvolatile RAM) where they are retained to maintain calibration. There is some interaction between each of the adjustments made. The effects of interaction are minimized by using the previously stored constants as a starting point for all recalculations of the SELF CAL constants. If starting with a "COLD START", the previous calibration constants are discarded; therefore, the SELF CAL tests are done twice to assure a converged solution. (The time required to perform the SELF CAL procedure from a COLD START is therefore obviously longer than the normal SELF CAL.)

Self Calibration may be started from the front panel using the EXTENDED FUNCTIONS menu or by the GPIB routines for automatically calibrating the analog systems within the 2430. Self Calibration routines calibrate the major portion of the analog system of the 2430 in about 10 seconds. A Self Calibration may be performed by the user at any time. Important times are after the instrument has warmed up, if the ambient operating temperature changes by a significant amount since the last Self Calibration, and just prior to making a measurement that requires the highest possible level of accuracy.

SELF DIAG. These are menu-driven tests, automatically executed at power-on. The Self Diagnostics test the functionality of all components that may be controlled or accessed by the 2430 System μP. The Self Diagnostics routines may also be accessed from the instrument front panel or by mean of the GPIB interface. If all tests pass—from an initial power-on, a call from the front-panel, or from the GPIB interface—the system invokes the SCOPE MODE.

Self Diagnostics involves a number of routines to perform the diagnostic tests with the result of each level of tests used as a basis for making the tests that follow. These routines are, in general, as follows:

1. System μP call to Self Diagnostics routine.

2. System ROM is checked to validate memory operation (1000 level tests).

3. Read/Write and Addressing tests are performed on registers (2000 level tests).

4. System RAM is checked for write-read capability to all addresses (3000 level tests).

5. Front panel and waveform processors are checked (4000 and 5000 level tests respectively).

6. Checksums of NVRAMS (both long-term and short-term RAM) are done to validate the stored calibration constants and waveform data (6000 level tests).

7. Calibrated analog circuits are tested to see if they will pass with the present calibration constants (7000-9000 level tests).

To test the analog systems, Self Diagnostics widens the limits of the resolution used for Self Calibration and performs all the SELF CAL tests to determine if they can be passed. If a Self Diagnostic test fails in the 7000 to 9300 level tests, it is not possible to assume a hardware failure unless SELF CAL is performed and a failure occurs in the same test or tests. Failure may only indicate that calibration is inaccurate for the current ambient temperature. The reason for this is that SELF CAL stores the new computed values of the constants used to obtain instrument calibration in the present instrument condition and then uses the new constants for subsequent calibration tests. However, SELF DIAG uses the previously stored calibration constants (without changing them to meet present ambient temperature conditions). If the ambient temperature has changed sufficiently to affect calibration, the tests run may not be able to converge to the correct limits (even though they are wider than those of SELF CAL). This indicates that a SELF CAL should be done to move the calibration constant values to the new "in-calibration" limits to compensate for the present instrument conditions, whereupon the SELF DIAG test should pass.

Extended Cal and Extended Diagnostics

NOTE

EXT CAL and the SPECIAL menu choices are normally disabled to the user. The cabinet must be removed and Jumper J156 must be removed (diagram 13) to enable the menus. Disabling is done to prevent the user from accidently voiding the calibration.

EXT CAL. Extended Calibration is an interactive procedure that requires the calibrator to apply standard voltages to the Vertical and External trigger inputs as part of the procedure. Extended Cal uses the test voltages to automatically set the correct Attenuator Gain through the Preamplifiers and the Trigger circuitry offset and gain. The internal 10 V Calibration Reference is verified against the applied dc test voltage standard as part of the Attenuator calibration.

NOTE

Attempting an EXT CAL for ATTEN and TRIG calibration without having the correct dc voltage levels available will cause the "FAIL" message to appear above the menu label of the failed areas. However, in the event of a failed attempt, the previous calibration constants will not be overwritten, and the instrument will remain in its previous state of calibration. Also to warn the user that a calibration attempt has failed, the message "UNCALD" will appear in the EXT DIAG menu, and the instrument will enter the Extended Diagnostics Mode (displaying the EXT DIAG menu) at each subsequent power-on.

The FAIL message will also be displayed as the result of an actual hardware failure. Instruments displaying a FAIL message should be referred to a qualified service person for any necessary servicing if a correct calibration attempt does not pass.

The display ADJUSTS routines generate test waveforms or voltage levels that are used by the calibrator to set the vertical and horizontal gain and offset for the crt drive signal and the CCD output amplifier gains. These display adjustments also include edge focus, geometry, crt bias, and other adjustments to optimize the crt display. (No two crts are exactly alike, therefore these tests must be user interactive.)

Other manual adjustments requiring calibration are the 50 MHz bandwidth limit (plus the 20 MHz bandwidth limit with the Video Option installed) and the CCD clock sample skew.

Extended Calibration via the GPIB is much more than those menu choices accessed in the EXT CAL menu. Each test available in Extended Diagnostics is accessible for running as a calibration step, in groups or one at a time.

EXT DIAG. Extended Diagnostics is the complete set of tests and procedures that are available. All other choices of the CAL/DIAG menu and the power-on self test are sub-sets. The Extended Diagnostics menus permit selection of individual tests to isolate an error to the lowest level possible. The test can be made to loop, for using external test and measurement equipment to isolate signal path problems, once the area of failure has been determined by the automatic tests.

Any of the Self Diagnostics tests may be accessed either individually or in selected groups using the EXT DIAG control menu. The tests use internal feedback and the digitizing capabilities of the instrument to minimize the need for applying external signals or using external test equipment to troubleshoot. Testing of a failed area down to the lowest functional level possible (in some cases to the failed component) provides direction for further troubleshooting with service routines and/or conventional methods. Troubleshooting a failure of the 2430 may be based on assumptions made possible by running selected tests to verify good circuit blocks, thereby eliminating those blocks from consideration as a failed area.

SERVICE ROUTINES. The Service Routines are menu, GPIB interface, or jumper initiated routines for exercising the hardware, usually in a looping mode, that allow a service person to troubleshoot a fault in the 2430 using external testing and measuring equipment. Where possible, the

Extended Diagnostics routines are used for looping to permit access to them from both the front-panel EXTENDED FUNCTIONS menu and the GPIB interface.

Jumper-initiated tests include Kernel Mode for the System μP and the Waveform μP, Waveform μP Bus Control Mode, Bus Isolate Mode, System μP Chip Select test, Resets for the System μP and the Waveform μP, a Front Panel μP internal diagnostics test, and a Front Panel Multiplexer test. A description of these tests and how they are used is included in Table 6-6, Extended Diagnostics.

Troubleshooting routines (written by a system programmer) that systematically exercise specific firmware or hardware functions may be implemented via the GPIB interface. This type of external testing aids in troubleshooting the scope by providing a troubleshooting tool that may be changed as needed by controller programming.

Use of these routines provides service personnel with signals and procedures that enable fault isolation and restoration of an instrument to a functional level that is supported by the Extended Diagnostics and/or other Service Routines.

Special Diagnostics Features

The menu choices under SPECIAL are normally disabled to the user, and if the SPECIAL button is pressed, the message "DISABLED—SEE MANUAL" is displayed. If the functions are enabled for servicing by removing J156 (located on the A13 board and shown in diagram 13), pressing the SPECIAL choice of EXTENDED FUNCTIONS calls up the display "WARNING: SERVICE ONLY—SEE MANUAL" with the choices of COLD START, CAL PATH ON/OFF (in Version 2.0 firmware), and FORCE DAC. The three choice are special diagnostics functions that are not normally to be called up by the user. COLD START eliminates all the previous calibration constants and restores them to known nominal values. A COLD START is especially useful for removing scrambled data from the NVRAM and is required in the event that the NVRAM or keep-alive battery has to be replaced. After a COLD START, a partial recalibration is required to return the instrument to its previous state.

FORCE DAC is a special diagnostic tool that permits the service technician to change the value of selected adjustment constants as an aid in troubleshooting parts of the internal circuitry, especially the digital-to-analog converter circuitry and all the output sample-and-hold circuits of the DAC System. CAL PATH ON/OFF turns on or off the calibration signal path to the Peak Detectors. It is a useful diagnostics device in the event that large offset errors have driven the display off-screen. Switching CAL PATH ON eliminates the Attenuators and Preamplifers from the input signal path and places the calibration reference level on the display. If that brings the display back on screen, the offset problem may be isolated to the Attenuators or Preamplifiers; if not, then the problem may be in the Peak Detectors or CCDs.

Power-On Self Diagnostics

At instrument power-on, a self-test sequence is executed automatically in the first 15 seconds. If the instrument has been calibrated and no hardware errors are detected, the instrument will come up in the acquisition mode in effect at power off. If errors are detected or if part of the instrument is uncalibrated, the instrument will come up in the EXTENDED DIAGNOSTICS menu with errors displayed and/or the message "UNCALD" at the bottom of the display area above the menu selection labels (see Figure 6-4). Exiting the EXTENDED DIAGNOSTICS mode if the menu is displayed is done by pressing the MENU OFF/EXTENDED FUNCTION button.

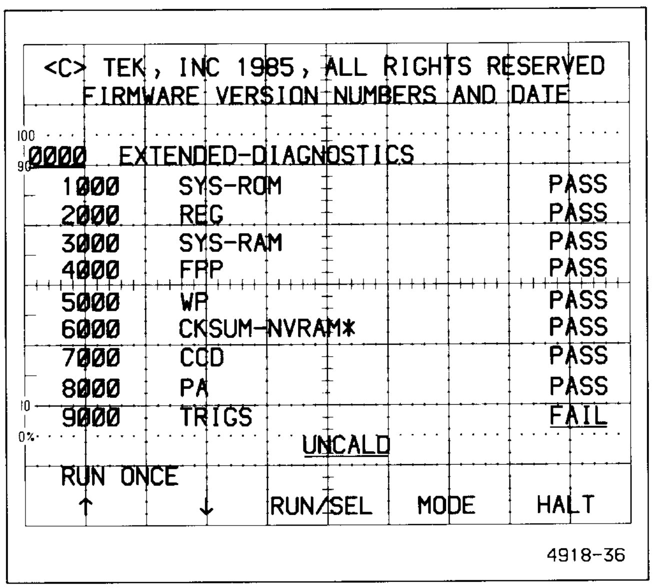


Figure 6-4. Main EXT DIAG Menu.

As the power-on diagnostic tests are being performed, the Trigger LEDs are flashed in a coded sequence to indicate the level of test being run. In a normal sequence with no failures, the tests run quickly, and the length of time that an LED is lighted may be very short. If a failure occurs, the Trigger LEDs are used to flash a binary code of the FIRST failed test (see Figure 6-5 for the binary codes of the LEDs). This failure display is important; it may be the only troubleshooting clue available if, for any reason, the 2430 cannot display the extended diagnostics menu.

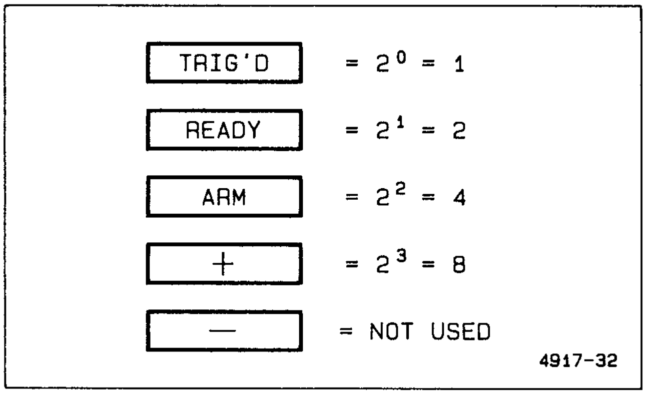


Figure 6-5. Trigger LED binary coding for diagnostic tests.

For example, if test 2130 should fail, an observer will see the following flashes of the LEDs to indicate the failed test number:

1. All the LEDs are lighted at the beginning of the power-on sequence to check that they all are capable of being turned on.

2. The TRIG'D LED is lighted to show that tests at level 1000 are being run, then the READY LED is lighted to show that 2000 level tests are being run. (Some test levels are done very fast, and the LEDs do not remain on long.)

3. When the test failure occurs, all the Trigger LEDs are lighted and held on for a period of time to indicate a failure has been found; then the sequence of turning on the LEDs begins for the code number of the failed test.

4. For the first number of the failed test, the READY LED turns on for a binary 2 (the failed test is in the 2000 level); all the LEDs are then turned on to separate the numbers of the test code.

5. The second number of the test number (one) is shown by turning on the TRIG'D LED for the binary code for 1, then all the LEDs are again turned on as the code number separator.

6. The third number of the failed test (three) is shown by turning on both the TRIG'D and the READY LEDs. Their binary values are summed (1 + 2) to obtain the third number of the failed test (three), and all the LEDs are again lighted to separate the numbers.

7. The fourth and final number of the failed test is 0, and all the LEDs remain off between the number separators code.

8. After flashing out the coded number of the first failed test, the diagnostics continues on with the remaining tests, if able to. Any additional failures found, if any, will NOT be flashed on the Trigger LEDs.

If you miss the code the first time (as is usual unless you are expecting a failure), you must turn off the 2430 and turn it back on again to rerun the tests. It takes a little practice to read the code from the LEDs.

Power-On/Self Diagnostics Test Failure

If the Self Diagnostics tests fail, either at power-on or when called by the user from the front panel, the "EXTENDED DIAGNOSTICS" mode will be entered. The menu displayed in Extended Diagnostics permits the user to determine which test(s) failed as a start in isolating the fault to the problem area (see Table 6-6). A failure of tests 6000-9300 does not necessarily indicate a fatal instrument fault. An abnormal power-off or transient power condition may have prevented the orderly shutdown that normally saves the data needed to return the scope to the operating state present at power-off. A failure of the SELF DIAGNOSTICS will also occur if the present temperature of the scope is very different from the temperature during the last SELF CAL. In the last case, the stored calibration constants may not permit accurate measurements to be made.

NVRAM Failure

Anything that causes bad data to be stored in the NVRAM (nonvolatile RAM) will cause a failure of one or all of the 6000 level tests (CKSUM-NVRAM). Loss of stored data from the NVRAM can cause seemingly unrelated failures in the diagnostic tests. That is because all the fail flags and calibration constants against which the current testing is performed are stored in the NVRAM. Checking against erroneous data and marking failures using bad flags provides failure indications not related to a hardware failure. Doing a "COLD START" (see "Special Diagnostic Features") loads all the NVRAM locations with known nominal values and removes the invalid data. This permits SELF CAL and testing to be completed correctly. Replacing the NV RAM or the Lithium storage battery requires a COLD START to restore the NV RAM data to known values. Even though the SPECIAL menu choices may be disabled from front-panel access, a COLD START is done automatically when the instrument finds no stored calibration constants during the first power-on after the replacement.

At power-on, the 2430 checks the self-calibration constants, waveform data, waveform scaling factors, and power-off front-panel control settings stored in the instrument. Failure of a 6000 subset diagnostic test indicates a checksum failure of the stored data in the nonvolatile RAM. If test 6100 fails, tests 6200 and 6300 in the subset are not done. The causes of a failure in this area may be non-fatal to continued instrument operation, and normal (or near-normal) operation may be recovered by the user.

Loss of calibration constants (failure of CAL-CONSTANTS test 6100) causes the instrument to do a "COLD START" with the resulting replacement of all calibration constants by predetermined nominal values. After a COLD START, all previously stored waveforms are invalid (saveref memories will be marked "EMPTY" and none of the VERTICAL MODE waveforms can be called up for display until valid data is obtained), and an INIT PANEL is done to set all the front-panel controls and GPIB states to their INIT values (see Table 6-7 at the back of this section for a complete list of INIT settings).

Continued scope operation after a COLD START is obtained by first performing the SELF CAL procedure to restore the automatic calibration constants. (Pressing the up-arrow menu button shown in the EXTENDED DIAGNOSTICS menu returns to the main CAL/DIAG menu with the SELF CAL choice.) SELF CAL takes a little more time to complete than normal after a COLD START. This is because the nominal starting point values for the calculations are farther from the correct results than the previously calculated SELF CAL constants.

NOTE

DO NOT TURN THE 2430 OFF WHILE THE SELF CAL ROUTINE IS RUNNING. Turning off the power prior to completion of SELF CAL will again invalidate the instrument calibration constants. The SELF CAL routine must also be allowed to complete before the MENU OFF/EXTENDED FUNCTIONS button is pressed to obtain a valid calibration.

After SELF CAL has been done, the REPET cal in the EXT CAL menu must also be done if the scope is to be operated in the REPET mode. The ATTEN and TRIGGER choices (normally disabled to the user) in the EXTENDED CAL menu are labeled "UNCALD" after the COLD START. Pressing the MENU OFF/EXTENDED FUNCTIONS button returns the scope to the operating mode for near-normal operation. The COLD START nominal calibration values supplied for the ATTEN and TRIGGER calibration permit normal measurements to be made, but with slightly reduced vertical gain and trigger level readout accuracy.

Replacement of the calculated ATTEN and TRIGGER calibration constants by a COLD START causes the scope to enter the EXTENDED DIAGNOSTICS mode with the "UNCALD" message displayed for each following power-on. The ATTEN and TRIGGER choices in the EXTENDED CAL menu will also be labeled UNCALD. These messages are there to remind the user that the scope must be referred to a qualified service person to replace the nominal COLD START calibration constants with actual calculated values. External test equipment and access to inside of the scope are required to perform the EXTENDED CAL procedures needed.

Loss of the stored power-off front-panel settings (failure of FP-LAST test 6200) causes the scope to do an INIT PANEL on power-up (see Table 6-7 for the INIT settings). Recovery of normal operation is done by pressing MENU OFF/EXTENDED FUNCTIONS to exit EXTENDED DIAGNOSTICS and resetting the front-panel controls to the required settings for the measurement to be made. The "FAIL" condition for test 6200 will be reset to PASS and the scope will not enter EXTENDED DIAGNOSTICS on the next power-up if permanent failure of the memory has not occurred.

Loss of the waveform scaling factors (failure of WFM-HEADERS test 6300) causes all waveforms to be invalid. On power-on, invalid waveforms are turned off and not permitted to be called up for display and saveref memories are marked "EMPTY." Exiting EXTENDED DIAGNOSTICS by pressing the MENU OFF/EXTENDED FUNCTIONS button then pressing ACQUIRE to obtain valid waveform data permits continued normal operation of the scope.

Loss of individual waveforms from the SAVE memory, a short-term nonvolatile RAM, will not cause a power-up test failure. Such a loss can occur if the scope remains off beyond the nonvolatile time limit of the SAVE RAM (three to five days without powering on the scope). If the scope was acquiring when turned off, it will be in the ACQUIRE mode when turned back on, and if the scope is triggered, new waveform data will fill the waveform record. If the scope was in the SAVE mode when turned off, the user is notified of the waveform data loss by replacing the invalid waveform(s) with a horizontal line broken by full-screen fill areas (broken line of dots with vectors off). Simply acquiring new waveform data in any affected memory restores the display to normal. If saveref memory REF4 has been set to store front-panels rather than the fourth reference waveform, those front- panel setups in RECALL locations 2-5 may be lost by a long-term power off. An attempt to recall an invalid front-panel setting will ring the warning bell, and no changes to the current front-panel settings will be made. New front-panel setups have to be saved to replace the ones lost.

Calibration Test Failures

Failure of diagnostic tests numbers 7000 through 9300 may indicate that instrument calibration is invalid at the present temperature. If that condition occurs, the instrument will enter the EXTENDED DIAGNOSTICS mode, and an "UNCALD" message will then be displayed. Such a non-fatal condition might exist if the last SELF CAL was done at an operating temperature that is very different than the present temperature of the scope.

In this case, the power-on self diagnostics detect that the stored calibration constants may not permit accurate measurements to be made. Recovery is made by allowing the instrument to warm up ("NOT WARMED UP" message not displayed in the main CAL/DIAG menu) and running the SELF CAL procedure to recalculate the calibration constants.

A diagnostic test number of 7000-9300 that continues to fail diagnostics after SELF CAL is done indicates that some condition exists that prevents correct operation. The scope may still be operational for limited use, depending on the nature of the failure. For example, if the failure is in the CH 2 side only, CH 1 may still be used for making measurements with confidence that the required vertical accuracy is available. Exit the Extended Diagnostics mode by pressing the MENU OFF/EXTENDED FUNCTIONS button to operate the scope.

CALIBRATION/DIAGNOSTICS OPERATION

All the 2430 calibration and diagnostic routines are accessible through the EXTENDED FUNCTIONS menu and via the GPIB. The EXTENDED FUNCTIONS menu is selected by the MENU/EXTENDED FUNCTIONS button when no other menus are displayed. Pressing the bezel button under the CAL/DIAG menu choice that appears, produces the following menu display:

<status>	<status>	<status>	<warm-up>
SELF	EXT	SELF	EXT
CAL	CAL	DIAG	DIAG

<status> indicates the most current result of the test or calibration, which is a result of the last text ran. A failure occurring after having passed a test does not automatically change the status; a new test must be done to determine the current status each time EXTENDED DIAGNOSTICS is entered from the front panel.

For calibration <status> can be:

UNCALD	instrument has not been calibrated.
FAIL	hardware errors were detected during calibration (calibration may not be valid).
PASS	the instrument was successfully calibrated.

For diagnostics <status> can be:

(blank)	test has not been executed.
FAIL	test failed on last attempt.
PASS	test passed on last attempt.

<warm-up> is the warning "NOT WARMED UP" which is displayed for approximately ten minutes after power-on. Calibrating the instrument during this period is not recommended.

NOTE

The "NOT WARMED UP" message is displayed after every power-on for the eight minute period, even if the scope is turned off and then right back on. In this case, calibration may be performed as soon as the instrument has stabilized after power-on.

Self Calibration

A complete Self Calibration of the instrument is executed when SELF CAL is pressed. If no errors are detected during the calibration sequence, the instrument returns to its pre-self-calibration status condition. Any detected error puts the instrument into the initial EXTENDED DIAGNOSTICS menu shown in Figure 6-4 with the appropriate error(s) indicated.

NOTE

If, after running SELF CAL, any test sequence fails SELF DIAG, it is recommended to the user that the instrument be brought to the attention of a qualified and authorized service person.

Extended Calibration

NOTE

If Extended Calibration is internally disabled, the scope will not respond to a press of the menu buttons in the EXT CAL menu.

Pressing the EXT CAL button selects the Extended Calibration menu:

<status> <status> <status>
ATTEN TRIGGER REPET ADJUSTS ↑

A choice of any of the four selections begins execution of the indicated semi-automatic calibration routine. Pressing the up-arrow button returns to the CAL/DIAG menu level. The correct dc test voltage must be available to complete the ATTEN and TRIGGER calibration.

EXT CAL routines can be aborted at any time by pressing the MENU OFF/EXTENDED FUNCTIONS button, but once a calibration choice (except ADJUSTS) is started, it must be successfully completed or the status will be FAIL.

Power-On Self Diagnostics

At instrument power-on, a self-test sequence is executed automatically in the first 15 seconds. If the instrument has been calibrated and no hardware errors are detected, the instrument will come up in SAVE acquisition mode. If errors are detected or if part of the instrument is uncalibrated, the instrument will come up in the EXTENDED DIAGNOSTICS menu with errors displayed and/or the message "UNCALD" at the bottom of the screen. Exiting to the Scope Mode from the EXTENDED DIAGNOSTICS mode is done by pressing the MENU OFF/EXTENDED FUNCTIONS button.

Front-Panel Self Diagnostics

Pressing the SELF DIAG button from the CAL/DIAG menu also causes execution of the complete Self Diagnostic test sequence. If no self-test errors occur, the word "PASS" will appear in the <status> position. If errors are detected, the instrument will be put into the EXTENDED DIAGNOSTICS menu with the appropriate errors displayed, if possible.

Extended Diagnostics

From the CAL/DIAG menu, a choice of EXT DIAG calls up the Extended Diagnostic menu. The display is:

<mode>
↑ ↓ RUN/SEL MODE HALT

<mode> indicates which looping mode is selected.

On entering the Extended Diagnostics, a list of the top-level tests with their most recent status—PASS, FAIL, or blank (indicating that the test has not been run)—is displayed (see Figure 6-4). In addition, if the instrument is not fully calibrated, the word "UNCALD" is displayed near the bottom of the screen above the menu button choices.

The display of test selections in the Extended Diagnostics menu is a hierarchically structured set of tests in lists containing the test numbers, test names, and last status of the test results. If the test has not been run since the last "COLD START," no status will be displayed. If an upper level test in the set (such as REG) is run, all tests in the REG test hierarchy will be done and labeled with a PASS or FAIL status.

UP/DOWN ARROWS. The up-arrow and down-arrow buttons move an underscore pointer through the displayed list of diagnostic tests. Moving the pointer to a diagnostic below the title line and then pressing the RUN/SEL button selects a menu of tests available at the next level down with that diagnostic. Moving the pointer up above the title line returns to the next level of hierarchy in the menu (if not at the top line). If at the top line of 0000, a press of the up-arrow button returns the CAL/DIAG menu choices.

A press of RUN/SEL with the pointer at the title line, causes all the tests at and below that diagnostic level to be run. An individual test can be selected by using the arrow keys to move the pointer to the desired test then pressing the RUN/SEL button. The cumulative result of any test run will be displayed on test completion at the right of the title line. This will be either PASS, FAIL, or blank if an attempt was made to run a non-automatic test.

NOTE

A diagnostic name in the Extended Diagnostic menu followed by an asterisk is not testable. The asterisk indicates either that the test is accessible for calibration only using the EXT CAL menu choices or that it may be checked at power-on only. The PASS/FAIL message displayed indicates the results of the last Extended Calibration or the last power-on check. A FAIL label on an asterisked test will be accompanied by an "UNCALD" label above the bezel button labels. An UNCALD label also appears above the uncalibrated selection of the EXT CAL menu.

MODE. The MODE button rolls through the manner in which a selected test will be run. The choices are RUN ONCE, RUN CONTINUOUS, RUN UNTIL FAIL, and RUN UNTIL PASS. If RUN CONTINUOUS is chosen before starting the selected test, it will be continually executed until the HALT button is pressed. The choice of RUN UNTIL PASS and RUN UNTIL FAIL may also be stopped using the HALT button. In addition, all tests (except a looping Front Panel μP test) can be aborted with the MENU OFF/EXTENDED FUNCTIONS button. Selecting to run an asterisked test automatically switches to RUN ONCE, and the test does not run.

HALT. Pressing HALT causes all diagnostic test activity to stop at the finish of the current test in progress. It is especially used to halt a continuously running test.

DIAGNOSTICS OPERATION VIA THE GPIB INTERFACE

Operation of the GPIB interface is described in Appendix A of the Operators Manual. This additional information describes use of the diagnostic commands. Operation of any of the four Cal/Diagnostic modes is selected by using the keywords SELFCal, EXTCal, SELFDiag, or EXTDiag as arguments with the TESTType command via a GPIB controller. The selected TESTType will start when the EXEcute command is received. See Table A-14 in Appendix A of the Operators Manual for the definition of the GPIB calibration and diagnostics commands.

Self Calibration

If TESTType SELFCal is selected, the Self Calibration portion of the test sequence will run in its entirety when the EXEcute command is received. A service request (SRQ) will be issued when the sequence is finished if the OPC mask is on. The status byte received by the controller will indicate if the test completed either with error or with no error. See Table A-16 of Appendix A of the Operators Manual for a list of the status bytes.

If an error occurs during SELFCal, it is reported to the controller when the ERRor? query is issued to the instrument. ERRor? returns a string of error numbers (up to nine) resulting from the last EXEcute command. These numbers will be the highest order in the hierarchy of the SELF CAL routine; so, to locate the exact test that failed in the tree, the TESTNum must be set to a lower level and the ERRor? query reissued until the lowest detection level of the failure is reached. The ERRor? query returns 0 if no errors have occurred. This method of failure location is used for errors generated by any of the calibration or diagnostics sequences.

Extended Calibration

The EXTCAL TESTtype allows specifying the calibration sequence (TESTNum) to be performed. The calibration routine specified may be any steps or sub-steps of the EXT CAL or SELF CAL routines. The user is responsible for assuring that any externally required test equipment has been connected and programmed, and that pauses in the procedure to make manual adjustments or equipment changes are terminated via a 2430 menu button push or a GPIB STEp command to advance to the next step in the sequence. The external calibration sequence numbers to be used as the numerical argument for TESTNum are listed in Table 6-6 under the "Test Number" column heading. The valid test numbers for Calibration are 7000 to 9300 in the table. Error handling is the same as in SELFCal.

Self Diagnostics

Invoking the TESTType SELFDiag causes execution of the entire self-diagnostic sequence when an EXEcute command is received. Error handling is the same as in SELFCal.

When Self Diagnostics is called via the GPIB, completion and/or failure will cause an SRQ to be issued by the instrument. The status bytes returned on a poll indicate a successful completion or failure of the Self Diagnostics sequence. Errors can then be queried via the GPIB and traced to the lowest level of the Extended Diagnostics in the same manner as from the front panel. Failure of Self Diagnostics when run from the GPIB does not put the instrument into the Extended Diagnostics menu as it does when run from the front panel.

Extended Diagnostics

TESTType EXTDiag allows a specific TESTNum to be selected for execution upon receiving an EXEcute command. Error handling and reporting is the same as in SELFCal. Looping a test is done by issuing the LOOp command prior to the EXEcute command, and the HALt command stops the looping test.

DIAGNOSTIC PROCEDURES

The various tests resident in the 2430 are organized into a tree structure with a test number designating each node. The root node is 0000. A summary of the way in which the tests are performed and the type of test made follows the test number and test name in Table 6-6.

NOTE

FAIL and PASS flags in the Extended Diagnostics menu show the results of the last test ran. If a defective device that has previously caused a FAIL flag to be set is replaced, the test must be run again to obtain a PASS indication in the menu.

These troubleshooting procedures are broken down into several types. The 2430 Troubleshooting Procedures of Table 6-6 provide a description of the tests made and, in many cases, the troubleshooting procedure used in case of a test failure. Video Option troubleshooting procedures are given in Table 6-7. Other areas of the 2430 require more extensive troubleshooting trees. These areas are: the Low Voltage Power Supply, the Display System, and System Clocks. Troubleshooting trees are located in the "Diagrams" section of this manual. Some of the troubleshooting procedures are very general, in that they don't lead the troubleshooter directly to a specific component or components that may be faulty. In those cases, it is up to the troubleshooter to analyze the information obtained from the tests made to determine the actual fault. Figure 6-6 is a flow chart that shows the initial troubleshooting steps as an aid in determining where to start.

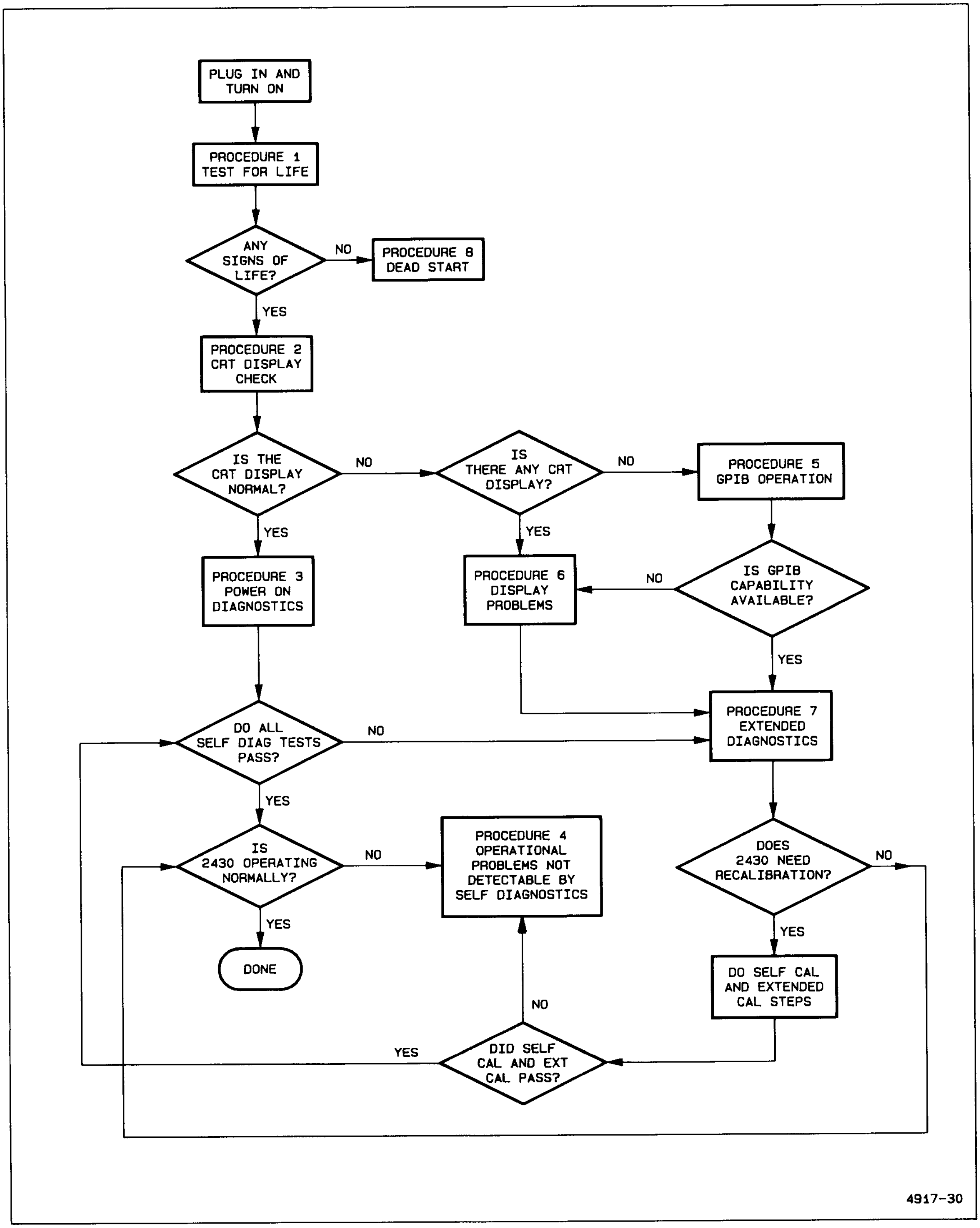


Figure 6-6. Initial troubleshooting chart.

Table 6-6

2430 Troubleshooting Procedures

1	**INITIAL INDICATIONS**
TESTS FOR LIFE	1. Are TRIGGER LEDs flashing? If all lights are flashing, suspect Waveform μP ROM U480 or U490 (diagram 2) or their selects. 2. Is there activity from GPIB LEDs during turn-on? If the three LEDs above the 2430 crt (LOCK, SRQ, and ADDR) all light then go through a binary counting pattern (test number 2170), the diagnostics are working, and the instrument is alive. Go to Procedure 2. 3. After 30 seconds of turn-on, press MENU OFF and cycle the SLOPE switch. If the + and − Slope LEDs light alternately, the System μP is alive, and the operating system is active. Go to Procedure 2. 4. Did the attenuator relays click? If the relays clicked, the power-on self tests were running. 5. If any of the signs-of-life occurred, then assume that there is some "life in the box" and go to Procedure 2; otherwise, go to Procedure 8.
2	**CRT DISPLAY CHECK**
	1. If the menus are normal (can focus, adjust intensity, etc.), then go to Procedure 3. 2. If there are no displays then go to Procedure 5. 3. If there is a display, but the display is incorrect (no intensity control, out of focus, etc.), a dot only, a vertical or horizontal streak, then it is an analog problem. Go to Procedure 6. 4. If portions of the readout are missing or wrapped over, but the power-on test runs, the front-panel controls and the EXT DIAG menus may still be useful. Attempt to use the diagnostics to determine the failed tests. Also, read the binary code of the first failed test that is flashed by the Trigger LEDS during the power-on sequence. Use that information as a starting point for troubleshooting, using the steps indicated for the failed test in Procedure 7, "EXTENDED DIAGNOSTICS". The most probable cause of a failure of this type is a bus problem or bad IC on a bus causing a stuck bit in Display circuitry of the Time Base/Display board (schematic diagrams 16 and 17). The busses to suspect are the ones connected to the IC indicated by the failed test.
3	**POWER-ON DIAGNOSTICS**
	NOTE: THIS IS NOT SELECTABLE, IT EXECUTES AT POWER-ON. 1. If all the power-on tests pass, go to Procedure 4. If not, then go to Procedure 7.
4	**OPERATIONAL PROBLEMS (Not detectable by diagnostics)**
NO SIGNAL ACQUISITIONS	Phase Clock Array Outputs A10U470 (schematic diagram 11) 1. Check A10U470 (Phase Clock Array) at pins 13, 14, 15, and 16 for output clocks. 2. If no outputs, the problem is probably U470 or the input circuit to U470 at pins 65 and 67; i.e., CR580, C580, or C462. 3. If U470 is replaced and outputs are obtained, do the following test: turn the 2430 to the setting 5 ns/div, REPET ON, NORMAL acquisition. Insert a 30 MHz sine-wave into CH 1. Watch the waveform as it is created on screen. Make sure no misplaced samples occur 20 ns after they should (this will be obvious by the appearance of spikes on the screen within about one minute). If this happens, replace gate array again until the problem goes away. 4. If the Phase Clock Array is working, the problem is the Time Base. See the Time Base troubleshooting chart located in the "Diagrams" section of this manual.

Table 6-6 (cont)

TIMING ERROR AT 50 μs/div AND FASTER

Phase-Locked Loop Circuit (schematic diagram 11).

1. Check the 4 MHz input to U381 pin 6. If there is no 4 MHz clock at TP174 then go to the Timebase troubleshooting chart (located in the "Diagrams" section) and troubleshoot the System Clocks.

NOTE

Use 2430 CURSOR function of 1/TIME to measure the frequency. The cursor position difference will read out directly in frequency.

2. Check U381 pin 9 for 4 MHz if SEC/DIV is 50 μs, and 5 MHz if SEC/DIV is 20 μs.

   Frequency too low at pin 9:

   a. Check that U381 pin 3 has negative pulses and that the voltage at U381 pin 12 is positive with respect to U381 pin 3. The VCO CTL voltage at TP581 can be as high as +12 V.

   Frequency too high at pin 9:

   b. Check that U381 pin 12 is ramping negative with respect to U381 pin 3 (average not absolute) and TP581 can be as negative as −0.6 V.

   c. If these conditions are not true, the problem is probably Phase/Frequency Detector U381 or amplifier U580.

MISSING DATA POINTS IN REPET

Jitter Correction Troubleshooting (schematic diagrams 12 and 13):

On the 2430 under test, select REPET acquisition mode, AUTO LEVEL, VERT Trigger, DC Trigger COUPLING, and set the SEC/DIV setting to 5 ns. Then select ACQUIRE and connect a probe from the CH 1 input to TP345 (4C) (found above A10U450, the CH 1 CCD, in the main board).

If there are bands of missing data points every two divisions, only a few data points are placed every two divisions, or the waveforms are distorted, the problem may be in the Jitter Correction circuitry.

The Jitter Correction circuit has both analog and digital circuits. First check the digital portion to insure that it is working. If that is ok, then assume that the problem is in the analog portion of the Jitter Circuit.

However, if the Jitter Correction circuit is found to be working correctly and the waveforms are still distorted (specifically spikes), then the problem may be with the Phase Clock Array Outputs A10U470. To check U470, see NO SIGNAL ACQUISITIONS in this table.

DIGITAL SECTION TROUBLESHOOTING

1. Check that START1 and START2 are present at U841 pin 2 and U842 pin 2 (diagram 13) respectively and that they are coincident.

   a. Test the collector of Q492 and Q391 (diagram 12) for the START pulses.

   If missing:

   b. Check for SLRMP1 and $\overline{\text{SLRMP1}}$ at the bases of Q492 and Q491.

   c. Check for SLRMP2 and $\overline{\text{SLRMP2}}$ at the bases of Q391 and U390.

   d. Check for RAMP and $\overline{\text{RAMP}}$ at the bases of Q392 and Q490.

   If any gating signals are absent, backtrack to U470 and/or U370 (on diagram 11) and locate the defective component.

Table 6-6 (cont)

2. Check that STOP1 and STOP2 are present at U841 pin 12 and U841 pin 12. These signals are not coincident and should be jittering with respect to one another.

   If missing, backtrack to U490 and/or U390 (diagram 12) to locate the defective component.

3. While triggering on the START1 pulse, check for gated signal (by STOP1) at U852 pin 1. Check at U853 pin 1 for gated signal while triggering on the START2 pulse. If either gated signal is missing, check the gating components to locate the problem.

4. While triggering on the START1 pulse, check for activity (fast to slow) at the Jitter Counter (U852 and U853) outputs (pins 3, 4, 5, 6, 11, 10, 9, and 8). Observe that each output pin on the ICs should be switching slower than the preceding one as the counters count down. Replace the counter if found defective.

5. Check that the inputs to U752 are gated to the outputs of U752. The only time they are the same is if both pin 1 and 19 are low. If a WORD trigger probe is not available, the following setup may be used making use of the A and B Trigger Mode to obtain coincident triggering.

HORIZONTAL

A and B SEC/DIV	500ns
MODE	B

VERTICAL

MODE	CH 1 and CH 2
COUPLING	DC
VOLTS/DIV	2 V
POSITION	Traces to graticule center

TRIGGER

A TRIGGER SOURCE	EXT1 A*B
A LEVEL	500 mV
SLOPE	– (minus)
MODE	NORMAL
B TRIGGER SOURCE	EXT2
MODE	TRIG AFTER; EXT CLK OFF

Now connect the EXT1 to U752 pin 1 and EXT2 to U752 pin 19. The input-output pairs may now be checked, and they should compare at the "T" of the trigger point.

ANALOG SECTION TROUBLESHOOTING

1. Connect a probe from CH 1 of the 2430 under test to the 4C test point on its main board. Select REPET, set the 2430 under test to 5 ns/div and obtain a stable trigger.

2. Set the test scope to 500 μs/div.

With the test scope:

3. Make sure that the signal at the collector of Q491 and Q390 stabilizes at about 800 mV. This is the baseline stabilization circuit. The waveforms shown next to the schematic diagrams are useful to make waveform comparisons.

4. Check for a fast ramp that corresponds to RAMP and $\overline{\text{RAMP}}$ from U370. This ramp should rise from the stabilization level to a maximum and start down at the same time that the START1 (or START2) pulse steps high, and that the STOP1 (or STOP2) pulse steps high when the descending ramp crosses 0 V. If not, troubleshoot the circuitry to determine the problem. These ramps should be linear both in rise and fall times.

Table 6-6 (cont)

GPIB	GPIB Test for Activity (schematic diagram 20): 1. Press the OUTPUT menu button, then SETUP, then MODE. Select L/ONLY and see if the ADDR LED is on. Select T/L and see if the ADDR LED is off. Select T/ONLY and see if the ADDR again is on. 2. If the LEDs follow the above, GPIB IC U630 is at least responding to the System μP, and the problem is probably in GPIB Bus Buffers U720 or U624. 3. If the LEDs do not follow the above pattern, troubleshoot bidirectional buffer U532 or U630 (assuming the LEDs do the 0 through 7 binary count during REG test section of EXT DIAG).
FRONT PANEL PROBLEMS	Front Panel and Auxiliary Front Panel (schematic diagrams 4 and 6): If there is a front panel problem and the Extended Diagnostics have not detected anything, the problem is not in the Front Panel Processor or its handshake logic with the System μP. On the Front Panel μP (U700), do the following checks: **NOTE** *When probing around the Front Panel μP circuitry, it is possible to cause bad data to be written to the System μP and/or the Front Panel μP by inadvertent grounding of pins or accidental shorting of pins together. If this should occur, many trouble symptoms may be present. To cure these symptoms, turn off the 2430 and turn it back on again. This rewrites all RAM space in the System and Front Panel microprocessors with correct operating data.* 1. Check pins 26, 27, 28, 29, 30, and 15 for active output signal switching. These signals are all asynchronous, so a stable display pattern is not possible (without going to SAVE mode on the test scope). 2. If the signals checked in Step 1 are active, go to Step 3. If these signals are not actively switching, perform the Front Panel MUXTEST to check that the μP drives the MUXSEL signal lines in a tight looping routine. In the MUXTEST, only the MUXSEL signal output lines are being driven. No output will be seen on the S/$\overline{L}$ or SHCLK lines (pins 29 and 30 respectively). 3. Check pin 24 for active AOUT0 return signal from the Front Panel pots. 4. If the return signal line is active, go to Step 5. If it is not active, showing the different voltage levels from the Front Panel pots, troubleshoot Front Panel Pot Scanner U902 (an 8-to-1 multiplexer). Problems with a single pot output rather that a total failure of the Pot Scanner may be checked out using the MUXTEST mentioned in Step 2. 5. Check pin 25 for active return signal from the Front-Panel Switches. 6. If the SW/OUT signal line is active, the Switch Scanner circuitry is working. If it is not active, troubleshoot 1-of-8 decoder U903 and serial shift register U904 for correct operation. 7. Check pin 22 (AOUT2) for an active return signal from the Auxiliary Front Panel INTENSITY pot and Front Panel BNC connectors. Individual signal voltage levels may be checked using the Front Panel MUXTEST if the signal line is active. If switching levels are not present on the AOUT2 signal line, troubleshoot 8-to-1 multiplexer U600. 8. Check pin 9 (SWOUTA) for an active signal when one of the Auxiliary Front Panel buttons is pressed (bezel, SELECT, STATUS, MENU OFF). Otherwise, a HI is being shifted out of serial shift register U700. If the SWOUTA signal does not show a square pulse when one of the buttons is pressed, troubleshoot U700.

Table 6-6 (cont)

Front Panel MUXTEST:

An intermittent failure or noisy front panel pot can produce inconsistent control changes. To test individual pots for smooth operation and full range control limits, the Front Panel MUX SELECT test may be used to provide stable triggering.

1. Turn the power off and connect pins 2 and 3 of J155 together.

2. Ground the MUXINH signal at the end of R815 nearest the front of the 2430 to DGND.

3. Connect the test scope to observe the AOUT0 signal at R800 pin 8. Trigger the test scope on MUXSEL2 at R800 pin 4. Set the SEC/DIV switch to 100 μs and the VOLTS/DIV to 2 V.

4. Power on the 2430. When it does the power-on test, it will signal a test failure of 4300 on the Trigger LEDS, and there will be no display on the 2430 crt.

5. Rotate the following rate position pots:

   CH 1 Vertical Position
   CH 2 Vertical Position
   Horizontal Position
   Cursor/Delay Position

6. Check that the pots go into the rate region at both extremes of rotation and that the voltage level for each pot moves smoothly from one amplitude level to the other (approximately 0.5 V to 5 V total range) as the pot is rotated. See the test waveform illustration to identify the portion of the waveform associated with the control being rotated.

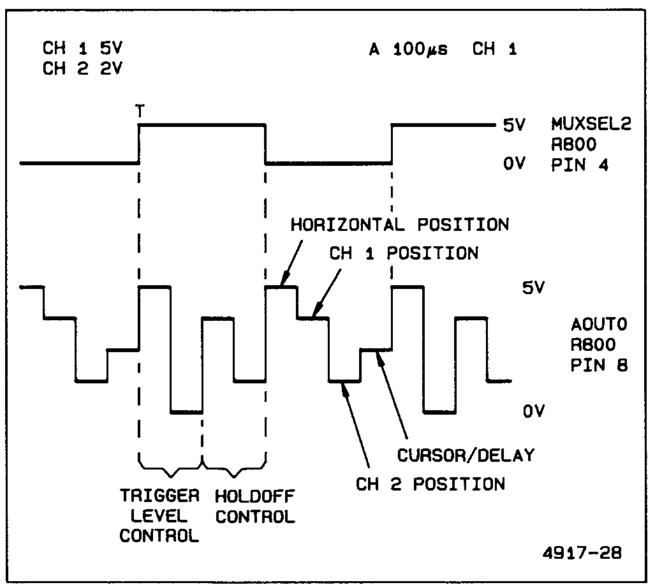


Figure 6-7. Mux Test waveforms.

7. Rotate the following infinite rotation pots:

   Trigger Level Control
   Holdoff Control

Table 6-6 (cont)

	8. Check that both sides of the pot have equal output range (approximately 0 V to 5 V) and that the voltage level for each side of each pot moves smoothly from one extreme to the other as the pot is rotated through the continuous range (not its end-switching region). 9. Connect the test scope to observe the AOUT2 signal at R809. This signal is from the Auxiliary Front Panel circuitry. 10. Momentarily short the shell of each of BNC input connectors to its coded-probe-switching ring and observe that the voltage level for that connector goes from 5 V to 0 V. 11. Rotate the infinite rotate INTENSITY pot and check for smooth voltage level changes on both sides of the pot (from approximately 0 V to 5 V). 12. The two remaining analog levels are the CH 1 and CH 2 50 ohm overloads. Check that they are approximately 3 V each.
BELL PROBLEM	Bell Circuit (schematic diagram 20): Remove the word trigger probe, then: 1. Connect a probe to the emitter of A12Q592. Then select the B TRIGGER SOURCE menu and press the BEZEL switch for WORD. The voltage should go close to +4 V with about a 1 V p-p, 2 kHz square wave superimposed upon it (peak of 5 V). If the 4 Vdc is not present, check the signal path back to A12U760 pin 16. If the 2 kHz is missing, check back to the oscillator circuit A12U274.
CALIBRATOR PROBLEMS	Calibrator (schematic diagram 13): **NOTE** *Make sure that you have not made the mistake of viewing the Calibrator signal output with a 10 MΩ probe and have the channel in 50 Ω input termination.* The calibrator circuit can be split into two parts. The source of the signal (CALCLK input at W122 pin 2) and the analog output stage on circuit board A13. 1. Check for a 3 V square-wave signal at the forward end of R831 (100 Ω resistor under A13U831 near the cable connector). If present, the problem is in U831, U731, Q831, or one of the parts in that output amplifier circuit. a. Check U831 pin 8 for a signal. b. Check U831 pin 2 for +2.4 V. c. Check U831 pin 1 for +5.1 V. d. Check emitter of Q831 is the same as the base of Q831. 2. Check for a 3 V square wave at A11U680 pin 18. If present, the problem is a defective cable connection from A11 to A13 boards. 3. Check for a square-wave signal at A11U680 pin 2. If present, replace A11U680. 4. Replace A11U670.

Table 6-6 (cont)

VIDEO OPTION	Video Option (schematic diagram 21): If TV triggers are selected and the menu says not installed, then the diagnostics have detected a problem (if the option is installed). See Table 6-7, the Video Option troubleshooting table.
WORD TRIGGER	Word Trigger (schematic diagram 20): 1. Make sure the Word Trigger probe connector is properly installed (connector is on the 2430 rear panel). 2. Select TRIG POSITION to 1/8, SEC/DIV to 100 μs, and VOLTS/DIV to 2 V. Probe A12U754 pin 5 for clock pulses. If not present, verify A12U754 pin 1 $\overline{\text{(RESET)}}$ is HI and A12U754 pin 11 has clock pulses. Replace A12U754 if the signals at pins 1 and 11 are ok. 3. Verify that the flex connector at the back of the A12 board is installed correctly. If ok, then the WORD RECOGNIZER probe is possibly defective. Try the probe on another 2430 to verify its operation.
DAC SYSTEM FAILURE	DAC System (schematic diagrams 5 and 6): Symptoms are CCD and Peak Detectors gain fails SELF CAL, and Trig Level fails SELF CAL. 1. Check TP650 (found on the Main Board) for 0 V. 2. Check TP660 (also on the Main Board) for +1.25 V. 3. If the test point voltages are good, the DAC SYSTEM is operating normally to this point. Troubleshoot the DAC multiplexers (U831, U821, and U830) and the individual DAC output ports (schematic diagrams 5 and 6). 4. If the levels at TP650 and TP660 are bad, check DAC multiplexer U651, the DAC inputs (U800 pins 1 through 12), and current-to-voltage converter U661. Should see U661 having an output of 32 dc levels, switching from one to the next each 2 ms, and then repeating. The maximum output level is ±1.36 V. This output signal should be present at the input to each of the DAC multiplexers (pin 3), and each multiplexer output pin should have a steady dc voltage level present. 5. Check that only one DAC MUX enable at a time from U272 is LO. 6. Use the FORCE DAC test to check suspected output ports for correct control range.
Force DAC Test	1. Press the SPECIAL menu choice under Extended Functions and then press FORCE DAC. **NOTE** *The SPECIAL menu choices are normally disabled to the user and press of the SPECIAL menu button calls up the display "DISABLED—SEE MANUAL". To enable the choices for servicing, the cabinet must be removed and Jumper A13J156 (EXT CAL DIS on diagram 13) must be removed.* 2. The first and second bezel buttons are used to select through the DAC values to be tested. The INTENSITY knob sets the values. 3. Test suspected DAC circuits for correct voltage limits over the control range using the test points and values given in the following Force DAC Ranges table.

Table 6-6 (cont)

Force DAC Ranges

DAC Output	DAC Ampl Output	COLD START DAC VALUES	Voltage Range		Effect of Increasing Value
			0	4095	
CH1Bal CH2Bal	U641-7 U641-1	2048/0 V	−1.37 V	1.36 V	Trace shifts down
CH1Gain CH2Gain	U641-8 U641-14	668/−4.37 V	−6.48 V	1.58 V	Gain decreases
1POS 2POS	U630-1 U630-14	2048/5 V[a]	−4.35 V	−5.66 V	Trace moves up
PD11 PD13 PD21 PD23	U631-1 U681-7 U640-7 U640-8	2048/0 V	−1.37 V	1.36 V	Offset goes up Offset goes down Offset goes up Offset goes down
CT11 CT21	U840-1 U840-8	2048/0 V	4.06 V	10.89 V	3 side goes up 1 side goes down
CM11 CM13 CM21 CM23	U841-1 U841-7 U841-8 U841-14	1500/-0.37 V	−1.35 V	1.35 V	
OD11 OD13 OD21 OD23	U840-7 U840-14 U661-14 U631-14	2200/10.29 V	5.88 V	14.07 V	Gain increases
JIT1 JIT2	U661-1 U661-7	3841/−2.54 V	−7.69 V	−2.23 V	Fast Ramp Slope increases for more counts per sec
ALVL BLVL	U640-1 U640-14	2176/0.09 V	−1.37 V	−1.36 V	Triggers at lower point
GRAT	U520-10 U820-1	4095/14.66 V 4095/−3.34 V	0.83 V[b] 4.20 V	14.66 V −3.35 V	Decrease Grat intensity
INTN NORM RDOI	U820-8 U820-7 U820-14	3160/0.78 V 1640/−0.28 V 2050/0 V	−1.37 V	1.36 V	Increases intensity
CURS (CAL)	U610-3 U610-4 U610-6 U610-13 U610-15	2048/0 V	−1.37 V ~0 V ~0 V ~0 V ~0 V	1.36 V ~0 V ~0 V ~0 V ~0 V	Current output into 75 Ω loads

[a]DAC values for CH 1 and CH 2 POS need an acquisition after the COLD START to be rewritten. Turn off EXT DIAG menu and press acquire; then go to FORCE DAC.

[b]Limits at a DAC count of approximately 2000.

Table 6-6 (cont)

Force DAC Ranges (cont)

DAC Output	DAC Ampl Output	COLD START DAC VALUES	Voltage Range		Effect of Increasing Value
			0	4095	
HORF	U631-8	100/−3.90 V	−4.11 V	4.09 V	Increases holdoff
DACO	U650-6	2048/0 V	13.92 V	−13.15 V	Unbalances DAC
DACG	U660-6	3929/−0.21 V	14.02 V	−13.32 V −5.18 V[c]	Uncalibrates DAC

[c]DACG (DAC gain) is interactive with DACO (DAC offset), and the DACG range can be limited if DACO is not centered. Changing either DACG or DACO will cause the remaining DAC System outputs to be invalid until the correct settings for DAC gain and offset are rewritten into the DAC System.

HOLDOFF PROBLEMS

Trigger Holdoff Circuitry (schematic diagram 13):

Run Extended Diagnostic test 2600 for the SIDE-BOARD registers U761 and U762. If that fails, troubleshoot the indicated failure.

If not, troubleshoot the Trigger Holdoff circuitry.

1. Check the emitter voltages for logical HI/LO as follows:

SEC/DIV	Q761	Q771	Q772	Q783
500 ns	HI	LO	LO	−15 V
1 μs	LO	HI	LO	−15 V
10 μs	LO	LO	HI	+5 V

If these levels are not correct, suspect the corresponding emitter diode, or the transistor emitter-base junctions as being defective. Observe that Q783 has no emitter diode, so suspect the transistor itself or Q782.

Some triggering failures are an indication of possible problems with the ATHO (A trigger holdoff signal). If ATHO is stuck HI, no triggers will be permitted by A/B Trigger Logic Array U150; if stuck LO, the triggering will be unstable.

2. Check the signals around flip-flop U872 for proper action of that device (see the test waveforms associated with the circuit next to schematic diagram 13).

Test scope: Select ENVELOPE 1 and AUTO TRIGGER MODE. Scope under test: Select 5 ns/div, trigger on the CAL signal, and set HOLDOFF to minimum.

X-Y PLOTTER OUTPUT

X-Y Plotter Circuitry (schematic diagram 20):

1. Check that the signals at A12U120 pins 5 and 8 are the same. Replace A12U120 if they are not.
2. Check that the signals at A12U120 pins 3 and 4 are the same. Replace A12U120 if they are not.
3. Test that the B and C multiplexer selection lines are HI (A12U130 pins 9 and 10) and that the enable line is being driven from HI to LO during plotting.

If not there, troubleshoot A12U760 and A12U884 to determine why the select is not being generated (both shown on schematic diagram 1).

Table 6-6 (cont)

	4. Check that the signals on pins 4 and 15 are at −2 V when not plotting. If not ok, replace A12U130.
PEN LIFT PROBLEM	Pen Lift Circuitry (schematic diagram 20): PIN WON'T OPEN: Check Q402 collector for +5 V. If not correct, then either the transistor is defective, the drive to it is incorrect, or the relay coil K302 is open. If A12Q402 is +5 V, and the relay is closed, replace K302. PIN WON'T CLOSE: Check Q402 collector for +0.3 V. If not correct, then either the transistor is defective, the drive to it is incorrect, or the relay coil K302 is open. If A12Q402 is +0.3 V, and the relay is open, replace K302.
5	**GPIB CAPABILITY AVAILABLE FOR EXTENDED DIAGNOSTICS**
	Extended Diagnostics test may be run via the GPIB interface to track down failed devices when the Front Panel is locked up due to a front-panel failure or when there is no display visible. The importance of this is that the initial step of locating all problem areas is simplified when the 2430 can do it itself. 1. If the hardware and software are available to interface a 2430 to a GPIB controller, then run the Extended Diagnostics test. Troubleshoot any failed diagnostics test as indicated in Procedure 7. 2. If GPIB interface is not available, go to Procedure 6 to troubleshoot the display problem.
6	**DISPLAY TROUBLESHOOTING**
INTENSITY	No Intensity (HV Supply and CRT, schematic diagram 19): If there is no GPIB capability, troubleshooting is going to be more difficult if no display is available. The steps in this table address the analog problems not detectable by the Extended Diagnostics in any case. Digital failures of the Display System are covered in the troubleshooting tables in the "Diagrams" section at the back of this manual. 1. Press STATUS to set READOUT level. 2. If no display is present, check the crt intensity grid voltage (V1000 pin 3), the grid bias adjust, the crt cathode and heater circuits, and the crt anode HV. **WARNING** *A High Voltage probe is required to measure the grid, cathode, and anode voltage of the crt.* 3. If no voltages are present, troubleshoot the HV power supply. The −15 V Unreg supply is fused by F961 (schematic diagram 23) which will be open if a component failure in the HV power supply caused excessive loading.

Table 6-6 (cont)

4. If crt voltages are good, and still no intensity, turn off the 2430 and check the crt heater for continuity from pins 1 to 14. If open, change the crt.

5. Does intensity vary with the Grid Bias Adjust? If not, troubleshoot the DC Restorer circuit. If it does, check the signal from U227 at pin 13.

6. Check input to U227 $\overline{ZON}$ on pin 3. If input ok, check supply voltages to U227. If all ok, change U227.

7. If $\overline{ZON}$ not present, troubleshoot the Z-Axis Logic circuitry, U223C and input gates and signals (schematic diagram 17).

8. If all ok in the crt and Z-Axis circuitry, go to the "No Display" troubleshooting tree at the back of this manual. Also, check that the Power-on Self Test completes without hanging. (See "System µP Halts in Power-up Test" following "No Intensity Control.")

No Intensity Control

1. Check signal output of U227 at pin 13. Is the waveform correct (see waveform 145 on schematic diagram 19), and does its amplitude vary with the DISP INTENSITY control? If yes, then check the signal path components to the junction of CR442 and R546 for continuity.

2. If the signal at U227 pin 13 does not vary with the DISP INTENSITY control, check CR135 for open or short.

3. Check the $\overline{ZINT}$ signal on pin 2 of U227. Does it vary correctly with the DISP INTENSITY control? If yes, suspect U227. If no, then use the FORCE DAC test to verify the INTENSITY pot and the DAC SYSTEM.

4. If the INTENSITY pot changes the DAC settings in the FORCE DAC test, the pot and pot-scanning circuitry are ok; if not, troubleshoot the Front Panel.

5. Check the suspected DAC outputs at the points indicated in the FORCE DAC test table. If DAC outputs are ok, troubleshoot Intensity multiplexer A10U811 (schematic diagram 6) and its select signals, and the Z-axis signal amplifiers (A10U810 and A10U812). Troubleshoot DAC circuit if the DAC outputs are bad (see the DAC System troubleshooting procedure).

6. Check the DISDN signal at U414A pin 6 and the PRESTART + DISPLAY signal at U323A pin 3 for correct operation (schematic diagram 17). If not correct, troubleshoot the Readout State Machine (see the "No Display" troubleshooting tree at the back of this manual).

SYSTEM µP HALTS IN POWER-UP TEST

Test 3000—TRIG and READY LEDs on or Test 6000—READY and ARM LEDs on, and the 2430 Self Test has halted.

Problem is probably in the Display State Machine circuitry (schematic diagram 17) or the DISDN signal path to the System µP Interrupt circuit. Check that the DISDN signal is correct at U414 pin 6 (waveform 126 on schematic diagram 17); if not, troubleshoot the Display State Machine (see NO DISPLAY troubleshooting chart in the "Diagrams" section for typical Display State Machine waveforms). If the DISDN signal is ok, check the DISDN signal path to U580 pin 4 for continuity.

Test 8000—plus (+) LED on and Self Test has halted.

1. "Running Self Test" message is displayed, but nothing else is occurring.

Check the ACQDN signal at A11U670 (Time Base Controller).

Table 6-6 (cont)

	2. No display is seen. Check operation of the Readout State Machine.
FOCUS	If all the focus voltages and adjustments are correct in the following checks and proper focusing cannot be attained, suspect a defective crt. Check all the crt voltages and EXT CAL Display ADJUSTS for the crt to verify their accuracy before changing a suspected crt. No Focus at Any Intensity: 1. Check the ASTIG adjustment. 2. Check junction of R262 and R145 for a voltage swing of 0 to 15 V as the FOCUS pot is adjusted from one extreme to the other. If not correct, troubleshoot pot, connectors between the pot and the junction, and the 15 V supply to the FOCUS pot. 3. Check at the collector of Q152 for a voltage swing of −175 V to −115 V as the FOCUS pot is adjusted from one extreme to the other. 4. Check for −300 V at the junction of R248 and R247. If not correct, check CR611, CR610, C618 and the 150 V peak ac supply. **WARNING** *An HV probe is required for the following step.* 5. Check the intensity grid, cathode, and anode voltages for correct levels. If not correct, troubleshoot faulty circuit. Poor Focus at High Intensity: 1. Check the HIGH DRIVE FOCUS adjustment. 2. Check the wiper of R400 for a varying voltage as the DISP INTENSITY is increased to high intensity levels. If not correct, check Q500, CR500 and VR316 for shorts or opens. 3. If the output of R400 tracks the display intensity changes, check R395, R297, C295, and P174. Poor Edge Focus: 1. Check the EDGE FOCUS adjustment. 2. Check the collector of Q269 for a voltage swing of −131.8 V to −111.8 V as the EDGE FOCUS pot is adjusted from one extreme to the other. Check the wiper of R300 for a voltage swing of 0 to 50 V as the pot is adjusted from one extreme to the other. If not correct, check the pot and the +61 V supply.
DEFLECTION PROBLEM	Display Output (schematic diagram 18): Vertical Deflection Bad (Horizontal stripe only) or Horizontal Deflection Bad (Vertical stripe only). 1. Press SAVE/RECALL SETUP and then press the fifth menu selection button to do a PANEL INIT. 2. Connect the CALIBRATOR output signal to the CH 1 BNC using one of the supplied 10X coded probes. Set the 2430 VOLTS/DIV setting to 200 mV. Press SAVE on the 2430, then MENU OFF.

Table 6-6 (cont)

3. Trigger the test scope on the $\overline{\text{ZON}}$ signal at U223 pin 8 (schematic diagram 17). Set the test scope Trigger Coupling to HF Reject and Slope to – (minus).

4. Use the test scope to compare the circuit signals at the points indicated in schematic diagram 18 to the corresponding waveforms shown next to the diagram. (The HOLDOFF control will be of some use in obtaining a stable display if using an analog scope. If using a 2430 as the test scope, press SAVE to obtain a stable display, if necessary, for viewing.)

5. Troubleshoot as necessary if incorrect waveforms are found. If none of the waveforms are correct, problem is either U170 or bad input from the Vertical Display DAC, (U142) for bad vertical deflection. For bad horizontal deflection, problem is either U370B or bad input from the Horizontal Display DAC, U250. If bad input signals, troubleshoot the Display and Attributes Memory and Display DACs (schematic diagram 16). See "Distorted Display" troubleshooting chart at the back of this section.

6. If the waveform at U170 pin 6 is correct (or U370B pin 7 for the horizontal signal), but not correct at the integrator output, check that the sample switch (U270B) is getting the $\overline{\text{SAMPLE}}$ drive signal. Troubleshoot the Vertical or Horizontal vector generator circuitry.

7. Is display switching correctly for dots, envelope, vector, and readout displays? If not, check multiplexer U290 and select signals (AMP0 and AMP1).

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7 EXTENDED DIAGNOSTICS

If unfamiliar with the use or operation of the extended diagnostics routines of the 2430, the "Calibration and Diagnostics" and information supplied in the "Diagnostics" subsection of this section may prove quite useful.

0000 EXTENDED DIAGNOSTICS

Running extended diagnostics at this level runs all tests. It is equivalent to SELF DIAG in the CAL/DIAG menu. A failed test is indicated by a FAIL label in the main Extended Diagnostics menu. Go to the lower testing levels of a failed test to isolate the failure.

1000 SYS-ROM

System ROM A12U670, A12U680, A12U682, A12U690, and A12U692 (schematic diagram 1):

Testing Method:

Ran from this level, all ROM tests are selected in turn, or an individual test may be called by selecting test numbers 1100 through 1900.

These tests compute the cyclic redundant word for the contents of the ROM. The resulting value is compared to the stored value of the first word of the ROM (the previously computed CRCC). A correct match indicates a good ROM.

If marked FAIL in the main Extended Diagnostic menu, go to the next level and run the test to determine the failed ROM or ROMs.

Troubleshooting Procedure:

1. A failed ROM test indicates a defective ROM. Check that the correct ROMs are installed in the correct sockets. Check out the supply voltages and the chip select to a failed ROM to verify them.

2. A failure of most or all paged ROM indicates a paging chip select problem. The last condition is probably not detectable, as the System μP is unable to obtain its operating instructions from the ROM. The System μP Kernel test (given in Procedure 8) may be used to check that the microprocessor is operating and to check the chip-select addressing circuitry for correct operation.

Table 6-6 (cont)

1100 ROM1	Base page ROM, A12U670.
1200 ROM0.0-0	Page 0, lower half of A12U680.
1300 ROM0.1-1	Page 1, lower half of A12U682.
1400 ROM0.2-2	Page 2, lower half of A12U690.
1500 ROM0.3-3	Page 3, lower half of A12U692.
1600 ROM0.0-4	Page 4, upper half of A12U680.
1700 ROM0.1-5	Page 5, upper half of A12U682.
1800 ROM0.2-6	Page 6, upper half of A12U690.
1900 ROM0.3-7	Page 7, upper half of A12U692.
2000 REG	Registers Testing: Testing Method: From this level, all register tests are selected in turn. Individual tests may be executed by selecting test numbers 2100 through 2600. If marked FAIL in the main Extended Diagnostics menu, move the cursor to the 2000 level test and rerun to find next lower failure level in the Registers tests. All register names have the convention of assuming the name given to the schematic-designated chip-select line for that register (i.e., MISC is the name of the chip select on the time base/display board to registers U532 and U540). The register tests are organized by circuit board. Where possible, a set of four bit patterns have been used. The register tests have the capability of testing for stuck bits (both high and low) for each data line as well as testing each data line for interconnecting shorts to other data lines. If all bit patterns of a test fail, check for a defective chip select, a defective IC in the chip-select path, or possibly the part under test is defective. If at least one bit pattern passes, use the "which bit changed" method of isolating which bit(s) have the problem.
2100 PROCESSOR	System μP Register Tests—A12 Circuit Board: Testing Method: The processor board has nine register tests. These are organized from the System μP outward for increasing confidence. One should always check multiple failures from top to bottom, investigating each in turn.

Table 6-6 (cont)

2110
DIAG0

Page Control Register (PCREG) A12U860 (schematic diagram 1):

Testing Method:

Sets PCREG (bit D7) = 0 and tests for = 0 (stuck at one). Sets PCREG (bit D7) = 1 and tests for = 1 (stuck at zero). If both tests pass, the result flag is set to PASS; otherwise, it is set to FAIL.

If test = FAIL then look for failure using the following steps:

1. On the test scope, connect CH 1 to J125 pin 15. Select Slope, + (plus); Trigger Source, CH 1; Trigger Level, 1 V; CH 1 and CH 2 input coupling, DC; CH 1 and CH 2 VOLTS/DIV, 2 V. This step provides a positive, TTL-level trigger strobe (or pulse) for validation of the signal being tested while a test is running. The test scope setup will be used in each of the Registers troubleshooting procedures.

Now using CH2 probe:

2. Run test 2110 in CONTINUOUS mode and check for clock activity at U860 pin 11 (clocks on LO-to-HI transition close to the end of the trigger strobe pulse); if not, troubleshoot its clocking circuitry (U884, U862, and U866).

3. Check that U860 pin 19 clocks from LO-to-HI and remains HI after the trigger strobe pulse returns to LO. If not, replace U860.

4. Test for a chip select at U854 pins 1 and 19 (LO enables). If not correct, troubleshoot System Address Decode circuitry (U884, U862, and U866).

5. While selected, check that U854 pin 11 is set to the state of U860 pin 19. If DIAG0 failed and the chip selects to U854 and the signal to U854 pin 11 are ok, then U854 is probably defective.

2120
DCOK U654

Interrupt Register A12U654 (schematic diagram 1) and DCOK logic circuitry A16U395 and associated components (schematic diagram 23):

Testing Method:

The power supply sends a TTL signal to the interrupt register to inform the System μP of the logic AND of the power supply voltages. DCOK tests INTREG (bit 7). If = 1, the test result = PASS; otherwise, the result = FAIL.

Troubleshooting Procedure:

If test = FAIL then look for failure using the following steps:

1. Set up the test scope as per Step 1 of the 2110 troubleshooting procedure.

Now using CH2 probe:

2. Run test 2120 in CONTINUOUS MODE and check for $\overline{\text{INTREG}}$ chip select on pins 1 and 19 of Interrupt Register U654. If not present, troubleshoot the System Address Decoding circuitry (U884, U862, U866A, U870B, and associated components) for proper inputs and outputs.

3. While the test is running, test U654 pin 17 for steady-state HI value. If HI and DCOK fails, then replace U654. If LO, then check the power supply voltages and the DCOK AND circuit. If supply voltages are not correct, troubleshoot the low-voltage power supply and regulators; if voltages are correct, troubleshoot A16U395 and associated components (schematic diagram 23).

Table 6-6 (cont)

2130 BUSTAKE	Page Control Register A12U860 (schematic diagram 1), OR-gate A12U332D (schematic diagram 2), and Interrupt Register A12U654: Testing Method: To test for stuck at 1, PCREG U860 is written the pattern x00xxxxx to clear BUS REQUEST and BUSTAKE bits. Then INTREG (bit 6) is tested for = 0, and the PASS/FAIL results are set accordingly. The PCREG is set for a BUSTAKE (x1xxxxxx). This time the INTREG (bit 6) should = 1. The result is set to FAIL if the test fails. Troubleshooting Procedure: If test = FAIL then look for failure using the following steps: 1. Set up the test scope as per Step 1 of the 2110 troubleshooting procedure. Now using the CH 2 probe: 2. Run test 2130 in CONTINUOUS MODE and check for INTREG chip select at U654 pin 1 and 19. If not present, troubleshoot the System Address Decoding circuitry (U884, U862, U866A, U870B, and associated components) for proper inputs and outputs. 3. Check that BUSTAKE on PCREG U860 pin 16 has LO-to-HI and HI-to-LO transitions on alternate PCREG chip selects. If not, suspect problem with U860. 4. Check INTREG U654 pin 15 for a LO-to-HI transition when BUSTAKE on PCREG U860 pin 16 is set from LO-to-HI; if not, then check U332D (schematic diagram 2) for correct gating.
2140 DIAG1	Processor Miscellaneous Out and Processor Miscellaneous In Registers (A12U750 and A12U854) Diagnostic Bit 1 (schematic diagram 1): Testing Method: This is the first test for the PMISCOUT and PMISCIN registers. The byte to PMISCOUT U760 is set to 00000000 and PMISCIN (bit 4) is tested for = 0. The test result flag is set PASS or FAIL. PMISCOUT is then set to 10000000 and PMISCIN (bit 4) is again tested. If the test fails, the test result is set to FAIL. Troubleshooting Procedure: If test = FAIL then look for failure using the following steps: 1. Set up the test scope as per Step 1 of the 2110 troubleshooting procedure. Now using the CH 2 probe: 2. Run test 2140 in CONTINUOUS MODE and check for chip select at U760 pin 11. If not present, troubleshoot the System Address Decoding circuitry (U884, U862, U866A, U870B, and associated components) for proper inputs and outputs. 3. Test U760 pin 19 for a LO-to-HI transition between chip selects. If missing, replace U760; if ok, suspect U854.

Table 6-6 (cont)

2150
COMREG

Interrupt Latch (COMREG) A12U550 and Display Status Register (SSREG) A12U542 (schematic diagram 2):

Testing Method:

A BUSTAKE is executed (previously tested) and the 4Q output of U550 (pin 15) is set LO. SSREG U542 bits 0 and 1 (pins 16 and 18) are then tested to see if they are LO, and the test results are set accordingly.

NOTE

The inputs of U542 (pins 2 and 4) are wired together.

Pin 15 of U550 is then set HI and SSREG bits 0 and 1 are tested for HI. If the test fails, the test result is set to FAIL.

Troubleshooting Procedure:

If test = FAIL then look for failure using the following steps:

1. Set up the test scope as per Step 1 of the 2110 troubleshooting procedure.

Now using CH 2 probe:

2. Run test 2150 in CONTINUOUS mode and check that U550 pin 1 ($\overline{\text{COMREG}}$) is set LO during the period that the clock line ($\overline{\text{WWR}}$) to U550 at pin 9 has a LO-to-HI transition. This may be done by saving the $\overline{\text{COMREG}}$ signal in REF1 and displaying it at the same time as the clock pulse on U550 pin 9 is acquired. If these signals are not coincident, then troubleshoot the cause and correct the problem. See Figure 6-8 for typical register test waveforms.

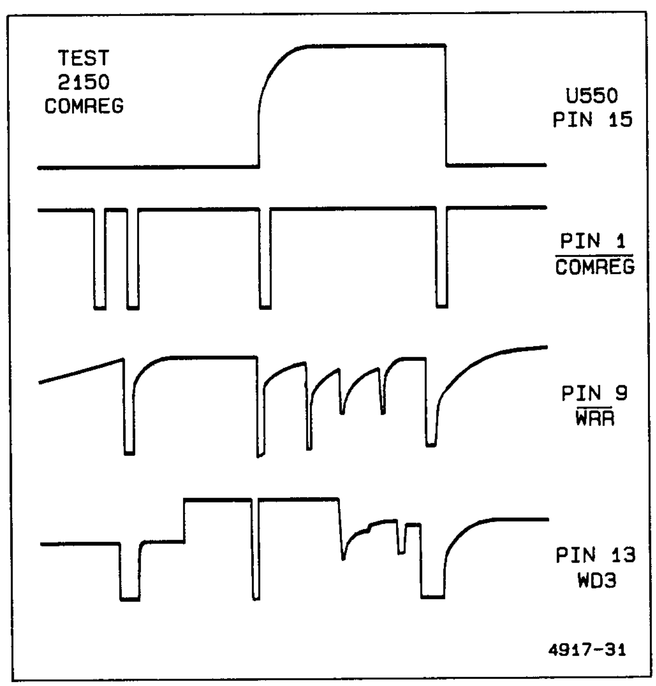


Figure 6-8. Typical Register test waveforms.

Table 6-6 (cont)

3. Check that U550 pin 15 has a LO-to-HI transition after the second clock pulse goes LO-to-HI. If no transition, change U550; if ok, check chip enable of U542 on pin 1 ($\overline{\text{SSREG}}$) to be LO after $\overline{\text{WRR}}$ on U550 pin 9 goes LO-to-HI. If ok, then suspect U550. If the enable is defective, troubleshoot and correct the problem.

2160
WPDN

Waveform μP Done A12U550 (schematic diagram 2):

Testing Method:

A BUSTAKE is executed (previously tested) and pin 10 of Interrupt Latch U550 is set LO. Then pin 14 (bit 2) of PMISCIN register U854 (schematic diagram 1) is tested for a LO, and the test results are set accordingly.

Then pin 10 of U550 is set HI, and U854 pin 14 is tested for a HI. If test fails, the test result is set to FAIL.

Troubleshooting Procedure:

If test = FAIL then look for failure using the following steps:

1. Set up the test scope as per Step 1 of the 2110 troubleshooting procedure.

Now using CH2 probe:

2. Run test 2160 in CONTINUOUS mode and check that U550 pin 1 ($\overline{\text{COMREG}}$) is set LO during the period that the clock to U550 pin 9 ($\overline{\text{WRR}}$) has a LO-to-HI transition. This may be done by saving the $\overline{\text{COMREG}}$ signal in REF1 and displaying while acquiring the clock pulse on U550 pin 9. If these signals are not coincident, then troubleshoot the cause.

3. Check that U550 pin 10 has a HI-to-LO transition on the first enable and a LO-to-HI transition after the second clock pulse goes LO-to-HI. If bad, change U550; if good, check chip enable at U854 pins 1 and 19 is LO after U550 pin 10 goes from LO-to-HI. If ok, then suspect U854. If the enable is defective, troubleshoot and correct the problem.

2170
DIAG2

Diagnostic Bit 2 Word Trigger Register A12U754 (diagram 20):

Testing Method

WDREG U754 pin 19 (DIAG2) is set to 0xxxxxxx and PMISCIN A12U854 pin 5 (bit D6) (schematic diagram 1) is tested for 0. The test result is to PASS or FAIL accordingly.

WDREG U754 pin 19 (DIAG2) is then set to 1xxxxxxx and PMISCIN U854 pin 5 (bit D6) is tested for 1. If the test fails, the test result is set to FAIL.

WDREG also drives the GPIB LEDS on the front panel. Bit patterns xxxxx000 to xxxxx111 are sent in a binary sequence with a 50 ms delay between patterns. The register is then reset to entry values.

Troubleshooting Procedure:

If test = FAIL then look for failure using the following steps:

1. Set up the test scope as per Step 1 of the 2110 troubleshooting procedure.

Table 6-6 (cont)

	Now using CH2 probe: 2. Check that U754 pin 1 $\overline{\text{RESET}}$ is HI. 3. Run test 2170 in CONTINUOUS mode and check the clock line to A12U754 at pin 11 for LO-to-HI transitions. Since this is the register that provides the strobe to WORD TRIG, there should be four clock pulses, one at each end of the trigger strobe and two under it. If not, troubleshoot the clock source to isolate the problem. 4. Test that U754 pin 19 has a LO-to-HI transition on the third strobe. If there is no LO-to-HI transition, replace U754. If there is, then test A12U854 pin 15 for the same signal as at U759 pin 19. If present, replace U854; if not, find the open.
2180 FLD2	Video Option Mode Register A12U750 (schematic diagram 20): Testing Method: TVREG U750 is set = 00000000 and PMISCIN A12U750 pin 3 (schematic diagram 1) is tested for 0. The test result is set accordingly. TVREG U750 pin 2 (bit D0) is then set to 1 and PMISCIN (bit D7) is tested. If the test fails, the test result is set to FAIL. Troubleshooting Procedure: If test = FAIL then look for failure using the following steps: 1. Set up the test scope as per Step 1 of the 2110 troubleshooting procedure. Now using the CH 2 probe: 2. Run test 2180 in CONTINUOUS mode and check the clock line to A12U750 $\overline{\text{TVREG,}}$ pin 11 (schematic diagram 20) for LO-to-HI transitions. There should be two clock pulses under the trigger strobe. If not, troubleshoot the clock source back through Decoder A12U884 (schematic diagram 1) to isolate the problem. 3. Test that U750 pin 2 (FLD2) has a LO-to-HI transition on the second strobe. If there is no LO-to-HI transition, replace U750. If there is, then test U854 pin 17 (schematic diagram 1) for the same signal as at U750 pin 2. If present, replace U854; if not, find the open.
2190 MWPDN	Miscellaneous Register A12U760 (schematic diagram 1): Testing Method: A BUSTAKE is executed (previously tested), Interrupt Latch bit D2 is set true (WPDN) and PMISCOUT Register U760 pin 2 (the mask for WPDN), is set to 0. INTREG U654 pin 18 (bit D0) is tested for 0 and the test result is set accordingly. PMISCOUT U760 pin 2 (bit D0) is set to 1 which should unmask the WPDN that is already set true. INTREG (bit 0) is tested for 1. If test fails, the test result is set to FAIL.

Table 6-6 (cont)

Troubleshooting Procedure:

If test = FAIL then look for failure using the following steps:

1. Set up the test scope as per Step 1 of the 2110 troubleshooting procedure.

Now using the CH 2 probe:

2. Run test 2190 in CONTINUOUS mode and check that A12U550 pin 1 $\overline{\text{COMREG}}$ (schematic diagram 2) is set LO during the period that the clock line U550 pin 9 has a LO-to-HI transition. This may be done by saving the $\overline{\text{COMREG}}$ signal in REF1 (if using a 2430 as the test scope) and displaying it while acquiring the clock pulse on U550 pin 9. If these signals are not coincident, then troubleshoot the cause.
3. Check that U550 pin 2 has a LO-to-HI transition on the second clock pulse. If bad, change U550. If ok, store in REF1 and display it while testing output of A12U880 pin 6 (schematic diagram 1). If ok then replace U654; if not, check the inputs to U880 on pins 4 and 5, and if those are ok, replace U880.

2200
TB-DSP

Display Control Registers (schematic diagram 17):

Testing Method:

Running the test from this level will test all the Display Control registers. These tests will utilize four bit patterns to detect faults. If marked FAIL at this level, go to the lower levels in the menu to test for the failed register. The four bit patterns sent in each of the register tests are as follows:

Test 1—10100101 is sent to the input latch and read back via the output buffer. Test result is set to fail if not a match.

Test 2—01001011 is sent and read back. Test result is set to fail if not a match.

Test 3—10010110 is sent read back. Test result is set to fail if not a match.

Test 4—00101101 is sent and read back. Test result is set to fail if not a match.

NOTE

DISCON (bit 0) will not change, as it has the main board diagnostics as its input.

2210
MISC

Misc Registers A11U532 and A11U540 (schematic diagram 17):

Testing Method:

The MISC register is two components; latch U532 and read-back buffer U540. The test result is set to PASS and the test is done; any failure sets it to FAIL.

If run from this level, all four tests are selected in turn. One may execute any single test by selecting 2211 to 2214. The test involves writing four unique patterns (see test 2200) to U532 and reading them back from U540. The four patterns test for all stuck-at(s) and for lines shorted to other lines. By knowing which test fails and the bit pattern, one may easily determine a bus problem by observing which bits are the same in the failed tests.

Table 6-6 (cont)

	Troubleshooting Procedure: If test = FAIL for all tests, then look for failure using the following steps: 1. Set up the test scope as per Step 1 of the 2110 troubleshooting procedure. Now using the CH 2 probe: 2. Run test 2210 in CONTINUOUS Mode and check U532 pin 1 for $\overline{\text{MISC}}$ to be LO during the time of the trigger strobe. If not, troubleshoot the Register Select circuitry (U550 and U450D) for proper operation. 3. Check U532 pin 19 for clock pulse activity ($\overline{\text{WR}}$ strobe from System μP). 4. If 1 and 2 above are ok, then select a pattern test and check that the data lines are the same states as the pattern; i.e., 10100101 would have the D7 pin = 1, D6 pin = 0, etc. **NOTE** *Must select test mode of RUN ONCE for stability.* If ok, repeat steps 2 and 3 for U540, and replace U540 if steps 2 and 3 pass.
2220 MODECON	Mode Control Register A11U541 and A11U542 (schematic diagram 17): Testing Method: The MODECON register is two components, latch U541 and read-back buffer U542. The test result is set to PASS, any failure sets it to FAIL. If run from this level, all four tests are selected in turn. One may execute any one test by selecting 2221 to 2224. The test involves writing four unique patterns (see test 2200) to U541 and reading them back from U542. The four patterns test for all stuck-at(s) and for lines shorted to other lines. By knowing which test fails and the bit pattern, one may easily determine a bus problem by observing which bits are the same in the failed tests.
	Troubleshooting Procedure: If test = FAIL for all test then look for failure using the following steps: 1. Set up the test scope as per Step 1 of the 2110 troubleshooting procedure. Now using the CH 2 probe: 2. Check U541 pin 1 for PWRUP = HI; if not, troubleshoot Power Up circuitry (schematic diagram 23). 3. Run test 2220 in CONTINUOUS mode and check U541 pin 11 for clock pulse $\overline{\text{MODECON}}$ activity. **NOTE** *First clock pulse is the write to U541, the second is the read from U542.* 4. If 2 and 3 above are ok, then select a pattern test and check that the data lines are the same states as the pattern; i.e., 10100101 would have the D7 pin = 1, D6 pin = 0, etc. If ok, replace U542.

Table 6-6 (cont)

2230
DISCON

Display Control Register A11U530 and A11U531 (schematic diagram 17):

Testing Method:

The DISCON (display control) register is two components, latch U530 and read-back buffer U531. The test result is set to PASS, any failure sets it to FAIL.

If run from this level, all four tests are selected in turn, or one may execute any one test by selecting 2231 to 2234. The test involves writing four unique patterns (see test 2200) to U530 and reading them back from U531. The four patterns test for all stuck-at(s) and for lines shorted to other lines. By knowing which test fails and the bit pattern, one may easily determine a bus problem by observing which bits are the same in the failed tests.

NOTE

The readback bit (bit 0) is the main board diagnostic bit and will not be tested.

Troubleshooting Procedure:

If test = FAIL for all test then look for failure using the following steps:

1. Set up the test scope as per Step 1 of the 2110 troubleshooting procedure.

Using the CH 2 probe:

2. Run test 2230 in CONTINUOUS mode and check U530 pin 1 for $\overline{\text{DISCON}}$ = LO during the time of the trigger strobe. If not, troubleshoot the Register Select circuit (U550 and U450D) for proper operation.
3. Check U530 pin 11 for clock pulse activity ($\overline{\text{WR}}$ strobe from System μP).
4. If 2 and 3 above are ok, then select a pattern test and check that the data lines are the same states as the pattern; i.e., 10100101 would have the D7 pin = 1, D6 pin = 0, etc. If ok, replace U531.

2300
TB-DSP

Display Memory Bus Registers:

Running this test will test all the Display bus registers. There are seven tests in this section. The first two write a pattern to one register and read back from another as in the previous section.

The next three tests deal with the "Q" bus of the display state machine and require strobing of data and shifting of bits for readout.

The remaining two tests use initialized data in U441 and U440 (display and readout memory will be written with our standard four patterns in the first four bites of each memory).

If marked FAIL in the Extended Diagnostic menu, go to the next lower level of diagnostics and run those tests to determine the problem register.

Table 6-6 (cont)

2310
VCURS

Volts Cursors Register A11U241 (schematic diagram 16) Testing Method:

The Volts Cursors Register test checks two components; latch U241 readback is via Diagnostic Buffer U141. The test result is set to PASS, any failure sets it to FAIL.

If run from this level, all four tests are selected in turn, or one may execute any one test by selecting 2311 to 2314. The test involves writing four unique patterns (see test 2200) to U241 and reading them back from U141. The four patterns test for all stuck-at(s) and for lines shorted to other lines. By knowing which test fails and the bit pattern, one may easily determine a bus problem by observing which bits are the same in the failed tests.

Troubleshooting Procedure:

If test = FAIL for all tests then look for failure using the following steps:

1. Check U241 pin 1 to be LO ($\overline{\text{VCURSEN}}$).
2. Check $\overline{\text{VCURS}}$ clock to U241 at pin 11 for activity (save to REF1 and display for timing).
3. Select one pattern and check each output relative to the REF1 clock pulse for the proper level for that bit/pattern. If incorrect, replace U241.
4. Check U141 pins 1 and 19 for the $\overline{\text{YDIAG}}$ pulse after the clock pulse to U241. If ok, replace U141. If not present, replace U550 (schematic diagram 17).

2320
TCURS

Time Cursor Register A11U441 (schematic diagram 16):

Testing Method:

The TCURS test checks two ICs; U441 is a latch and the read back is Diagnostic Buffer U243. The test result is set to PASS, any failure sets it to FAIL.

If run from this level, all four tests are selected in turn, or one may execute any one test by selecting 2321 to 2324. The test involves writing four unique patterns (see test 2200) to U441 and reading them back from U243. The four patterns test for all stuck-at(s) and for lines shorted to other lines. By knowing which test fails and the bit pattern, one may easily determine a bus problem by observing which bits are the same in the failed tests.

Troubleshooting Procedure:

If test = FAIL for all test then look for failure using the following steps:

1. Check U441 pin 1 to be LO ($\overline{\text{TCURSEN}}$).
2. Check U441 pin 11 ($\overline{\text{TCURS}}$) for clock activity (save to REF1 and display for timing).
3. Select one pattern and check each output relative to the REF1 clock pulse for the proper level for that bit/pattern. If incorrect, replace U441.
4. Check U243 pins 1 and 19 for the $\overline{\text{XDIAG}}$ pulse after clock pulse to U441. If ok, replace U243; if not present, replace U550 (schematic diagram 17).

Table 6-6 (cont)

2330
U130

Ramp Buffer A11U130 (schematic diagram 16):

Testing Method:

If run from this level, all four tests are selected in turn, or one may execute any one test by selecting 2331 to 2334.

This test requires the display state machine to be operative. There is no "good" way to ensure that it is functional, and there have been no previous tests to help to find that out. Therefore, if this test fails, it could be for several reasons other than U130. If the power-on Self Test starts to run but halts at test level 3000 or test level 6000 (as indicated by the lighted Trigger LEDs), the problem may be in the Display State Machine circuit (schematic diagram 17) or the DISDN signal path to the System μP Interrupt circuit. Use the Display Troubleshooting Chart to troubleshoot the Display State Machine and check that the DISDN signal at U414 pin 5 is correct.

Initialization:

DISCON = 01100000. Significant bits are b2, b5, b6, and b7 ($\overline{\text{STOPDIS}}$, enable "Q" bus, not ENV mode).

MODECON = 00001000. Significant bit is b3 (U140 lower half).

MISC = 00100000. Significant bit is b5 (ZAXIS OFF).

The test result = PASS.

The test is to load a pattern into the display counters, U220 and U211, with the $\overline{\text{LDCOUNT}}$ strobe (data loaded to U222 is fixed). Their outputs are selected by U221, U212, U210 holding U414A in the reset mode and not PRESTART. Since the $\overline{\text{STOPDIS}}$ line is LO, the display counters are selected as the source to the Q bus (U210, U212, U221). The inputs to U130 are the bits Q1..Q5 where Q1..Q3 = 0. and Q4, Q5 are the b0, b1 data of pattern. To read back properly, shift the pattern left 3 bits and use only the lower 5 bits of XDIAG (U243).

Test 1. 10100101 is loaded and read back via U243. Test result is set to fail if not a match on bits 0 through 5.

Test 2. 01001011 is loaded and read back via U243. Test result is set to fail if not a match on bits 0 through 5.

Test 3. 10010110 is loaded and read back via U243. Test result is set to fail if not a match on bits 0 through 5.

Test 4. 00101101 is loaded and read back via U243. Test result is set to fail if not a match on bits 0 through 5.

Troubleshooting Procedure:

NOTE

Q0 through Q3 = 0. Q4 through Q11 map to D0 through D7; i.e., Q4 = d3. By knowing which test FAILs and the bit pattern one may easily determine the problem bit(s) (look for the bit column in the failed tests that are the same).

If 2 or 3 tests fail, then there is a bus problem of some sort and they must be examined. If all four tests FAIL, then the problem can be in several locations.

Table 6-6 (cont)

1. $\overline{\text{LDCOUNT}}$ might not be strobing the data into Display Counters U220 and/or U211 (schematic diagram 17).
2. U414A may not be resetting, or U323 pin 3 might be HI due to a failure.
3. Address Multiplexers U221, U212, and U210 may not be operating properly.
4. Ramp Buffer U130 (schematic diagram 16) may be defective.

Set up the 2430 test scope as in Step 1 of the 2110 troubleshooting procedure.

Now using the CH 2 probe:

1. Run test 2230 in CONTINUOUS mode and verify the $\overline{\text{LDCOUNT}}$ strobe pulse at pin 11 of U222, U220, and U211.
2. Verify that after $\overline{\text{LDCOUNT}}$ strobe, that the outputs of U222, U220, and U211 are stable and of the correct level for the test selected.
3. Verify that U323 pin 3 is LO.
4. Verify the outputs of U221, U212, and U210 are stable and correct after the $\overline{\text{LDCOUNT}}$ strobe to the previous bus.
5. Verify the chip enable to U130 pins 1 and 15 is LO. If ok to here, replace U130.

2340 U140

Readout Buffer U140 (diagram 16):

Testing Method:

If run from this level, all four tests are selected in turn, or one may execute any one test by selecting 2341 to 2344.

This test requires the display state machine to be operative. There is no "good" way to insure that it is functional and there have been no previous tests. Therefore, if this test fails, it could be for several reasons other than U140.

Initialization:

DISCON = 01100000. Significant bits are b2, b5, b6, and b7 ($\overline{\text{STOPDIS}}$, enable "Q" bus, not ENVELOPE mode).

MODECON = 00001000. Significant bit is b3 (U140 lower half).

MISC = 00100000. Significant bit is b5 (ZAXIS OFF).

The test result = PASS.

The test is to load a pattern into the display counters, U220 and U211, with the $\overline{\text{LDCOUNT}}$ strobe. The counter outputs are switched to the Q bus through U221, U212, U210 by holding U414A in the reset mode (PRESTART + DISPLAY is LO). The inputs to U140 (lower half) are the bits Q6 through Q8 where Q1 through Q3 = 0. Q4 and Q5 are the b0 and b1 data of the pattern. To read back properly, one shifts the pattern left 3 bits and use bits 4, 5, and 6 of XDIAG (U243); the test result is set to FAIL if the test fails.

Table 6-6 (cont)

Test 1. 10100101 is loaded and read back via U243. Test result is set to fail if not a match on bits 0 through 5.

Test 2. 01001011 is loaded and read back via U243. Test result is set to fail if not a match on bits 0 through 5.

Test 3. 10010110 is loaded and read back via U243. Test result is set to fail if not a match on bits 0 through 5.

Test 4. 00101101 is loaded and read back via U243. Test result is set to fail if not a match on bits 0 through 5.

Then MODECON is set to 00010000 to select the top half of U140 and the pattern is shifted left 2 bits. YDIAG (U141) bits 4, 5, 6, and 7 are tested, and the test result is set to FAIL if the test fails.

Test 1. 10100101 is loaded and read back via U141. Test result is set to FAIL if not a match on bits 0 through 5.

Test 2. 01001011 is loaded and read back via U141. Test result is set to FAIL if not a match on bits 0 through 5.

Test 3. 10010110 is loaded and read back via U141. Test result is set to FAIL if not a match on bits 0 through 5.

Test 4. 00101101 is loaded and read back via U141. Test result is set to FAIL if not a match on bits 0 through 5.

NOTE

Q0 through Q4 = 0. Q4 through Q11 map to D0 to D7. i.e., Q7 = D3. By knowing which test FAILs and the bit pattern one may easily determine the problem bit(s) (look for the bit column in the failed tests that are the same).

If 2 or 3 tests fail, then there is a bus problem of some sort, and the busses must be examined. If all four tests FAIL, then the problem can be in several locations.

1. $\overline{\text{LDCOUNT}}$ might not be strobing the data into U220 and/or U211 (Display Counters, schematic diagram 17).
2. Flip-flop U414A may not be resetting, or OR-gate U323 pin 3 might be HI due to a failure.
3. The busses into or out of Address Multiplexers U221, U212, U210 may not be operating properly.
4. Readout Buffer U140 may be defective.

Troubleshooting Procedure:

Set up the 2430 test scope as in Step 1 of the 2110 troubleshooting procedure.

Now using the CH 2 probe:

1. Run test 2340 and verify the $\overline{\text{LDCOUNT}}$ strobe pulse at pin 11 of U222, U220, and U211.
2. Verify that after $\overline{\text{LDCOUNT}}$ strobe, that the outputs of Address Multiplexers U222, U220, U211 are stable and of the correct level for the test selected.

Table 6-6 (cont)

	3. Verify that U323 pin 3 is LO. 4. Verify the outputs of U221, U212, and U210 are stable and correct after the $\overline{\text{LDCOUNT}}$ strobe to the previous bus. 5a. Verify the $\overline{\text{RO}}$ chip enable to U140 pin 1 is HI for about half of the Trigger strobe positive period, and then that it goes LO and stays LO for the remaining time. This LO selects inputs Q6 through Q9 of U140. 5b. Verify the $\overline{\text{COUNTEN}}$ chip enable to U140 pin 19 has a HI-to-LO transition; then, before the time that U140 pin 1 goes LO, U140 pin 19 goes HI. While U140 pin 19 is LO, inputs Q6, Q7, Q8 are selected. If ok to here, replace U140.
2350 U240	Readout Buffer U240 (diagram 16): Testing Method: If run from this level, all four tests are selected in turn, or one may execute any one test by selecting 2351 to 2354. This test requires the display state machine to be operative. There is no "good" way to insure that it is functional, and there have been no previous tests to help find that out. Therefore, if this test fails, it could be for several reasons other than U240. Initialization: DISCON = 01100000. Significant bits are b2, b5, b6, and b7 ($\overline{\text{STOPDIS}}$, enable "Q" bus, not ENV mode). MODECON = 00010000. Significant bit is b3 (U240). MISC = 00100000. Significant bit is b5 (ZAXIS OFF). The test result = PASS. The test is to load a pattern into the display counters, U220 and U211, with the $\overline{\text{LDCOUNT}}$ strobe. The counter outputs are switched to the Q bus through U221, U212, U210 by holding U414A in the reset mode (PRESTART + DISPLAY is LO). The inputs to U240 are the bits Q0 through Q5 where Q0 through Q3 = 0. Q4 and Q5 are the b0, b1 data of pattern. To read back properly, one shifts the pattern left 6 bits and uses bits 6 and 7 of XDIAG (U243); the test result is set to FAIL if the test fails. Test 1. 10100101 is loaded and read back via U243. Test result is set to fail if not a match on bits 0 through 5. Test 2. 01001011 is loaded and read back via U243. Test result is set to fail if not a match on bits 0 through 5. Test 3. 10010110 is loaded and read back via U243. Test result is set to fail if not a match on bits 0 through 5. Test 4. 00101101 is loaded and read back via U243. Test result is set to FAIL if not a match on bits 0 through 5.

Table 6-6 (cont)

NOTE

Q0 through Q3 = 0, and Q4 through Q11 map to D0 to D7. i.e., Q7 = D3. By knowing which test FAILs and the bit pattern, one may easily determine the problem bit(s) (look for the bit column in the failed tests that are the same).

If 2 or 3 tests fail, then there is a bus problem of some sort that must be examined. If all four tests FAIL, then the problem can be in several locations.

1. $\overline{\text{LDCOUNT}}$ might not be strobing the data into U220 and/or U211.
2. Flip-flop U414A may not be resetting, or U323 pin 3 might be HI due to a failure.
3. Address Multiplexers U221, U212, and U210 may not be operating properly.
4. Readout Buffer U240 may be defective.

Troubleshooting Procedure:

Set up the 2430 test scope as in Step 1 of the 2110 troubleshooting procedure.

Now using the CH 2 probe:

1. Run test 2350 in CONTINUOUS mode and verify the $\overline{\text{LDCOUNT}}$ strobe pulse at pin 11 of U222, U220, and U211.
2. Verify that after $\overline{\text{LDCOUNT}}$ strobe, the outputs of Address Multiplexers U222, U220, U211 are stable and of the correct level for the test selected.
3. Verify that U323A pin 3 is LO.
4. Verify the outputs of U221, U212, and U210 are stable and correct after the $\overline{\text{LDCOUNT}}$ strobe to the previous bus.
5. Verify the $\overline{\text{RO}}$ chip enable to U240 pins 1 and 15 is LO. If ok to here, replace U240.

2360
U322

Vertical Buffer U322 (diagram 16):

Testing Method:

If run from this level, all four tests are selected in turn, or one may execute any one test by selecting 2361 to 2364. The contents of the first four bytes of U322 have been written and will now be tested against the values that were thought to be written, any failure to match will cause that test to fail. U322 is decoded by reading address 2000h.

Set test result = PASS.

If contents of 2000h not equal to 10100101, then test result = FAIL.

If contents of 2001h not equal to 01001011, then test result = FAIL.

If contents of 2002h not equal to 10010110, then test result = FAIL.

If contents of 2003h not equal to 00101101, then test result = FAIL.

Table 6-6 (cont)

Troubleshooting Procedure:

Set up the 2430 test scope as in Step 1 of the 2110 troubleshooting procedure.

Using the CH 2 probe:

1. Run test 2360 in CONTINUOUS mode and check U322 pin 19 for a negative strobe $\overline{\text{YSEL}}$ at 10 μs from the LO-to-HI transition of the trigger pulse. If not present, troubleshoot U323 and the inputs to it.
2. Check for activity on the $\overline{\text{WRD}}$ signal line of U322 (pin 1); if no activity, check for open back to A12U564 (schematic diagram 2).
3. Check that the data pattern for the test is correct at the input and output pins of U322. The data is stable during the $\overline{\text{YSEL}}$ strobe on pin 19, and the data bit level must be read in coincidence with it as other activity is also taking place on the WD bus. A Word Recognizer probe would be useful to make these checks, but it is not necessary.
4. If the input and output data patterns of U322 do not match, replace U322. If they match each other, but are not correct, suspect a problem with Vertical RAM U431. Run test 2361 through test 2364 to see if all patterns fail. If all do not fail, troubleshoot for a bad bit of the failing test or tests.
5. Check pin 20 $\overline{\text{(DEY)}}$ and pin 18 $\overline{\text{(CSY)}}$ of U431 for a negative strobe coincident with the $\overline{\text{YSEL}}$ strobe. If either is not present, troubleshoot U421 and the input signals to it.
6. Check that pin 21 of U431 $\overline{\text{(WE)}}$ is HI during the HI portion of the trigger strobe (displayed on CH 1 of the test scope). The data writes of the test patterns occur during the LO portion of the trigger strobe, and that activity can be seen. If the $\overline{\text{WE}}$ signal is not correct, troubleshoot U422 and the input signals to it.
7. Replace U431.

2370
U314

Horizontal Buffer (diagram 16):

Testing Method:

If run from this level, all four tests are selected in turn, or one may execute any one test by selecting 2371 to 2374. The contents of the first four bytes of U314 have been written and will now be tested against the values that were thought to be written, any failure to match will cause that test to fail. U314 is decoded by reading address 2800h.

Set test result = PASS.

If contents of 2800h not equal to 10100101, then test result = FAIL.

If contents of 2801h not equal to 01001011, then test result = FAIL.

If contents of 2802h not equal to 10010110, then test result = FAIL.

If contents of 2803h not equal to 00101101, then test result = FAIL.

Troubleshooting Procedure:

Set up the 2430 test scope as in Step 1 of the 2110 troubleshooting procedure.

Table 6-6 (cont)

Using the CH 2 probe:

1. Run test 2370 in CONTINUOUS mode and check U314 pin 19 for a negative strobe $\overline{XSEL}$ at 10 μs from the LO-to-HI transition of the trigger pulse. If not present, troubleshoot U323 and the inputs to it.
2. Check for activity on the $\overline{WRD}$ signal line of U314 (pin 1); if no activity, check for open back to A12U564 (schematic diagram 2).
3. Check that the data pattern for the test is correct at the input and output pins of U314. The data is stable during the $\overline{XSEL}$ strobe on pin 19, and the data bit level must be read in coincidence with it, as other activity is also taking place on the WD bus.
4. If the input and output data patterns of U314 do not match, replace U314. If they match each other, but are not correct, suspect a problem with Horizontal RAM U431. Run test 2371 through test 2374 to see if all patterns fail. If all do not fail, troubleshoot for a bad bit of the failing test or tests. A Word Recognizer probe would be useful for making these checks but is not necessary.
5. Check pin 20 ($\overline{DEX}$) and pin 18 ($\overline{CSX}$) of U440 for a negative strobe coincident with the $\overline{XSEL}$ strobe. If either is not present, troubleshoot U421 and the input signals to it.
6. Check that pin 21 of U440 ($\overline{WE}$) is HI during the HI portion of the trigger strobe (displayed on CH 1 of the test scope). The data writes of the test patterns occur during the LO portion of the trigger strobe, and that activity can be seen. If the $\overline{WE}$ signal is not correct, troubleshoot U422 and the input signals to it.
7. Replace U440.

2400 TB-DSP

Running the test at this level will execute the Time Base Controller (U670) tests for Short-Pipe (SISO) and FISO modes.

The test causes Time Base Controller U670 to simulate all the necessary states to get an acquisition in Short-Pipe and FISO modes.

2410 U670 FISO

Time Base Controller A11U670 (schematic diagram 8):

Running the test executes the Time Base Controller in FISO mode.

Troubleshooting Procedure:

Set up the 2430 test scope as in Step 1 of the 2110 troubleshooting procedure.

Now using the CH 2 probe:

1. Run test 2410 in the CONTINUOUS mode. Set the Sec/Div setting of the test scope to 1 μs and connect the CH 2 probe to pin 19 of bidirectional buffer U641 ($\overline{TBSEL}$); save CH 2 into REF1 and Display REF1.
2. Position CH 2 down to allow room and connect the CH 2 probe to U641 pin 1; save CH 2 into REF2 and Display REF2. The LO $\overline{TBSEL}$ pulse should be coincident to a HI $\overline{RD}$ pulse; if not, then troubleshoot the $\overline{TBSEL}$ or the $\overline{RD}$ signal line.

Table 6-6 (cont)

	3. Position CH 2 down to allow room to display the signal and probe U641 pin 11 through 18. While the REF1 signal $\overline{TBSEL}$ is LO and REF2 signal $\overline{RD}$ is HI, compare the results to 01100101 where U641 pin 11 is D7 and U641 pin 18 is D0. If they do not compare, replace U641. 4. Test the output of U670 pin 26 for a square wave with a period of about 200 μs. If not correct, replace U670. 5. If present, test for the square wave at U680 pin 16; replace U680 if TIMER signal is missing. 6. If all checks were ok, suspect A12U542 (schematic diagram 2).
2420 U670 SISO	Time Base Controller A11U670 (schematic diagram 8): Troubleshooting Procedure: Set up the 2430 test scope as in Step 1 of the 2110 troubleshooting procedure and run test 2420 in the CONTINUOUS mode on the 2430 under test. Now using the CH 2 probe: 1. Position the trigger strobe (CH1) near the top of the crt and connect the CH 2 probe to pin 19, $\overline{TBSEL}$, of U641. Adjust the Sec/Div setting of the test scope to 1 μs. Verify that there is a negative $\overline{TBSEL}$ pulse during the positive trigger strobe. Save the CH 2 waveform in REF1 and display REF1. 2. Position the CH 2 display down to allow room and connect the CH 2 probe to U641 pin 1. Save CH 2 into REF2 and display REF2. The $\overline{TBSEL}$ pulse should be coincident to a HI $\overline{RD}$ pulse; if not, then troubleshoot the chip select or $\overline{RD}$ signal line. 3. Position the CH 2 display down to allow room and probe U641 pin 11 through 18 while REF1 signal is LO and REF2 signal is HI. Compare the results to 01000000 where U641 pin 11 is D7 and U641 pin 18 is D0. If they do not compare, replace U641. 4. Test the output of U670 at pin 26 for a square wave signal (TIMER) with a period of about 200 μs; if not present, replace U670. 5. If present, test for the square wave at U680 pin 16 and replace U680 if missing. 6. If all checks were ok, suspect A12U542 (schematic diagram 2).
2500 MAIN	The MAIN board has five shift-register tests. These are in two groups. The first group includes Gate Array U270, Peak-Detector U530, Attenuators U511 and U221 (acting as one 16-bit register), Trig U140. The second group has the System-DAC U850 and U851 (acting as one 16-bit register). From this level, the initialization and all five tests are selected in turn. An individual test may be run by selecting test numbers 2510 to 2560. There is one diagnostic bit for readout off the main board and that is the logic-AND of the MSB of all the shift registers. The shift registers are preset to 10100101, or 1010010110100101 and the diagnostic bit is tested to see if a "1" is being read out for the MSB. If the diagnostic bit is not = 1, then either one of the registers is not loading or the diagnostic bit is stuck. In any event, no further meaningful data is possible, so the test stops. If initialization is successful, each bit is shifted out, register by register, and compared against what it should be by shifting the initial pattern and comparing the MSB. After any register is tested, it is reinitialized so the next register may be tested. Discon (input = U531 pin 18, output = U531 pin 17) is the diagnostic bit from the main board.

Table 6-6 (cont)

2510 INIT SHIFT REGS	Acquisition Control Shift Registers A10U270 (Gate Array), A10U530 (Peak Detector), A10U140 (Trig Control), DAC Input Shift Register A10U850/U851 (schematic diagram 5), and Attenuator Shift Register A10U221/U511 (schematic diagram 9): Testing Method: For this test to pass, the MSB of the five output registers above must be high. If one of the registers didn't have the correct pattern strobed in, the test fails. Troubleshooting Procedure: Set up the 2430 test scope as in Step 1 of the 2110 troubleshooting procedure. Run test 2510 in CONTINUOUS mode. Using the CH 2 probe: 1. Check A10U380 pin 3 (schematic diagram 5) for a HI level during the HI period of the trigger strobe. If ok, then check for the same signal at A11U531 pin 18 (schematic diagram 17). If correct and test is failing, replace U531 and run SELF DIAG. 2. Check U380 pins 1 and 2. If both are HI during the trigger strobe HI and pin 3 does not follow, then replace U380. If neither pin 1 nor 2 is HI, then suspect DAC Select Multiplexer U272 or its input gating. 3. If U380 pin 2 is LO, then run test 2560 and troubleshoot using the procedure given for that number. 4. If U380A pin 1 is LO, then find which cathode of the input diodes (CR185, CR186, CR286, or CR287) is LO. Run the test number for the suspected Shift Register and check the inputs (clocks, data, and power) to it (look at the information given with the test number for the troubleshooting procedure for each Shift Register). If they are all ok, replace the suspected Shift Register; if not, troubleshoot the bad input.
2520 ATTEN	Attenuator Shift Registers A10U221/A10U511 (schematic diagram 9): Testing Method: For this test, the MSB of A10U511 (pin 13) will be compared with what the MSB should be with each shift of the register. If one of the bits differs from the loaded-in pattern, the test fails. Troubleshooting Procedure: Set up the 2430 test scope as in Step 1 of the 2110 troubleshooting procedure. **NOTE** *For the following, set the Trigger Position of the test 2430 to 3/4. If using an analog scope for testing, use the appropriate holdoff and trigger level to view the signals of interest.* Run test 2520 in CONTINUOUS mode. Using the CH 2 probe: 1. Check U511 pin 9 and U221 pin 9 for +5 V (registers not held reset). If not +5 V, then repair. 2. Check Shift Register U221 at pin 8 for activity (ATT SR CLOCK line). If clock is missing, troubleshoot Control Register Clock Decoder A10U271 (diagram 5).

Table 6-6 (cont)

	3. Check U221 pins 1 and 2 for activity (ACD line is the data input). If ACD missing, troubleshoot the signal path to and gating on the inputs of DAC Multiplexer Select register U272 (diagram 5). 4. Check U221 pin 13 for activity; replace U221 if inactive. 5. If checks good to this point and the test still fails, replace U511.
2530 PEAK DETECTOR	Acquisition Control Register A10U530 (schematic diagram 5): Testing Method: For this test, the MSB of A10U530 (pin 13) will be compared with what the MSB should be with each shift of the register. If one of the bits differs from the loaded-in pattern, the test fails.
	Troubleshooting Procedure: Set up the 2430 test scope as in Step 1 of the 2110 troubleshooting procedure. **NOTE** *For the following, set the Trigger Position of the test 2430 to 3/4. If using an analog scope for testing, use the appropriate holdoff and trigger level to view the signals of interest.* Run test 2530 in CONTINUOUS mode. Using the CH 2 probe: 1. Check U530 pin 9 for a HI level. If LO, then check R531 and source of +5 V. 2. Check U530 pin 8 for activity (PD SR CLK signal line); if inactive, repair. 3. Check U530 pins 1 and 2 for activity (ACD line is the data input). Repair if inactive. 4. If all inputs are good, replace U530.
2540 GATE ARRAY	Acquisition Control Register A10U270 (schematic diagram 5): Testing Method: For this test, the MSB of U270 (pin 13) will be compared with what the MSB should be with each shift of the register. If one of the bits differs from the loaded-in pattern, the test fails.
	Troubleshooting Procedure: Set up the 2430 test scope as in Step 1 of the 2110 troubleshooting procedure. **NOTE** *For the following, set the Trigger Position of the test 2430 to 3/4. If using an analog scope for testing, use the appropriate holdoff and trigger level to view the signals of interest.* Run test 2540 in CONTINUOUS mode. Using the CH 2 probe: 1. Check U270 pin 9 for a HI level. If not +5 V, check R269 and source of the +5 V. 2. Check U270 pin 8 for activity (GA SR CLK signal line); if inactive, repair. 3. Check U270 pins 1 and 2 for activity (ACD line is the data input). Repair if inactive. 4. If all inputs are good, replace U270.

Table 6-6 (cont)

2550 TRIG	Acquisition Control Register A10U140 (schematic diagram 5): Testing Method: For this test, the MSB of A10U140 (pin 13) will be compared with what the MSB should be with each shift of the register. If one of the bits differs from the loaded-in pattern, the test fails.
	Troubleshooting Procedure: Set up the 2430 test scope as in Step 1 of the 2110 troubleshooting procedure. **NOTE** *For the following, set the Trigger Position of the test 2430 to 3/4. If using an analog scope for testing, use the appropriate holdoff and trigger level to view the signals of interest.* Run test 2550 in CONTINUOUS mode. Using the CH 2 probe: 1. Check U140 pin 9 for a HI level ($\overline{\text{RESET}}$). If LO, repair. 2. Check U140 pin 8 for activity (TRIG CONT CLK line). If inactive, repair. 3. Check U140 pins 1 and 2 for activity (ACD line is the data input); repair if inactive. 4. If all inputs are good, replace U140.
2560 SYSTEM DAC	DAC Input Shift Registers A10U850/A10U851 (schematic diagram 5): Testing Method: For this test, the MSB of A10U851 (pin 13) will be compared with what the MSB should be with each shift of the register. If one of the bits differs from the loaded-in pattern, the test fails.
	Troubleshooting Procedure: Set up the 2430 test scope as in Step 1 of the 2110 troubleshooting procedure. **NOTE** *For the following, set the Trigger Position of the test 2430 to 3/4. If using an analog scope for testing, use the appropriate holdoff and trigger level to view the signals of interest.* Run test 2560 in the CONTINUOUS mode. Using the CH 2 probe: 1. Check U850 pin 9 and U851 pin 9 for HI level. If not +5 V, check R850 and source of the +5 V. 2. Check U850 pin 8 and U851 pin 8 for clock activity. If clocks are inactive, then: a. Check U280B pin 5 to have a LO gate present; replace U272 if pin 5 is stuck either HI or LO. b. Check U280B pin 6 for clocking signals during the HI period of the trigger strobe. c. Replace U280 if not gating correctly; troubleshoot clock signals if not present. 3. Check the data input to U850 at pins 1 and 2. The signal should be a train of pulses during the HI period of the trigger strobe. If the data input signal is not present, test signals around U280D and correct.

Table 6-6 (cont)

	4. Check U850 pin 13 that the first 8-bits of the 16-bit pattern comes out as the second is shifted into U850 at pins 1 and 2. (A Sec/Div setting of 0.5 ms on the test scope is good for viewing the data pattern, and the latched data on pin 13 is much easier to view than the input data pulses). If the data is not shifting through U850, then replace U850. 5. If the data is coming through U850, check U851 pins 1 and 2 to verify that it is ok there. Check pin 13 of U851 for a data pattern of 1010010110100101. (Each bit is approximately 0.2 ms wide, so a 0.4 ms wide pulse is two bits.) 6. Replace U851 if not shifting the signal through.
2600 SIDE U761/U762	Holdoff Register A11U762 (schematic diagram 13): Testing Method: From this level, all four tests are selected in turn. Individual test may be called by selecting test numbers 2610 to 2640. The test involves writing 4 unique patterns to U762 and reading them back from U761. The four patterns test for all stuck-at(s) and for lines shorted to other lines. By knowing which test FAILs and the bit pattern, one may easily determine a bus problem by observing which bits are the same in the failed tests. The HOREG register is two integrated circuits; U762 is a latch and the read back is U761. If all tests pass, the test result is set to PASS; any failure sets it to FAIL. **NOTE** *Bit 3 of the test patterns is not allowed to be set LO as it would reset the GPIB chip and we cannot restart it from the diagnostic routines.* Test 1. 10101101 is sent to U762 and read back via U761. Test result is set to FAIL if not a match. Test 2. 01001011 is sent to U762 and read back via U761. Test result is set to FAIL if not a match. Test 3. 10011110 is sent to U762 and read back via U761. Test result is set to FAIL if not a match. Test 4. 00101101 is sent to U762 and read back via U761. Test result is set to FAIL if not a match.
	Troubleshooting Procedure: If the failure occurs for all tests: Set up the 2430 test scope as in Step 1 of the 2110 troubleshooting procedure. Now using CH2 probe: 1. Check that U762 pin 1 $\overline{\text{HOREG}}$ is LO about 12 μs after the trigger strobe. If $\overline{\text{HOREG}}$ is absent, test the inputs of U781. Replace U781 if the inputs are ok; if not ok, troubleshoot that problem. 2. Check that U762 pin 9 ($\overline{\text{WR}}$ clock) has a LO-to-HI transition during the enable time. (Save enable in REF1 and display it while looking at the clock.) Clock line is the write line; if missing, suspect open run or connection. 3. Check the outputs U762 (pins 15, 12, 10, 7, and 5) for the proper levels for the pattern that is being looped on. Replace U762 if incorrect. 4. Check U761 pin 1 to be enabled after the clock to U762 pin 9. If present, then the problem is possibly U762.

Table 6-6 (cont)

3000 SYS-RAM	All RAM tests are non-destructive. The first RAM tested is the Display RAM. It is then used, if good, as a storage location for the contents of the other RAMs while they are being tested. The contents are returned after the test is completed. From this level, all nine RAMs are selected in turn. An individual RAM test may be run by selecting test numbers 3100 to 3900. 3100 DISPLAY (VERTICAL) — 2K — U431 3200 READOUT (HORIZONTAL) — 2K — U440 3300 MAIN (SYSTEM) — 2K — U668 3400 SAVE — 2K — U350 3500 ATTRIBUTE — 4K × 1 — U430 3600 ACQUIRE — 2K — U600 3700 CMD/TEMP — 2K — U440 3800 COEFF — 2K — U432 3900 NV (NONVOLATILE) — 2K — U664 The RAM test is in four parts: One shifted left through a field of zeros with incrementing address. One shifted right through a field of zeros with decrementing address. Zero shifted left through a field of ones with incrementing address. Zero shifted right through a field of ones with decrementing address. The four tests may be executed from this level (3000) or from any of the nine sublevels (3100 through 3900), or any individual test may be executed by entering test number 3x10 through 3x40 (x = 1 through 9).
3100 A11U431	DISPLAY (VERTICAL) RAM A11U431 (schematic diagram 16): Troubleshooting Procedure: If test = FAIL then look for failure and correct using the following steps: Using the CH 1 probe: 1. Run test 3110 in CONTINUOUS mode and check for activity on the chip select line to U431 ($\overline{CSY}$, pin 18). If active, trigger the test scope on the signal. If no chip select, work backwards and find problem. Using the CH 2 probe: 2. Check for activity on the write enable line to U431 ($\overline{WE}$, pin 21) and note that it is LO at the same time as the chip select line. If no signal present, work backwards and find the problem. 3. Check for activity on the output enable line to U431 ($\overline{DEY}$, pin 20). If none, work backwards and find the problem. 4. Check the data I/O pins of U431 (pins 9, 10, 11, 13, 14, 15, 16, and 17) for activity when test 3100 is selected. If no activity when $\overline{DEY}$ (output enable) is LO (pin stuck HI or LO), then suspect U322; otherwise suspect U431.

Table 6-6 (cont)

3200
A11U440

READOUT (HORIZONTAL) RAM A11U440 (schematic diagram 16):

Troubleshooting Procedure:

If test = FAIL then look for failure and correct using the following steps:

Run test 3210 in CONTINUOUS mode.

Using the CH 1 probe:

1. Check for activity on the chip select line U440 ($\overline{CSX}$, pin 18, and trigger the scope on the CH 1 signal. If none, work backwards and find problem.

Using the CH 2 probe:

2. Check for activity on the write enable line U440 pin 21, and note that it is LO at the same time as the chip select line. If none, work backwards and find the problem.
3. Check for activity on the output enable line U440 pin 20. If none, work backwards and find the problem.
4. Check the data I/O pins U440 (pin 9, 10, 11, 13, 14, 15, 16, and 17) for activity when test 3210 is selected. If no activity (stuck HI or LO) when output enable is LO, then suspect U314; otherwise suspect U440.

3300
A12U668

MAIN (SYSTEM) RAM A12U668:

If the System RAM data bus, chip selects, or output enable lines are defective, the processor system will not function and the Kernel tests will need to be executed to isolate the problem. Therefore if the RAM test fails, the most likely problem is U668. See Procedure 8 for the Kernel test.

3400
A12U350

SAVE RAM A12U350 (schematic diagram 2):

Troubleshooting Procedure:

If test = FAIL then look for failure and correct, using the following steps:

Select test 3410 and RUN CONTINUOUSLY.

Using the CH 1 probe:

1. Check for activity on the pin 20 chip select line to U350, and trigger the scope on the signal if active. If no chip select, work backwards through the chip select circuitry and find problem.
2. Check for activity on the write enable line to U350 ($\overline{WRR}$, pin 27) and note that it is LO at the same time as the chip select line. If no activity, work backwards and find the problem.
3. Check for activity on the output enable line to U350 ($\overline{WRD}$, pin 22). If no activity, work backwards and find the problem.
4. Check the data I/O pins U350 (pins 9, 10, 11, 13, 14, 15, 16, and 17) for activity when test 3400 is selected. If no activity (stuck HI or LO) when output enable is LO, then suspect buffer U352; otherwise suspect U350.

Table 6-6 (cont)

3500 A11U430	ATTRIBUTE RAM A11U430 (schematic diagram 16): Troubleshooting Procedure: If test = FAIL then look for failure and correct using the following steps: Run test 3510 in CONTINUOUS mode. Using CH 1 probe: 1. Check the write enable to U430 ($\overline{WRA}$, pin 8) for activity and trigger on the signal if active. If no activity, troubleshoot OR-gate U422A and U422C and their input signals. Check that pin 10 is LO; if not, repair. Using the CH 2 probe: 2. Check for activity at the data input to U430 (DI, pin 11) timed with the enable pulse. If no signal, suspect U423A or U422B. 3. If the checks in Steps 1 and 2 are ok, replace U430.
3600 A11U600	ACQUIRE RAM A11U600 (schematic diagram 8): Troubleshooting Procedure: If test = FAIL then look for failure and correct, using the following steps: Run test 3610 in CONTINUOUS mode. 1. Check for LO on chip select line U600 pin 18. Repair if not LO. 2. Check for activity on the write enable line to U600 ($\overline{WE}$, pin 21). If no activity, work backwards and find the problem. 3. Check for activity on the output enable line to U600 ($\overline{OE}$, pin 20). If no activity, work backwards and find the problem. 4. Check the data I/O pins of U600 (pins 9, 10, 11, 13, 14, 15, 16, and 17) for activity when test 3600 is selected. If no activity (stuck HI or LO) when the output enable is LO, then suspect buffer U610; otherwise suspect U600. 5. Check the address lines (MA0-MAA) for activity. If no activity on any lines, troubleshoot the $\overline{WE}$ and TB2MEM signals to U300, U400, and U410. If an address line is stuck, troubleshoot that problem.
3700 A12U440	CMD/TMP RAM A12U440 (schematic diagram 2): **NOTE** *If tests 3400 through 3700 and 3800 all fail, the most likely faults are: a stuck data line to A12U352, a bad select signal to A12U352, or Waveform Data Buffer A12U352 itself.*

Table 6-6 (cont)

Troubleshooting Procedure:

If test = FAIL then look for failure and correct, using the following steps:

Run test 3710 in the CONTINUOUS mode.

Using the CH 1 probe:

1. Check for activity on the chip select line to A12U440 (pin 18), and trigger the scope on the signal if active. If no activity, work backwards through U250C and find the problem.

Using the CH 2 probe:

2. Check for activity on the write enable line of U440 ($\overline{WRR}$, pin 21), and note that it is LO at the same time as the chip select line. If no activity, work backwards through U542B and find the problem.
3. Check for activity on the output enable line of U440 ($\overline{WRD}$, pin 20). If not being enabled, work backwards through U542B to find the problem.
4. Check the data I/O pins of U440 (pins 9, 10, 11, 13, 14, 15, 16, and 17) for activity. If no activity when output enable is LO, then suspect U352; otherwise check U440.

3800
A12U432

COEFFICIENT RAM A12U432 (schematic diagram 2):

NOTE

If tests 3400, 3700, and 3800 all fail, the most likely faults are: a stuck data line to Waveform Data Buffer A12U352, a bad select signal to A12U352, or Buffer A12U352 itself.

Troubleshooting Procedure:

If test = FAIL then look for failure and correct, using the following steps:

Run test 3810 in CONTINUOUS mode.

Using the CH 1 probe:

1. Check for activity on the chip select line of U432 (pin 18), and trigger the scope on the signal if active. If no activity, work backwards through U250D and find the problem.

Using the CH 2 probe:

2. Check for activity on the write enable line of U432 ($\overline{WRR}$, pin 21), and note that it is LO at the same time as the chip select signal. If no activity, work backwards through U542B and find the problem.
3. Check for activity on the output enable line of U432 ($\overline{WRD}$, pin 20). If not active, work backwards through U542B and find the problem.
4. Check the data I/O pins U432 (pins 9, 10, 11, 13, 14, 15, 16, 17) for activity. If no activity (stuck HI or LO) when output enable is LO, suspect U352; otherwise suspect U432.

Table 6-6 (cont)

3900 A12U664	NV RAM A12U664 (schematic diagram 1): If the system ram data bus, chip selects, or output enable lines are defective, the System µP will not function to run the diagnostics testing. Therefore, if test 3900 fails, the most likely problem is U664 itself. If the diagnostics tests do not run, the Kernel test will have to be used to isolate a system bus or address decoding problem. An NV RAM failure due to stored data being scrambled requires a "COLD START" to reload the NV RAM with correct nominal values. The 2430 will need a SELF CAL and an EXTENDED CAL of the ATTEN, TRIGGERS, and REPET after a COLD START to return it to a completely calibrated state.
4000 FPP	Front Panel µP A13U700 (schematic diagram 3): Testing Method: The Front Panel Processor test first sets all test results to NULL. Any failure to complete all the tests will result in a locked front panel. Depending on the nature of the failure, the Trigger LEDS may be latched in the first number of the test level that failed, the failure code may be flashed out on the LEDs (if it is the first failed test), or it may make it through the diagnostic, but with the FPP test marked FAIL. That information will help to isolate which circuitry may be defective and gives the starting point in troubleshooting a failure. It will be necessary to turn off the 2430 and turn it back on again to repeat the diagnostic testing from the front panel; however, testing may be done using GPIB diagnostic test commands. The Front Panel µP internal diagnostics require that the µP be reset. Therefore, the structure of the FPP tests is such that the processor is initialized when completed. This requires that ALL of the tests be run in order. Therefore, all tests will be run even though it appears that only a sub-test is being executed. Test Steps: 4100 U861 pin 9 should be reset to its LO state via U862B and U862A. 4200 U861 pin 6 should be reset to its HI state via U862C and U862D. 4300 U861 pin 9 (WR TO HOST) should clock pin 9 HI. 4400 U700 (Front Panel µP) checks its internal RAM, ROM, Timer, and A/D. Any failure will set the test result to FAIL. 4500 U861 pin 6 (FPDNRD) should clock pin 6 LO. 4600 U742 and U751. Four bit patterns are written to the FPP and echoed back. If these are not returned properly, the test result = FAIL. Troubleshooting Procedure: Failure of one of the Front-Panel µP tests may be indicated only by flashing out the failed test number on the Trigger LEDs, but if the diagnostic testing can continue past the failure, the Extended Diagnostic menu will be seen with the FPP test marked FAIL. The usual result of a Front Panel µP failure is a locked up front panel (the button and pots will not be functional). To rerun the diagnostic testing from the front panel to check the Trigger LEDs for the failed test number, it is necessary to turn off then turn back on the 2430.

Table 6-6 (cont)

Troubleshooting Front-Panel µP A13U700:

1. Check pin 5 for the 4 MHz clock.
2. Check pin 4 for +5 V, pin 1 for ground.
3. Check pins 8, 14, 16, 17, 19, 31, and 32 for +5 V and pins 6, 7, and 20 for ground.
4. Perform the Front Panel µP test if all the checks in steps 1, 2, and 3 were ok. If not, troubleshoot any problem area found by the checks.

Front Panel µP Test:

1. Turn off power and short pins 1 and 2 of J155 together. (The pins must remain shorted together during power-on.) This places the Front-Panel µP in the continuous self-diagnostic mode (Test 4400). Connect a test scope to view the signal present on pin 14 of U700.
2. Turn the power back on and observe the signal at pin 14. See test waveform illustration of Figure 6-9 for correct waveshape and timing.

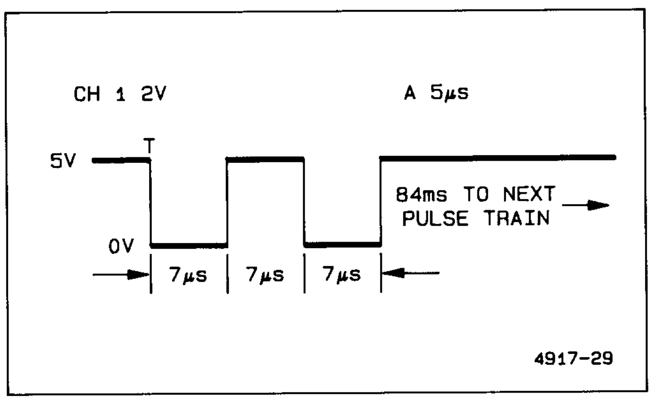


Figure 6-9. Front Panel µP diagnostics test.

3. If the test waveform is not present and the supply voltage, the ground, and the clock are correct, change the Front-Panel µP; it is possibly defective.

If the Front-Panel µP checks out ok, turn off the power and remove the jumper connected for the preceding Front Panel diagnostic test. Turn the 2430 back on and perform the following circuit checks for any of the Front Panel tests that failed when running the Extended Diagnostics via the GPIB. Use the circuit checks to isolate the problem in the associated circuitry. IF THE FPP DIAGNOSTICS TEST FAILED, THE ONLY WAY TO RUN THESE TESTS WILL BE VIA GPIB, AS THE FRONT PANEL WILL NOT RESPOND TO BUTTON PRESSES. To gain access to the 2430 via the GPIB when the EXT DIAG menu is being displayed, a MENU OFF command must be sent to exit extended diagnostics.

Table 6-6 (cont)

NOTE

Since the Front Panel μP is being reset in this test, there is no way to HALT if one chooses a CONTINUOUS loop mode and runs the tests from the front panel. However, to allow access to these features for any possible troubleshooting, looping has not been disabled. ONCE A TEST IS INVOKED IN CONTINUOUS MODE, A POWER OFF/ON CYCLE MUST BE USED TO EXIT FROM THE FRONT PANEL. Via the GPIB, the tests may be started and halted by sending the appropriate commands.

Set up the 2430 test scope as in Step 1 of the 2110 troubleshooting procedure.

Run tests 4100 through 4600 in CONTINUOUS mode. Use the CH 2 probe for the following checks while the specific test is selected and running.

4100 A13U861 pin 9 (FPINT):

1. Check U862 pin 1 for 0.2 μs negative strobe during the HI period of the trigger strobe. If not present, replace U862.
2. Check U861 pin 9 for a HI-to-LO transition. If not occurring, replace U861.

4200 A13U861 pin 6 ($\overline{\text{FPDNRD}}$):

1. Check U861 pin 1 for a negative strobe during the HI period of the trigger strobe. If not present, replace U862.
2. Check U861 pin 6 for a LO-to-HI transition from the strobe at U861 pin 1. If occurring, replace U861.

4300 A13U700 pin 12 (WR TO HOST):

1. Check that U861 pin 9 has a HI pulse. If not, select 50 ms/div and ENVELOPE acquisition mode on the test scope; then, run test 4000 for the scope under test. At pin 12 of U700, check for a strobe occurring near the falling edge of the trigger strobe. If the strobe is ok, replace U861. If missing, test for 4 MHz at U700 pin 5 and replace U700 if the 4 MHz clock is ok.

   If the 4 MHz clock is missing, troubleshoot the clock source. Restore the prior test scope setup as for test 2110 (a good use for RECALL SETUP if using a 2430 as the test scope.)

4400 DIAG BYTE A13U700:

1. Check that the enable pulse to U751 (pins 1 and 19) is present and save to REF1. If not present, check for an open between U862A pin 1 and U751 pins 1 and 19.
2. Display REF1 and probe U751 pin 18, 16, 14, and 12. These should all be LO during the time U751 is enabled. If not LO, it indicates either a problem in U700 or an invalid DC voltage level at one of the U700 inputs. If one of these four diagnostic bits is HI and the supply pins, etc., are ok, replace U700.

4500 A13U700 pin 13 (FPDNRD):

1. Select the 1/2 TRIG POSITION and set the Sec/Div setting to 1 ms on the test scope. Check for the FPDNRD clock pulse to U861 at pin 3 (leads the trigger strobe rising edge about 120 μs). If missing, replace U700.

Table 6-6 (cont)

2. Check for LO at U861 pin 6; replace U861 if pin 6 is HI.

3. Check A12U654 pin 13 for LO. Replace A12U654 if pin 13 is LO and test is failing.

4600 A13U742/A13U751:

1. Check for a pattern of 10100101 at U742 pin 19, 16, 15, 12, 9, 6, 5, and 2 at the rising edge of the trigger strobe (Word Recognizer Probe is useful for this check). If not, and U742 pin 11 is LO, then replace U742. If U742 pin 11 is HI, replace U700.

2. Check the enable pulse at U751 pins 1 and 19. Save and move to REF1.

3. Display REF1 and check for a 10100101 pattern coincident with the enable pulse at U751 pins 17, 15, 13, 11, 8, 6, 4, and 2. If not ok, replace U700.

4. Display REF1 and check for a 10100101 pattern coincident with the enable pulse at U751 pins 3, 6, 7, 9, 12, 14, 16, and 18. If not ok, replace U751.

4700 BATT STATUS

Battery A12BT800 (NVRAM keep-alive battery) (schematic diagram 1):

Testing Method:

There is no hardware exercised for this test. The operating system is informed by the front panel processor if the battery voltage is either high or low. The "test" is to read a memory location where the System μP has stored the status after checking with the FPP. If the status is unknown, the result is NULL. If the test "passes," it means that it is not defective in that direction.

Troubleshooting Procedure:

4710 HIGH:

Either the voltage is really high or the detection circuitry is defective.

1. Measure the battery voltage directly across the battery (BT800) and check for a range of 2.5 V to 3.5 V. If ok, then test from the + lead of BT800 to ground for the same or less voltage.

2. If ok, test for the same voltage range at A13U700 pin 21. If ok there, replace A13U700. If voltage is wrong at pin 21, backtrack to the problem component (suspect A12U490).

3. If the battery voltage is too high or the voltage to ground from the + lead is too high, check A12CR802. To ensure continued proper operation of the NVRAM, replace A12BT800 after correcting the overvoltage condition.

WARNING

When replacing the lithium battery, avoid personal injury by observing proper methods for handling and disposal. Improper handling may cause fire, explosion, or severe burns. Don't attempt to recharge and don't crush, disassemble, heat the battery above 212°F (100°C), incinerate, or expose contents of the battery to water. Dispose of battery in accordance with local, state, and national regulations.

4720 LOW:

Either the battery is defective or the detecting circuit is defective.

Table 6-6 (cont)

	1. Measure the battery voltage for a range of 2.4 V to 3.5 V. If low, replace the battery (BT800) observing the proper handling procedures. 2. If the battery voltage is correct, troubleshoot the detection circuitry as for a failure of test 4710, looking for the cause of a LOW reading.
5000 WP U470	Waveform μP A12U470 (schematic diagram 2): Testing Method: The nature of these tests is such that all tests must be executed in order and may not be individually executed. Therefore, any attempt to execute one test will result in all tests being executed. The Waveform Processor test first sets all test results to NULL. Any failures will be fatal in terms of instrument operation; however, the last test that was executed will be set FAIL and should help in diagnosing the cause of the problem. The Waveform μP command memory has been checked out by this time as well as the bus structure that permits the System μP to control the Waveform μP bus.
5100 RUN-TASK	Testing Method: Loads a task into Command Memory U440 and tells the Waveform μP to execute it. A 30 ms timeout is executed; and then, INTREG (bit 0) is tested for WPDN. If it has not been set, the task did not execute and terminate properly. If 5100 fails, it could be the Waveform Processor code ROMs, or the Waveform μP itself (U470). In any event, the Waveform Processor Kernel tests will need to be run to diagnose the source of the problem. Troubleshooting Procedure: Use the Waveform μP Kernel test in Procedure 8 to troubleshoot for a μP fault or a fault on the Waveform μP address or data bus.
5200 BUSGRANT	Testing Method: This test executes a bus request by setting bit D5 (pin 14) of PCREG U860 (schematic diagram 1) HI, delaying 10 ms, and checking bit D6 of INTREG (Interrupt Register) U654 to see if a BUSGRANT has occurred. Troubleshooting Procedure: Set up the 2430 test scope as in Step 1 of the 2110 troubleshooting procedure. Run test 5200 in CONTINUOUS mode. Using the CH 2 Probe: 1. Check U860 pin 15 for LO-to-HI transition. If not occurring, replace U860. 2. Check U332D (schematic diagram 2) pin 13 for LO-to-HI transition. If not occurring, replace Waveform μP U470. 3. Check U332D pin 11 for LO-to-HI transition. If not gating, replace OR-gate U332.

Table 6-6 (cont)

5300 VERSION-CHK	Waveform μP ROM A12U480 and A12U490 (schematic diagram 2): Testing Method: The version number in the header is preset to "?" and is filled in by this test. If the test fails, the "?" will remain in the header for further indication of an error. A Waveform μP reset causes the Waveform μP to read the version number bytes of the Waveform μP code. If the version number is incorrect, the Waveform μP code is incompatible with the System μP code and may not execute properly. Troubleshooting Procedure: If test 5300 fails, replace Waveform μP ROMs U480 and/or U490 with the correct ones for the version of System μP code being used.
6000 CK SUM-NVRAM	Nonvolatile RAM Checksum A12U664 (schematic diagram 1): Testing Method: Some of the CRCCs (check sums) are computed at power-down and will be valid only at power-up. Therefore, executing tests 5000 through 5003 will only display the flags that resulted from power-up diagnostics. **NOTE** *FAIL and PASS flags in the Extended Diagnostics menu show the results of the last test ran. If a defective device that has previously caused a FAIL flag to be set is replaced, the test must be run again to obtain a PASS indication in the menu.* When the instrument is SELF CALIBRATED, a CRCC is calculated and stored for the Calibration Constants in NV RAM. When power-down is executed, the values of the front-panel variables have a CRCC calculated and stored. When a waveform is saved, the CRCC is calculated for the waveform and headers and saved. On power-up, all of these are recalculated and compared to the stored CRCC word. If they do not agree, that test fails.
6100 CAL CONSTANTS	Calibration Constants: Troubleshooting Procedure: If FAIL, the calibration constants have been lost and a COLD START is executed. The instrument must be recalibrated to return to calibrated operation after a COLD START. A failure of 6100 is serious to the normal operation of the 2430, and the cause of the failure should be found and corrected to prevent reoccurrence. 1. Check BT800 and the components that connect and disconnect the battery from the NV RAM at power-off and power-on respectively.

Table 6-6 (cont)

	WARNING *If replacing the lithium battery, avoid personal injury by observing proper methods for handling and disposal. Improper handling may cause fire, explosion, or severe burns. Don't attempt to recharge and don't crush, disassemble, heat the battery above 212°F (100°C), incinerate, or expose contents of the battery to water. Dispose of battery in accordance with local, state, and national regulations.* 2. Test several times by cycling the power after the instrument has completed its self testing. If the test continues to fail, check the PWRUP line to U640 pin 2, and ensure that it is reset LO when the power line voltage drops below the minimum line voltage. If this line does not go LO soon enough, the power-down routines will not calculate the current check sums before the power is completely lost.
6200 FP-LAST	Front Panel Control Settings: Troubleshooting Procedure: If the last front-panel settings have been lost, the instrument will be set up in the INIT PANEL configuration in the SAVE/RECALL SETUP menu. If the power remains off for an extended period (more than 3 to 5 days), the short-term NV RAM will lose the stored data. If the data is lost with a short power-off, check capacitor C896 and its connect and disconnect circuitry.
6300 WFM-HEADERS	Waveform Data: Troubleshooting Procedure: The reference waveform memories will be declared EMPTY if the WFM-HEADERS do not check correctly. If the power remains off for an extended period (more than 3 to 5 days), the short-term NV RAM will lose the stored data, and new waveforms will have to be acquired to fill the reference memories. If the data is lost with a short power-off, check capacitor C896 and its connect and disconnect circuitry.
7000 CCD	CCD/CLOCK DRIVERS A10U350 (CH 2) and A10U450 (CH 1) (schematic diagram 10): Testing Method: These tests, if passed, indicate that the hardware is functional. IF A SELF DIAG OR EXTENDED DIAG TEST FAILS, ONE CANNOT ASSUME THE HARDWARE IS DEFECTIVE UNLESS THE SAME TEST FAILS A SELF CAL. The reason that SELF CAL must be run to assure a hardware failure is that SELF CAL computes new values of the constants for each test and uses them in the subsequent tests; whereas, diagnostic tests use previously stored constants for making the tests. If those stored values are not valid for the present operating temperature of the scope, the test may not be able to converge to a solution. The CCD has two classes of adjustments, centering and gain. In addition, several CCD parameters are measured and stored for use in Dynamic Calibration. Centering must be performed in all four acquisition modes because of offset differences in the different paths. Gain is performed in Short-Pipeline and FISO modes.

Table 6-6 (cont)

Failure of Tests in 7300 and 7400:

Troubleshooting Procedure:

The CCDs are a good suspect if any of the 7000-series diagnostic tests failed, especially in the 7300 and 7400 subsets. The Extended Diagnostics menu should be examined to determine if the problem is in only one or in both of the channels.

If both channels fail:

1. Check the CCD clocks. To determine if a clock problem is internal or external to the CCD/Clock Driver hybrid, compare the collector voltages of Q450, Q460, Q550, and Q560 to Waveform illustration 67 (associated with schematic diagram 10). If any of the clock waveforms are different, check the base of the associated transistor(s). If the base voltage is switching correctly, change the defective transistor. If not switching, trace back to the clock source from U470, the Phase Clock Array (on diagram 11), and check there. If the clocks are not correct there, change U470.
2. If the clocks are running correctly at the collectors of Q450, Q460, Q550, and Q560, check to see if pins 2, 3, 5, 6, and 7 of R470 are switching correctly (compare pins 2, 3, 4, and 5 to waveforms 68 through 71 on diagram 10). If not switching correctly, check the outputs of U470 for correct clock. If not present there, troubleshoot the Phase Clock Array (U470); if ok there, find the open.
3. If the clocks seem to be functioning normally to this point, check the shared clock signals at TP345, R366, R465, and R466. If these points are not switching, change the CCD/Clock Drivers (U350 and U450).

If a single channel fails:

1. Change the associated CCD/Clock Driver. If the problem is not corrected, troubleshoot the CCD Output circuitry.

NOTE

If any CCD or Peak Detector is changed, do not run a SELF CAL until the CCD OUTPUT Gain has been set using the EXT CAL ADJUSTS, test pattern number 6. Adjust the ±2 division gain for the changed channel both Side 1 and Side 2 according to the directions given in the display.

Failure of tests in 7100 or 7200:

The CCD output stage is a probable area for failure if a SELF CAL fails any of the 7100 or 7200 tests. Check these tests to see which channel did not pass, then perform the following steps.

CCD Output Troubleshooting Procedure (Schematic Diagram 14):

NOTE

Channel 1 components are reference (Channel 2 components are in parenthesis).

1. Input the 2430 calibrator signal to the channel that is not operating properly. If neither is working, start with CH 1. CH 1 components will be referenced, with the CH 2 circuit numbers given in parentheses. Set the bad channel to 100 mV/div, DC coupled, with 50 Ω termination off. Adjust the screen waveform so the ground dot on the 2430 under test is 2 divisions below center screen if possible. Set the input coupling of the other channel to ground. Turn the A SEC/DIV to 5 μs.

Table 6-6 (cont)

2. Verify that pins 1 and 5 (the CCD outputs) of R876 (R886) look similar to waveform 104 (on schematic diagram 14), with center screen being +5 V. If these waveforms do not appear, troubleshoot the CCD/Clock Drivers. Verify that pins 3 and 7 of R876 (R886) resemble waveform 105. Again, if this waveform does not appear, go to the CCD/Clock Driver troubleshooting.

3. Examine pin 1 of U770A and U870A (U780A and U880A). The input waveform should have an offset of +7.5 V, which is center screen in waveform 106. If this waveform does not look right, check the parts in this section for failures.

4. Compare pins 1 and 8 of U560 (pins 9 and 16 for channel 2) to waveform 107. If this waveform does not appear, check to see that pins 3 and 6 of U560 are switching between 0 and +15 V. If they are, then the switch (U560) is bad. If they are not switching, check to see if the base of Q660 (Q670) is switching between 0.5 V and 0 V. If it is, the transistor is bad. If it is not, trace $\overline{\text{OSAM1}}$ ($\overline{\text{OSAM2}}$) back to the Time Base board.

5. Observe the voltage at pin 7 of U770 and U870 (U780 and U880). It should be similar to waveform 110, except that an offset of up to ±1.3 V may appear. If this is not the result, check the +9 V and the centering voltage (7.5 V ±1.3 V). If the voltages are correct, check U770 and its associated transistors and other components for failure.

6. Check the collectors of Q770 and Q870 (Q780 and Q880). These should look like waveform 109, where center screen corresponds to ground. If they do not, make sure the bases are switching on and off. If they are switching and a collector is not, check the transistor for a collector-to-emitter short. If not switching on the base, trace the associated $\overline{\text{DS}}$ signal back to the Time Base board. The timing relationships of the $\overline{\text{OSAM}}$ and the $\overline{\text{DS}}$ signals are shown in waveform 45 through 51 of the System Clocks schematic (diagram 7).

7300 EFFICIENCY

CCD/CLOCK DRIVERS A10U350 and A10U450 (schematic diagram 10):

Testing Method:

This test measures the transfer efficiency of the CCD by comparing the gain of columns 2 and 16 of the CCD B register arrays. To do this, a ±4 division input is applied to the Peak Detector calibration inputs and acquired. Efficiency loss and apparent offset for the gain are both calculated and stored for use in dynamic data correction. Efficiency loss of more than 6% will cause an error to be flagged. Testing is performed at two SEC/DIV settings (2 μs and 500 ns) on all four CCD channels.

Troubleshooting Procedure:

If all other tests are ok, the most probable cause of failure is a defective CCD; replace the failed CCD.

7400 PD-OFFSET

PEAK DETECTORS A10U340 (CH 2) and A10U440 (CH 1) (schematic diagram 10):

Testing Method:

This test is to check the match of the offsets of the two paths through the peak detectors. A 0 V cal signal input (DAC value = 2048) is acquired and the A and B peak detector and D and C peak detector pairs (see Figure 3-5 in Section 3 of this manual) are matched by iteratively adjusting the appropriate PDOS (peak-detector offset) DACs and remeasuring the difference until offsets are matched. If matching cannot be accomplished within 1/2 DL for calibration or 1 DL for diagnostics, the test terminates due to acquisition count, and the test result is set to FAIL; otherwise, it passes.

Table 6-6 (cont)

	The SPECIAL menu choices under Extended Functions in Version 2.0 firmware provide a diagnostic switch to divide the signal acquisition path. CAL PATH ON/OFF turns on or off the calibration signal path to the Peak Detectors. It is a useful diagnostics device in the event that large offset errors have driven the display off-screen. Switching CAL PATH ON eliminates the Attenuators and Preamplifiers from the input signal path and places the calibration reference level on the display. If that brings the display back on screen, then the offset problem may be isolated to the Attenuators or Preamplifiers; if not, then the problem may be in the Peak Detectors or CCDs. With CAL PATH ON, the FORCE DAC test may be used to check the operation of the Peak Detectors and CCDs using the CURS (CAL) adjustment. Troubleshooting Procedure: 1. Do a COLD START and use the FORCE DAC test to determine if the DAC system can control the PD-OFFSET voltages (PD11, PD13, PD21, and PD23) correctly. If not, troubleshoot the DAC system. 2. If the DAC system is functioning normally, the most probable cause of a failure is a faulty Peak Detector. Replace the Peak Detector of the failing channel. **NOTE** *If any CCD or Peak Detector is changed, do not run a SELF CAL until the CCD OUTPUT Gain has been set using the EXT CAL ADJUSTS, test pattern number 6. Adjust the ±2 division gain for the changed channel, Side 1 and Side 2, according to the directions given in the display.*
8000 PA	Preamplifiers A10U320 (CH 2) and A10U420 (CH 1) (schematic diagram 9): Testing Method: The PA tests, if passed, indicate that the analog acquisition circuitry is functional. IF A SELF DIAG OR EXTENDED DIAG TEST FAILS, ONE CANNOT ASSUME THE HARDWARE IS DEFECTIVE UNLESS THE SAME TEST FAILS A SELF CAL. The reason that SELF CAL must be run to assure a hardware failure is that SELF CAL computes new values of the constants for each test and uses them in the subsequent tests; whereas, diagnostic tests use previously stored constants for making the tests. If those stored values are not valid for the present operating temperature of the scope, the test may not be able to converge to a solution. The Preamplifier has constants for Position Offset, Position Gain, Balance, Normal and Invert Gain, and Max Variable Gain. There is some interaction between adjustments. This effect is addressed by always using the previously stored constants in any setup and executing SELF CAL twice from a COLD START to assure an iterative solution of the calibration constants. Troubleshooting Procedure: 1. If SELF CAL fails, the calibration constants will most likely not be close enough to an operationally good value for the portions of the Preamp that work to function properly. Do a COLD START to replace the stored calibration constants with nominal values. **NOTE** *After a COLD START, the 2430 will need partial recalibration after it is repaired to return it to correct adjustment.*

Table 6-6 (cont)

2. If the 8000 level is flagged FAIL, there will be failure at one or more of the lower level tests. This is the case because one failure that misbiases the Preamp can cause several SELF CAL tests to fail.

3. After doing a COLD START, use the FORCE DAC test to determine if the DAC system can control the Preamp DAC voltages correctly for the tests that are flagged FAIL. Troubleshoot the DAC system for those DAC outputs showing no or improper control.

4. Check that the Preamp is responding to the DAC control voltage being changed. These are respectively for CH 1 and CH 2:

   1POS and 2POS to pin 17 for position input.

   CH1G and CH2G to pin 18 for gain control.

   CH1B and CH2B to pin 2 for balance.

   The check is set up by first doing a COLD START (to again set the calibration constants to known values), and then applying a 4-division signal to the CH 1 and CH 2 vertical inputs (or to the bad channel if only one is bad). Observe the signal on the crt, if possible; otherwise, use a test scope to probe the vertical signal path to check for correct response. Since the Preamp outputs are not accessible, use the output of the Peak Detectors to verify the signal through the Preamp. The side 3 Peak Detector output for CH 1 may be checked on R441 and R540; and for the CH 2 side 3 output, check at R244 and R341.

   Use either the Front Panel Controls or the Force DAC test to check the VARIABLE GAIN and VERTICAL POSITION. Balance may be varied only using the Force DAC function. Varying the channel balance should appear as a dc offset change to the vertical signal level. Prior to making any adjustments after a COLD START (either with the Front Panel controls or the Force DAC function), the signal at the output of the Peak Detectors should have a +8.7 V dc level with an ac signal (replica of the input signal) of approximately 0.5 V peak-to-peak.

5. The Preamplifier operating mode is set by a serial data word sent from the System μP. The CD input, pin 22, is the serial data input. A TTL-level logic swing should be present on this line whenever the Attenuators, Preamps, or A/B Trigger Generator operating modes are being set up. If there are no FAIL flags under these major test categories, the CD circuitry is most likely functioning properly. The $\overline{CC}$ input, pin 23, is the control clock input, and it should have a TTL-level logic swing on it only when the particular hybrid, in this case the Preamp hybrid, is being set up. Check that this line is high initially and pulses LO eight times for each Preamp load cycle. (The eight pulses may be separated into several groups of pulses.)

6. The Preamps have bypassed and decoupled voltage supplies. Check that the bypassing components in series with the power supplies are not open. Also check that the dc bias voltages at the Preamp are approximately the levels indicated on the schematic diagram in the service manual.

7. If the Preamp hybrid itself is suspected of being defective and the other channel is fully functional, swap Preamp hybrids between channels to see if the problem moves to the other channel. If so, replace the defective Preamp. If not, check the hybrid mount connections of the defective channel for corrosion or contamination that may be causing a poor contact.

Table 6-6 (cont)

8100 POSITION OFFSET	Acquisition System Position Offset: Testing Method: Position Offset is calculated at 50 mV per division only. Position offset must be performed for all four acquisition modes to compensate for the common-mode offsets in the CCD arrays that are not corrected by CCD centering. After the hardware is set up and the CCD constants set for the particular mode of operation, the Preamplifier is balanced by executing the balance routine, but only changing the DAC settings—not the cal constants. This assures an accurate position measurement. The Position Offset is then calculated by acquiring a ground level signal and comparing the Acquisition Memory value to what a ground acquisition should be (center screen is 00h). If the value is not within 1/2 DL for calibration or 1 DL for diagnostics, the position DAC outputs (CH1-PA-POS and/or CH2-PA-POS) are adjusted to compensate. When the acquisition is within limits, the test result is set to PASS. If the position offset cannot be adjusted to within specification, the acquisition count for an abort is taken, and the test result is set to FAIL. Troubleshooting Procedure (refer to test 8000 for more information): 1. Check that the decoupling network, R420/C423 or R222/C222 is functional. 2. Use the FORCE DAC test to determine if the CH1-PA-POS and/or CH2-PA-POS voltages are being controlled by the DAC System. If not, troubleshoot the DAC System. 3. Use the SPECIAL menu choice of CAL PATH ON to determine whether the offset error is prior to the Peak Detectors or after. Troubleshoot in the appropriate direction to locate the source of the offset error. 4. Check that the bypassing components in series with the power supplies are not open. Also check that the dc bias voltages at the Preamp are approximately the levels indicated on the schematic diagram in the service manual. 5. If the Preamp hybrid itself is suspected of being defective and the other channel is fully functional, swap Preamp hybrids between channels to see if the problem moves to the other channel. If so, replace the defective Preamp. If not, check the hybrid mount connections of the defective channel for corrosion or contamination that may be causing a poor contact. 6. Swap Peak Detector hybrids between channels to see if the problem channel reverses. If so, replace the faulty Peak Detector.
8200 POSITION GAIN	Preamplifier Position Gain A10U420 and A10U320 (schematic diagram 9): Testing Method: Position Gain is calculated at 50 mV per division only, using the stored Position Offset calibration constant. The DAC counts corresponding to +4 divisions of Position Offset are added to the Position Offset constant and an acquisition is made. After storing the results, a corresponding −4 division acquisition is made, and the two values of acquisition memory are checked for eight divisions of change in the calibration limits. The Position Gain constant is then calculated as a result of the data taken and stored as a Position Gain calibration constant. A Position Gain constant more than 20% different from the nominally expected value will cause the test to fail. **NOTE** *POSITION GAIN is not an iterative calibration as the gain is directly calculated.*

Table 6-6 (cont)

Troubleshooting Procedure (refer to test 8000 for more information):

1. Check that the decoupling network, R420/C423 or R222/C222 is functional.
2. Use the FORCE DAC test to determine if the CH1-PA-POS and/or CH2-PA-POS voltages are being controlled by the DAC System. If not, troubleshoot the DAC System.
3. Check that the bypassing components in series with the power supplies are not open. Also check that the dc bias voltages at the Preamp are approximately the levels indicated on the schematic diagram in the service manual.
4. If the Preamp hybrid itself is suspected to be defective and the other channel is fully functional, swap Preamp hybrids between channels to see if the problem moves to the other channel. If so, replace the defective Preamp. If not, check the hybrid mount connections of the defective channel for corrosion or contamination that may be causing a poor contact.
5. Swap Peak Detector hybrids between channels to see if the problem channel reverses. If so, replace the faulty Peak Detector.

8300 PREAMP BALANCE

Preamplifier Balance A10U420 and A10U320 (schematic diagram 9):

Testing Method:

Balance is performed in all five Preamplifier ranges, and on both channels simultaneously. Balance is calculated by first taking a ground acquisition in non-invert. Then an acquisition is made in INVERT, and a new balance DAC voltage is calculated that will keep the trace shift between non-invert and INVERT within limits for calibration or diagnostics. This is done until balance is within specification or until the maximum number of acquisitions has been reached. If the result is within specification prior to acquisition abort, the test result is set to PASS; otherwise, it is set to FAIL.

Balance Test Limits:

Range	50 mV	20 mV	10 mV	5 mV	2 mV
Cal limit	1/2 DL	1/2 DL	1 DL	1 DL	2 DL
Diag limit	1 DL	1 DL	2 DL	2 DL	4 DL

Troubleshooting Procedure (refer to test 8000 for more information):

1. Check that the biasing network associated with the balance input, pin 2, and pins 4, 20, and 25 is functional and that the voltage levels are approximately those indicated on the schematic diagram in the service manual.
2. Use the FORCE DAC test to determine if the CH1-BAL and/or CH2-BAL voltages are being controlled by the DAC System. If not, troubleshoot the DAC System.
3. Check that the bypassing components in series with the power supplies are not open. Also check that the dc bias voltages at the Preamp are approximately the levels indicated on the schematic diagram in the service manual.
4. If the Preamp hybrid itself is suspected of being defective and the other channel is fully functional, swap Preamp hybrids between channels to see if the problem moves to the other channel. If so, replace the defective Preamp. If not, check the hybrid mount connections of the defective channel for corrosion or contamination that may be causing a poor contact.
5. Swap Peak Detector hybrids between channels to see if the problem channel reverses. If so, replace the faulty Peak Detector.

Table 6-6 (cont)

8400 PREAMP GAIN and 8500 PREAMP INVERT GAIN	Testing Method: During calibration, gain constants are computed by using the Balance control to position +2.5 and −2.5 divisions and computing the next gain DAC value until the result is set to be within specifications. For diagnostics, the swing is reduced to ±1.5 divisions to allow for thermal drifts that occur due to temperature changes between power off and power on. The effects of thermal drift are especially noticeable at high vertical sensitivities. Limits are 1 DL for calibration and 2 DL for diagnostics. Gain is done for all five Preamplifier ranges in both normal and invert modes. Both Preamplifier channels are tested simultaneously. Since the transfer function of the gain control is non-linear, correction is done iteratively either until the gain is within specifications or until the maximum number of acquisitions allowed for the test has been reached. If the result is found prior to a test abort, the test result is set to PASS; otherwise, it is set to FAIL.
	Troubleshooting Procedure (refer to test 8000 for more information): 1. COLD START and use the Force DAC test to check that the DAC system is controlling the CH1-GAIN-CAL and CH2-GAIN-CAL voltages correctly. If not ok, troubleshoot the DAC system. 2. Check that the bypassing components in series with the power supplies are not open. Also check that the dc bias voltages at the Preamp are approximately the levels indicated on the schematic diagram in the service manual. 3. If the Preamp hybrid itself is suspected of being defective and the other channel is fully functional, swap Preamp hybrids between channels to see if the problem moves to the other channel. If so, replace the defective Preamp. If not, check the hybrid mount connections of the defective channel for corrosion or contamination that may be causing a poor contact. 4. Swap Peak Detector hybrids between channels to see if the problem channel reverses. If so, replace the faulty Peak Detector.
8600 PREAMP VAR MAX	Testing Method: In this test, the change in Preamplifier control which will yield an attenuation of 2.75 from the Calibrated VOLTS/DIV setting is measured on both channels at 50 mV per division in normal mode. This is done by re-performing the 50 mV noninverted gain test seeking a value of +2.5 divided by +2.75 (+0.91) division and −2.5 divided by −2.75 (−0.91) division on the output. The difference between the resulting gain control DAC setting and the gain control DAC calibration constant is the Var Max value. Inability to achieve an attenuation factor of 2.75 is a test failure.
	Troubleshooting Procedure (refer to test 8000 for more information): See the Troubleshooting Procedure for tests 8400 and 8500.

Table 6-6 (cont)

8700 ATTENUATORS	Channel 1 and Channel 2 Attenuators AT400 and AT300 (schematic diagram 9):

Testing Method:

THIS TEST IS ONLY PERFORMED USING EXTENDED CALIBRATION. With the Preamplifier set to 50 mV non-inverted, the Preamplifier gain test is repeated interactively using standard dc test voltages applied to the CH 1 and CH 2 inputs. By adjusting the Preamplifier balance to give -2 divisions, the output is swung between -2 (input grounded), and $+2$ (input set to 0.2 V per div), divisions. The gain control DAC is adjusted to achieve an output within specifications. The difference between the resulting control DAC setting and the gain calibration constant measured at 50 mV per division (non-inverted) is the attenuator gain constant. If a solution cannot be found, or if the resulting solution is more than a 2% gain error, the test result is set to FAIL. If the test fails, an attenuator gain of 0 (nominal) is stored for the calibration constant under the assumption that the test setup may be in error. The test is repeated for all three vertical attenuators (1X, 10X, and 100X) using input test voltages of 0.2 Vdc, 2 Vdc, and 20 Vdc.

Troubleshooting Procedure:

1. Check that the correct test voltages are used for the ATTEN calibration step.

2. Check that one audible click is heard when changing the VOLTS/DIV setting between 50 mV and 100 mV (10X attenuation) and between 500 mV and 1 V (100X attenuation). Also check that one audible click is heard when changing the Vertical input coupling between DC and AC, and when turning the fifty ohm input ON and OFF. Several clicks will normally be heard when switching in and out of GND Coupling.

3. If one and only one audible click was heard for each of the first four front-panel changes above, then the circuitry that drives the four mag-latch relays in each attenuator is functioning properly by switching the individual relays to the opposite latched position (the audible click).

4. Connect the output of a Standard Amplitude Calibrator to the vertical input of the failing channel using coaxial cable with no terminator. Set the Standard Amplitude Generator output and the VOLTS/DIV setting on the 2430 to the values given in the following table and check the signal path between the Attenuator and the Preamplifier input of the failed channel. With a 10X probe on the test scope, view the signal at the Preamp input pin. Use NOISE REJ Trigger Coupling and 20 MHz Bandwidth on the test scope to clear up the trace noise and obtain a stable trigger. If only one channel is bad, the other channel of the 2430 may be used to view the signal. The signal amplitude out of the Attenuator and into the Preamp should be approximately 50 mV peak-to-peak for each attenuator setting in the three ranges. A possible, but unlikely, source of a failure that is not in the signal path between the Attenuator and the Preamp is a shorted capacitor (C414 or C311) connecting to the Attenuator.

ATTENUATOR CHECK

Signal In	VOLTS/DIV	Signal Out
50 mV	2 mV to 50 mV	50 mV
0.5 V	100 mV to 500 mV	50 mV
5 V	1 V to 5 V	50 mV

5. If one channel shows PASS flags on all the ATTEN tests, swap the Preamps between channels to determine if the Preamplifier inputs are ok. If that swaps the problem, replace the faulty Preamp. If the problem remains in the same channel, replace the defective Attenuator.

Table 6-6 (cont)

	6. If none or only some audible clicks were heard, and assuming the Attenuator Register and Preamplifier tests passed the Power-on SELF TEST or a subsequent EXTENDED DIAGNOSTIC test, troubleshoot the magnetic-latch buffers (U510 and U220) and the latching circuitry (Q620, Q621, U520, and associated components) on diagram 9. 7. Check the ATTEN CLK line for the presence of a signal at the times when an audible click should be heard. 8. Shift Registers U221 and U511 are assumed functional with proper input signals if there is a PASS flag present at the 2520 level of the Extended Diagnostics menu after performing the EXT DIAG diagnostics test. Otherwise, troubleshoot the Shift Registers for the source of failure.
9000 TRIGGERS	A/B Trigger Generator A10U150 (schematic diagram 11): Testing Method: The Triggers tests, if passed, indicate that the analog trigger circuitry is functional. IF A SELF DIAG OR EXTENDED DIAG TEST FAILS, ONE CANNOT ASSUME THE HARDWARE IS DEFECTIVE UNLESS THE SAME TEST FAILS A SELF CAL. The reason that SELF CAL must be run to assure a hardware failure is that SELF CAL computes new values of the constants for each test and uses them in the subsequent tests. Whereas, diagnostic tests use previously stored constants for making the tests. If those stored values are not valid for the present operating temperature of the scope, the test may not be able to converge to a solution. Triggers have constants for offset and gain. The value of Level DAC output that caused the trigger to change state is assumed to be the upper hysteresis level in plus slope and the lower hysteresis level in negative slope. **NOTE** *TRIGGER MODE is set to A and B to program ATG output to be the AND of A and B triggers. Thus ATG may be tested as an indication that triggering has occurred. This requires that BOTH A AND B TRIGGERS MUST BE FUNCTIONAL TO GET EITHER TEST RESULT TO PASS.* Troubleshooting Procedure: External and Internal Trigger Path (common circuitry): 1. For this test to result in a PASS flag, several major circuit blocks must work correctly. Common to both the external trigger signal path and the internal trigger signal path is A/B Trigger Generator A10U150 (schematic diagram 11) with the following related input signals: a. ATHO (A Trigger Holdoff) from the Trigger Holdoff circuit (schematic diagram 13) to A/B Trigger Generator U150 through a level shifting resistor string of R225 and R134. The level at U150 pin 15 is less than +3.3 V for logic LO and greater than +4.0 V for logic HI. The input must be logic HI for a trigger output to occur. If the ATHO signal is not correct, see the "HOLDOFF PROBLEMS" in Procedure 4. b. A TRIG LEVEL and B TRIG LEVEL from the DAC System (schematic diagram 6) via A10U640A (A TRIG LEVEL) and A10U640D (B TRIG LEVEL) and filter networks R250-C250 or R162-C160 is another. These voltage levels should be adjustable from −1.3 V to +1.3 V using the FORCE DAC function.

Table 6-6 (cont)

c. ACD (Acquisition Control Data), A TRIG CLOCK, and B TRIG CLOCK are the signals that load the internal shift register of U150 with MODE, CPLG, and SLOPE requirements for the trigger signal. These lines should have TTL level voltage swings, and the A TRIG CLOCK clock and B TRIG CLOCK signal lines should only have transitions when the associated A or B Trigger MODE, CPLG, or SLOPE are changed. The ACD data line (U150 pin 46) should be checked for the presence of voltage transitions.

d. Six $\overline{SR}$ data lines set up the A TRIG SOURCE and B TRIG SOURCE selections. Shift Register A10U140 (schematic diagram 5) provides these signals, and it is tested by test 2510 of the Extended Diagnostics. The signals are assumed correct for a PASS flag at that diagnostic level. If a FAIL flag is present, follow the Troubleshooting Procedure under that diagnostic level.

2. High speed ECL level shift stages, Q250 and Q251 for MAIN GATE and Q150 and Q151 for DELAY GATE, are common paths for both Internal and External trigger sources. These stages should have an ECL input swing of less than +3.4 V for logic LO and greater than +4.0 V for logic HI. The output swing should be greater than −1.6 V for logic LO and less than −1.1 V for logic HI.

3. Trigger Logic Array A10U370 is also common to both the external and internal trigger signal paths. Related signal inputs that must be correct are:

a. EPTHO (End Pretrigger Holdoff) from Timebase Controller A11U670 (schematic diagram 8) via buffer U680E on the Timebase board. EPTHO must be TTL high for a trigger to occur. If that is not occurring, see the Timebase and System Clocks troubleshooting chart in the Diagrams pages at the back of this manual.

b. $\overline{WR}$, $\overline{ACQSEL}$, A0-A3, and GAD0-GAD7 are the digital control and data lines. These signals are tested by test number 2510 of the Extended Diagnostics and, if a PASS flag is present, are assumed to be correct. Otherwise refer to that diagnostics troubleshooting procedure for a failure of 2510.

4. The ATG path from Trigger Logic Array U370 to data bus bit D0 is also a common path. The AND logic function of the A Trigger Gate and the B Trigger Gate is performed within Trigger Logic Array U370. The path from A/B Trigger Gate inputs, through a logic ANDing gate, to the Trigger Logic Array Output (pin 63, ATG) is asynchronous and direct, delayed only by the propagation delay of the internal logic gate structures. The ATG signal has a TTL voltage level swing. The ATG output signal path is through R368 and W110 to buffer U851C (schematic diagram 13) and then through tristate buffer U761 to the D0 bit of the System μP data bus. This path through buffer U761 is not tested by test 2000 (Register Tests) of Extended Diagnostics, so it must be verified from U370 through U761 to be operational. ATG also clocks Trigger Holdoff flip-flop U872A.

EXTERNAL TRIGGER PATH—EXCLUSIVE:

5. EXTERNAL TRIGGER PREAMP A10U100 (schematic diagram 9) is only in the External Trigger Signal path. It should be verified to be functional if FAIL flags appear only at Extended Diagnostics levels with EXT labels.

a. There are only two mode control bits that set up U100. These bits are assumed to be correct if level 2510 of Extended Diagnostics shows a PASS flag. These two bits set up the 1X or 5X attenuation for each EXT TRIG channel.

b. Q110, U120, and associated circuitry produce a +5 V source that tracks the instrument −5 V source. The voltage level at U100 pins 17 and 44 should be verified to be +5 V. The decoupled −5 V power supply voltage at pin 7 of U100 must be present for this circuit and for the circuit of U100 to function properly.

Table 6-6 (cont)

	c. The voltage at U100 pins 25 and 36 should be verified to be +5 V to test for defective decoupling components (L210/C211 and L120/C112). INTERNAL TRIGGER PATH—EXCLUSIVE: 6. CH 1 and CH 2 PREAMPS U420 and U320, U230A, U230B, and associated components (schematic diagram 9) supply the Internal CH 1 TRIG and CH 2 TRIG signals, and should be verified for functionality if FAIL flags appear only on Extended Diagnostics levels with CH 1 or CH 2 labels. a. Operational Amplifiers U230B and U230A and associated components form common-mode level-trimming amplifiers for the CH 1 and CH 2 ±PICK outputs respectively. Since the CH 1 and CH 2 trigger signals originate from the −PICK outputs of the CH 1/CH 2 PREAMPs (U420 and U320), improper operation of these bias-trimming amplifiers will result in a diagnostic FAIL flag. When operating properly, the arithmetic average of the +PICK and −PICK bias voltages should be at or very near 0 V. If this is not the case, the amplifier circuitry needs to be repaired. (Note that the two circuits interact with each other.) b. If a channel PREAMP is suspected of having a defective −PICK output and the other channel shows no Diagnostics FAIL flags, swap PREAMPs to see if the problem moves to the other channel. If it does, replace the defective PREAMP.
9100 TRIGGER OFFSET	Trigger Signal Offset: Testing Method: A ground signal is provided to the trigger from the CH 1 or CH 2 pickoff (internal triggers) or from an external source (EXT1, EXT2 external triggers). This is done by grounding the attenuator or by providing a short at the EXT TRIG inputs. The trigger level DAC is moved in two binary searches to determine where the upper and lower hysteresis levels are while holding the "other" trigger level in such a state that should be "triggered." The constant is then set to the hysteresis level that represents the triggering point for the desired slope at zero input. The test is repeated for both A and B triggers for all input paths. For EXT TRIG inputs, levels are measured for both the 1X and 5X (attenuated by a factor of five) amplifier ranges. An additional offset for the trigger slope is obtained by measuring the trigger in minus (−) slope with a CH 1 input and computing the difference between the obtained value and that measured in plus (+) slope.
	Troubleshooting Procedure: 1. Run test 9100 in CONTINUOUS mode. 2. Starting with the signal path for ATG at pin 2 of A13U761 (schematic diagram 13), work backwards toward the trigger signal source using a test oscilloscope to check that the proper signals are present with the proper bias levels and voltage swings. 3. Use the troubleshooting comments under 9000 level as a guide. 4. ATG signal should be present at TTL level voltage swings. 5. MAIN and DELAY GATE signals to Trigger Logic Array A10U370 (schematic diagram 11) should be present at ECL voltage level swings. 6. A TRIG LEVEL and B TRIG LEVEL signals, at pins 13 and 37 of A10U150 respectively, should have several levels: ±1 V swings, ±0.5 V swings, and voltage swing levels that approach a final level of gain iteratively as the binary search is done.

Table 6-6 (cont)

	7. CH1 and CH2 TRIGGER signals should be at or near 0 V. (LR421/LR220 can be open and not cause a FAIL flag to appear at this diagnostic test level since this test only requires CH1/CH2 trigger signal to be near 0 V, which is the case with these components open. However, a FAIL flag will appear at the 9200 diagnostic level.) 8. EXT1 and EXT2 TRIG signals are provided externally, and the external signal paths to the Trigger Source Select function within A/B Trigger Generator U150 are not tested by running test 9200 CONTINUOUS Mode. If FAIL flags only appear at EXT diagnostic levels, the EXT source inputs of U150 are most likely functional, and the problem is either External Trigger Preamp U100 and related bias circuitry, or the BNC and R1001/R1003 signal path from the front panel.
9200 TRIGGER GAIN	Trigger Signal Gain: Testing Method: Trigger gain is measured for both A and B triggers and for CH 1 and CH 2 inputs. Trigger gain is set by positioning the input signal to +2 divisions using the CH 1 and CH 2 Preamplifier balance control. The trigger level is then determined by binary search using the same routine which is used for trigger offset. The same is done for −2 divisions. These results are then used to compute the trigger gain. Trigger Gain for the External Triggers is done in Extended Calibration of the TRIGGER circuits. A ground signal and externally supplied dc voltages are used to get a four-division level swing in both Ext Trig Preamp gain ranges. If gain cannot be measured, an error is flagged. On the External Triggers, a nominal gain value is stored if the test fails, on the assumption that the external setup may be faulty. The test(s) that failed will be marked FAIL in the Extended Diagnostic menu.
	Troubleshooting Procedure: 1. Run test 9200 in CONTINUOUS mode. 2. Starting with the signal path for ATG at pin 2 of A13U761 (schematic diagram 13), work backwards toward the trigger signal source using a test oscilloscope to check that the proper signals are present with the proper bias levels and voltage swings. 3. Use the troubleshooting comments under 9000 level as a guide. 4. The ATG signal should be present at TTL level voltage swings. 5. MAIN and DELAY GATE signals to Trigger Logic Array A10U370 (schematic diagram 11) should be present at ECL voltage level swings. 6. A TRIG LEVEL and B TRIG LEVEL signals, at pins 13 and 37 of A10U150 respectively, should have several levels: ±1 V swings, ±0.5 V swings, and voltage swing levels that approach a final level of gain iteratively as the binary search is done. 7. CH1 and CH2 TRIGGER signals should have two levels separated by 100 mV centered approximately around 0 V. (LR421/LR220 can be open and cause a FAIL flag to appear only at this diagnostic test level while the 9100 TRIGGER OFFSET level shows a PASS flag since that test only requires CH1/CH2 trigger signal to be near 0 V, which is the case with these components open.) 8. EXT1 and EXT2 TRIG signals are provided externally and this signal path to the Trigger Source Select function within A/B Trigger Generator U150 is not tested by running test 9200 in CONTINUOUS mode. If FAIL flags only appear at EXT diagnostic levels, the EXT source inputs of U150 are most likely functional and the problem is either External Trigger Preamp U100 and related bias circuitry, or the BNC and R1001/R1003 signal path from the front panel.

Table 6-6 (cont)

9300 REPET	This routine is not a test. Enough samples are acquired to calibrate the Jitter Correction Gain in Extended Calibration. Troubleshooting Procedure: 1. Use the Jitter Correction Troubleshooting procedure to locate the source of the failure.
8	**DEAD START**
POWER SUPPLIES	Low Voltage Power Supply (schematic diagram 22) and Low Voltage Regulators (schematic diagram 23): 1. Test for proper voltages on the SIDE BOARD. Check +15 V, +10 V, +8 V, +5 V, +5 V_D, −15 V, −10 V, −8.3 V Sense, −8 V, and −5 V for proper levels. If any of the voltages are incorrect, troubleshoot the bad supply. The +5 V_D supply is fused by F269 (schematic diagram 22) and the −15 V Unreg supply to the HV Oscillator is fused by F961 (schematic diagram 23). Both of these fuses are located under ribbon cables attaching to the power supply board and are hidden from view until the cables are disconnected. A Control Electronics Troubleshooting chart for the Low Voltage Power Supply is located in the "Diagrams" section of this manual. **WARNING** *If troubleshooting the Low Voltage Power Supply with the ac power connected, use of an isolation transformer is necessary to prevent damage to equipment and possible personal injury due to electrical shock.* 2. Check that PWRUP signal on U640 pin 2 is HI and that the $\overline{\text{RESET}}$ signal on U640 pin 37 is HI after the power on. If not, troubleshoot the Power Up (schematic diagram 23) and Power Up Reset circuitry (schematic diagram 1).
PROCESSOR CLOCKS	System Clocks (schematic diagram 7): 1. Check System μP A12U640 pin 38 (schematic diagram 1) for 8 MHz. If not there, check System Clocks for the defective component(s) (schematic diagram 7). Check that J132 (40 MHz oscillator/External clock jumper, schematic diagram 7) is properly installed. 2. Check Front Panel Processor A13U700 at pin 5 (schematic diagram 3) for the 4 MHz clock. If not there, check System Clocks for the defective clock circuit (schematic diagram 7). 3. Repair clocks. Go to the System Clock Troubleshooting chart (located in the "Diagrams" section of this manual). 4. If clocks are working, and the 2430 still gives no signs of life, use the System μP Kernel Test to verify operation of the System μP addressing and chip-select circuitry.
SYSTEM μP	System μP Aborts on Start-Up or While Operating: There is some internal consistency checking that can result in an "abort" of the operating routines. The abort routine loops endlessly, blinking the Trigger LEDs on and off in an abort code. On an abort, the Trigger LEDs are flashed three times, then an abort code is displayed in binary with the TRIG'D LED being the LSB of the code (see Figure 6-5), and the cycle is then repeated continually.

Table 6-6 (cont)

In version 1.7 software, an abort will cause the Trigger LEDs to flash, but no coded flashing is done. The abort codes for version 2 software and possible causes of an abort are shown in the following table:

CODE	Meaning	Possible Cause
1	Abort code initialized to this value at power-on.	Bad ROM/RAM. Firmware bug.
2	Unknown code received from Front Panel μP.	Front Panel μP data path to System μP bad.
3	Too many bytes received from Front Panel μP.	Front Panel μP data path to System μP bad or handshake logic bad.
4	Software Interrupt 2 or Software Interrupt 3 instruction executed.[a]	Bad ROM/RAM. Firmware bug.
5	GPIB terminator value for query response scrambled.	Bad ROM/RAM. Firmware bug. (May require a COLD START.)
6	GPIB event code to be reported is unknown.	Bad ROM/RAM. Firmware bug. (May require a COLD START.)
7	GPIB delimiter found by scanner has changed and is invalid.	Bad ROM/RAM. Firmware bug. (May require a COLD START.)

[a]SWI2 and SWI3 are not used in the software instructions. If executed, they were not as valid instructions.

Use the System μP Kernel Test to verify the ability of the System μP to function.

System μP A12U640 (schematic diagram 1) Kernel Test:

1. With the power off, move jumper J126 from pins 1 and 2 to pins 2 and 3 of P126. This disables the System μP Data Bus Driver, and allows the data bus lines to be pulled up and down to a single-byte instruction. The instruction (CLRB) continually fetches and executes the CLRB instruction to step through the entire 64 K of addresses.

2. Move jumper J127 (Waveform Processor Bus control) from the NORMAL position (pins 1 and 2 connected) to the BUSTAKE position (pins 2 and 4 connected). This places the Waveform Processor Bus under control of the System μP. In the mode, the basic operation of the System μP can be checked, and all the address decoding circuitry can be verified.

3. Connect CH 1 of a test scope to TP840. Display that signal and use it as a trigger source for the test scope. This point is the AF address bit (the MSB) of the address bus.

4. Turn the power on and check that the $\overline{\text{RESET}}$ signal on U844 pin 8 is HI; if not, troubleshoot the Power Up Reset circuitry (schematic diagram 1) and the Power Up circuitry (schematic diagram 23).

5. Adjust the test scope to view the AF signal. It should be a TTL-level square wave with a 50% duty cycle.

Table 6-6 (cont)

Using the CH 2 probe:

6. Check each address line in order (from AF to A0) for a valid TTL-level signal, with each lower address line having a frequency of exactly twice the frequency as the address above it. Any loss of the 50% duty cycle and/or distortion indicates a shorted address line. Check both the input and output pins of Address Buffers U732 and U632 to verify that they are working correctly, and to determine if address lines are shorted after the buffers. Waveform numbers 6, 7, 8, 9, 10, and 11 on schematic diagram 1 may be used to compare against the observed waveforms.

7. If a fault is found, if may be necessary to isolate the System μP address bus from the Waveform μP address bus to determine what circuitry is causing the problem. See the BUS ISOLATE and the WAVEFORM μP KERNEL MODE procedures following the SYSTEM μP CHIP SELECT TEST.

System μP Chip-Select Test:

1. From the Kernel mode, momentarily short the pins of J129 together to reset the processor. This forces ROM0.0 to be switched in. Set the test scope to 10 ms/div to view one whole cycle of the AF period, and set the Trigger Slope so that AF is shown LO during the first half of the display. While AF is LO, addresses from 0000h to 7FFFh are being executed; while HI, addresses from 8000h to FFFFh are executed.

2. Move jumper J127 (shown on schematic diagram 2) to connect pins 2 and 4. This causes the "BUSTAKE" condition so that the System μP has access to the Waveform μP memory space. In this mode, most of the processing system can be verified.

Using the CH 2 probe:

3. Look for a LO chip-select signal, at the point designated in the following table, that occurs during the correct portion of the AF waveform period. Waveforms 20, 21, 22, 23, 24, and 25, may be used as comparison waveforms for the chip selects output from Address Decoder U570 (schematic diagram 2—Waveform μP).

Chip Select	Test Point	Bus	Address Range (hex)	Position Within the AF Period
$\overline{\text{SAVE}}$	U580-8	WP	0000-1FFF	First 1/8th
$\overline{\text{DISP}}$	U570-13	WP	2000-2FFF	Third 1/16th
$\overline{\text{DATT}}$	U570-12	WP	3000-3FFF	Fourth 1/16th
$\overline{\text{ACQ}}$	U570-11	WP	4000-4FFF	Fifth 1/16th
CMD/$\overline{\text{TEMP}}$	U250-8	WP	5000-57FF	Twelfth 1/32nd
$\overline{\text{COEFF}}$	U250-11	WP	5800-5FFF	Thirteenth 1/32nd
$\overline{\text{HMMIO}}$	U870-6	BOTH	6000-6FFF	Seventh 1/16th
NVRAM	U840-6	SYS	7000-77FF	Sixteenth 1/32nd
$\overline{\text{SYSRAM}}$	U840-3	SYS	7800-7FFF	Seventeenth 1/32nd
$\overline{\text{ROM0.X}}$	U890-4	SYS	8000-BFFF	Third 1/4th
$\overline{\text{ROM1}}$	U890-5	SYS	C000-FFFF	Last 1/4th

Table 6-6 (cont)

4. Check the host memory-mapped I/O selects at the outputs of U830 to verify that selects are generated and only during the time $\overline{HMMIO}$ is LO.

5. With the power off, check that no two of the select outputs are shorted together. If shorted, troubleshoot the cause and repair.

NOTE

If the problem is that one of the selects is not being generated, the SELF TEST will be able to determine that a group of registers fail. However, if two or more of the select lines are shorted together, any addressed devices will try to respond at the same time and bus contention will occur. The result is that the normal SELF TEST diagnostics testing won't work.

6. Check each of the System μP data bus lines (D7-D0) on the outputs of Data Bus Buffer U650. Look for open bus lines (no activity) and hung bus lines (stuck HI or LO). If a fault is found, it will be necessary to determine if it is on the System Bus or the Waveform μP bus. Use the BUS ISOLATE mode to assist in checking for a fault location.

BUS ISOLATE MODE

1. Move jumper J127 to the BUS ISOLATE position (pins 2 and 4 connected). This electrically disconnects the Waveform μP bus from the System μP bus to isolate the different parts of the processing system from each other.

2. Recheck the faulty data bus line to determine if it is still faulty (problem on the System μP data bus) or the fault is gone (problem on the Waveform μP data bus).

3. Check that no data bus activity is occurring during the Waveform μP address space (see Figure 6-10 to compare against). Faulty address decoding can cause response from an incorrectly addressed device.

4. Check that the data bus is at the "float" level during periods of inactivity (waiting for a response from devices that are on the Waveform μP bus). A HI or a LO in the idle period indicates a stuck data bus.

5. If no faults are found on the System μP data bus, the problem data line may be on the Waveform μP bus. Use the Waveform μP Kernel mode to check for faults while the busses are isolated.

Table 6-6 (cont)

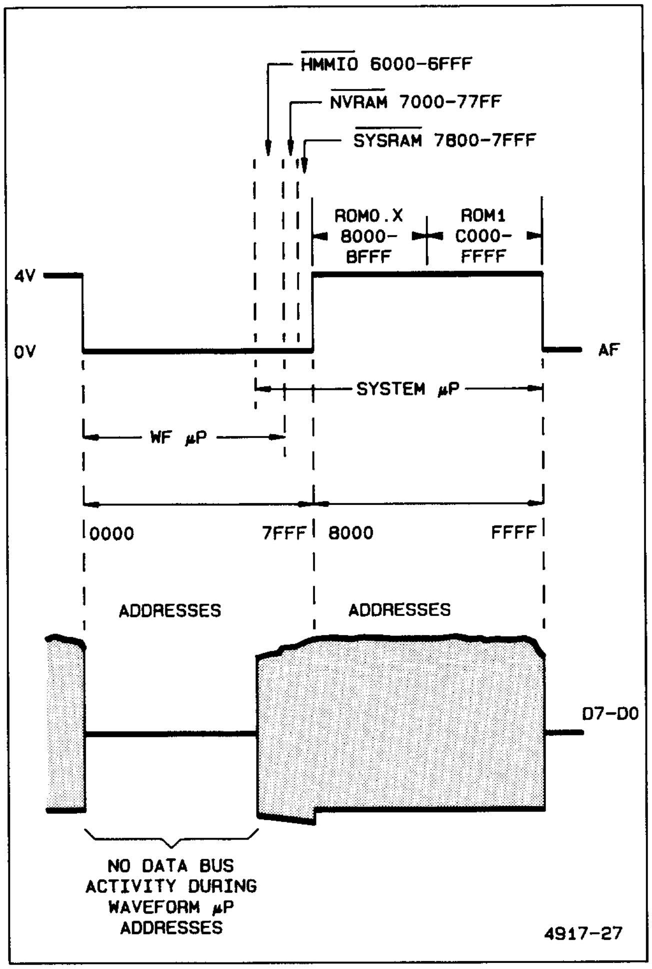


Figure 6-10. System μP data bit D7 in the Bus Isolate mode.

Table 6-6 (cont)

WAVEFORM μP

Waveform μP Kernel Mode:

This mode is used when a fault has been found on either the System μP data bus or the System μP address bus while in the BUS CONNECT mode or when SELF TEST 5100 (RUN TASK) fails in the Extended Diagnostics menu.

1. Turn off the power and place the processor system in the BUS ISOLATE mode (see the preceding steps).

2. Remove jumper J128 (Waveform μP Kernel Mode) and jumper J184 (Waveform μP Reset Release). Both are located on the Processor board near Waveform μP U470.

3. With the power on in the Kernel mode, the Instruction Data Bus lines are pulled up or pulled down in a command that causes the U470 to address every instruction in its memory sequentially and continually. Instruction address bus lines and data address bus lines can be checked for activity. All the Instruction address bus lines and the data address bus lines with the exception of the top five (WAA through WAE) increment with the periods shown in the following tables. WAA through WAE will be fixed random values because page switching of the memory is not done and is not set to any known state in the Kernel test.

Waveform μP Instruction Bus Address Lines

Signal	Location	Period
IA9	TP580	409.6 μs
IA8	U490-22	204.8 μs
IA7	U490-23	102.4 μs
IA6	U490-1	51.2 μs
IA5	U490-2	25.6 μs
IA4	U490-3	12.8 μs
IA3	U490-4	6.4 μs
IA2	U490-5	3.2 μs
IA1	U490-6	1.6 μs
IA0	U490-7	800 ns
CLK2D	U490-8	200 ns

Waveform μP Data Bus Address Lines

Signal	Location	Period
WAB	U562-9	1.6384 ms
WAA	TP562	819.2 μs
WA9	U562-5	409.6 μs
WA8	U562-2	204.8 μs
WA7	U364-19	102.4 μs
WA6	U364-16	51.2 μs
WA5	U364-15	25.6 μs
WA4	U364-12	12.8 μs
WA3	U364-9	6.4 μs
WA2	U364-6	3.2 μs
WA1	U364-5	1.6 μs
WA0	U364-2	800 ns

4. The Instruction Memory Data lines into the Waveform μP can also be checked to determine if any of the lines are shorted or open. Check against the schematic to see which lines (ID0 through IDF) are normally pulled up or normally pulled down for the Kernel test.

Table 6-7

Video Option Troubleshooting

VIDEO OPTION FAULT	Video Option (schematic diagram 21): If SET TV is pressed and an error message of "TV OPTION NOT INSTALLED OR FAULTY" is displayed, then the power-on SELF TEST has detected a problem (assuming the Video Option is installed). During the power-on SELF TEST, a byte is written to Line Counter A12U530 (schematic diagram 21) and read back. If the byte read back is not what is expected, a flag is set to indicate that the test failed. When the SET TV button is pressed, that flag is checked to see if the Video Option checked ok at power-up. If the test was not ok, the error message is displayed and the warning bell is sounded. If no error message is displayed, but test 2180 (FLD2) fails either at power-on or during a subsequent SELF TEST, troubleshoot as indicated in Table 6-6 Procedure 7 "Extended Diagnostics" for that failure.
	Troubleshooting Procedure: 1. Check A12U830 pin 3 (schematic diagram 1) for two negative strobes about 10.5 μs apart. (Viewing scope Sec/Div at 2 μs, trigger on negative slope of the signal.) If not present, replace U830. **NOTE** *The $\overline{GPIBSEL}$ signal also selects the Video Option registers. If communication via the GPIB interface is ok, then the select signals to Data Bus Buffer U532 (schematic diagram 20) and the buffer itself are ok. Suspect a problem with Programmable Line Counter U530 (schematic diagram 21).* 2. Check U332C pin 8 (schematic diagram 20) for the same negative strobes as at U830 pin 3. If not present, replace U332. 3. Check pins 2, 3, 4, 5, 6, 7, 8, and 9 of Data Bus Buffer U532 for activity (not stuck HI or LO) occurring at the same time as the negative strobe on U332C pin 8. If stuck, troubleshoot the bad bus line. 4. Check that pin 14 of U530 is at +5 V and that pin 1 is ground. If not, troubleshoot the cause. 5. Check that pin 8 of U530 is HI and that activity is occurring on pins 10, 11, 12, 13, 15, 16, and 17. If no activity, troubleshoot the problem. 6. If all inputs to U530 ok, replace U530.

Table 6-7 (cont)

TV TRIGGER PROBLEM

Auto triggering or unstable trigger in TV CPLG:

INITIAL SETUP:

Apply a negative-sync, flat-field, video signal to the CH 2 input. Select the correct protocol (System M or Nonsystem M) for the applied signal using the Extended Functions menus.

Set the following controls:

SLOPE/SYNC	– (negative sync)
VERTICAL MODE	CH 2
TRIGGER MODE	AUTO LEVEL
TRIGGER CPLG	TV
TRIGGER SOURCE	CH 2
SEC/DIV	20 μs
A TRIGGER HO	0 (no HO symbol displayed)
VOLTS/DIV	1 V

Press SET TV and select:

A TV COUPLING	TV LINE
CLAMP	OFF

1. Check the $\overline{\text{TVTG}}$ signal at U524B pin 8. If signal is present and no triggering is occurring, troubleshoot the Trigger Logic Array, A10U370 (schematic diagram 11).
2. If signal is absent, check the ATHO signal line at U424C pin 5 for HI-to-LO and LO-to-HI transitions. If not there, troubleshoot the Holdoff circuit (schematic diagram 13) as indicated in Table 6-6 in "HOLDOFF PROBLEMS".
3. If the ATHO signal is ok, check U424C pin 6 for an inverted ATHO signal; if not present, replace U424.
4. Check that U541B pin 6 has a positive pulse coincident with ATHO transitions. If not, replace U541.
5. Check that U524A pin 5 has a positive pulse coincident with the ATHO transitions. Check that U524A pin 3 is HI. If pin 3 is HI and pin 5 does not follow the ATHO transitions, replace U524.
6. Check pin 8 of U524B for a negative ($\overline{\text{TVTG}}$) pulse coincident with the LO-to-HI ATHO transitions. If not present, check that the TVENA signal on pin 12 is HI and that the HORIZCLK input on pin 11 (see waveform 163) is ok. If those signals are correct, replace U524; if not correct, troubleshoot the source of the problem.
7. Check the test waveforms shown for schematic diagram 21 (waveforms 159 through 168). Troubleshoot the circuitry indicated by an incorrect waveform (see the following troubleshooting procedures).

Table 6-7 (cont)

SIGNAL PROCESSING PROBLEM

See INITIAL SETUP in TV Trigger Problem for control settings and signal application. Set the test scope Sec/Div setting to 5 μs and the Volts/Div to 2 V.

1. Check U610 pin 5 for a horizontal line sync signal having the negative sync tip at about 0.5 V and a back-porch level of +4.5 V. If correct, check pin 6 of U420B for the correct signal (see waveform 162). If not correct there, troubleshoot the Sync Pickoff Comparator (Q504 and Q510) and Pulse Stretcher circuits.
2. Check that U750 pin 16 (schematic diagram 20) is LO with negative sync selected and HI with positive sync selected. If not, troubleshoot U750.
3. Is the TVRC signal present at U612 pin 3 (waveform 159)? If not, troubleshoot the source of the TVRC signal (Q140 and U150) and the connecting signal path.
4. Set the Input Coupling on the 2430 to GND and check that the dc levels at U612 pins 3 and 13 are about the same. If not, troubleshoot U710B and associated circuitry.
5. Set the Input Coupling to DC and check that the negative sync tip amplitude at U610 pin 9 is about 50 to 75 mV (from back-porch level to negative tip) with about a −3 V dc offset. If yes, the AGC amplifier and Sync Tip Clamp circuit are ok. Troubleshoot the Fixed Gain Amplifier, the Sync Pickoff Comparator, the Trigger Back-Porch Clamp, and associated circuitry. If the signal is not correct at pin 9 of U610 with the correct TVRC signal applied, troubleshoot the AGC amplifier and Sync Tip Clamp, and associated feedback circuitry.
6. Set Input Coupling to GND and check that U510 pin 6 is within 1 V of ground level. If not, troubleshoot U510 and associated circuitry.

PHASE-LOCKED LOOP PROBLEM

1. Set the Trigger CPLG to TV, Trigger SOURCE to CH 2, Trigger SLOPE to − (neg-sync), A TV COUPLING to FIELD1—Line count to 10, CH 2 input coupling to DC, SEC/DIV to 200 μs, TV CLAMP OFF, and VOLTS/DIV to 1 V (for a two-division signal amplitude). Connect a negative sync composite video signal to the CH 2 input.
2. Check pin 13 of U314 for narrow positive pulses that coincide with the horizontal sync pulses of the applied video signal. If not present, suspect the Phase Locked Loop circuitry and its input and output signals.
3. Check Q330, CR324, CR326, CR325, and VR234 for opens or shorts.
4. Check U308B pin 3 for a LO pulse coincident with the Horizontal Sync of the applied video signal. If not present, check for the presence of the $\overline{\text{COMPSYNC}}$ signal at U310A pin 5 (waveform 169). If $\overline{\text{COMPSYNC}}$ is ok, but the signal at U308B pin 3 is not, troubleshoot U420 and associated circuitry. If both are missing, troubleshoot back through the Video Option input and signal processing circuitry to find the problem.
5. Check the following signals: 2XH at U314 pin 4, $\overline{\text{2XH}}$ at U308A pin 9, $\overline{\text{HORIZCLK}}$ at U220B pin 12, HCLK at U220B pin 13, DLY'D HCLK at U220A pin 1 (held LO when the PLL is unlocked), VERTSYNC at U310A pin 1. Troubleshoot the cause of any missing signals. (See Figure 3-14 in Section 3 for typical waveforms.)

Table 6-7 (cont)

INCORRECT LINE COUNTING

See INITIAL SETUP in TV Trigger Problem for control settings and signal application. Set the test scope Sec/Div setting to 5 μs and the Volts/Div to 2 V.

1. Check that the correct protocol and Counter Restart choices are selected for the applied Video signal. (TV OPT under the EXTENDED FUNCTIONS—SYSTEM choices.)
2. Check that the $\overline{\text{HORIZCLK}}$ signal at U220B pin 12 is stable. If not, troubleshoot that problem.
3. Check that the FIELD signal at U424E pin 13 is stable and correct (waveform 164). If not, troubleshoot that problem. (Is the trigger signal amplitude excessive, causing erratic triggering?)
4. If the FIELD and $\overline{\text{HORIZCLK}}$ signals are ok, suspect a problem with Line Counter U530, NAND-gate U541, or U424.
5. Check that the FLD1 signal at U541 is HI when FLD1 is selected and alternates HI-to-LO when ALT is selected. If not, troubleshoot A12U750 (schematic diagram 20). (This assumes that the FLD2 diagnostic test passed the power-on diagnostics.)
6. Check Line Counter outputs at pin 27 and pin 3 for a LO-to-HI transition during the vertical sync pulse time. (View the composite video on channel 2 of the test scope and use the channel 1 probe to check the signal at pin 27 and pin 3. Trigger the test scope on the channel 1 signal. Use delayed sweep to view the signals if using an analog test scope.)
7. If not correct, replace U530.
8. Check that the clock at pin 8 of U424D is stable and has a LO-to-HI transition. If no transition, replace U424.

TV CLAMP PROBLEM

NOTE

The Video Option must have a composite-sync or composite-video signal source applied for the Channel 2 Display Clamp to function properly. Clamping action is unpredictable if an incorrect signal is applied. The TV CLAMP circuit remains on, even if TV COUPLING is not selected and may be used to clamp a Channel 2 display if the selected trigger source signal is a composite-sync or composite-video signal.

1. Set the Trigger CPLG to TV, Trigger SOURCE to CH 2, Trigger SLOPE to – (neg-sync), A TV COUPLING to FIELD1—Line count to 50, CH 2 input coupling to DC, SEC/DIV to 5 μs, TV CLAMP OFF, and VOLTS/DIV to 1 V (for a two-division signal amplitude). Connect the negative sync composite video signal to the CH 2 input in series with a dc offset voltage source. Set the offset level for 0 V offset.
2. Is the display triggered and stable? If not, the TV CLAMP circuit will not be properly enabled in any case, and some other problem may exist. Check that the collector of Q330 is LO. If not LO, either the PLL (U314) is not locked or Q330 or its associated circuitry is defective; go to PHASE-LOCKED LOOP PROBLEM troubleshooting.
3. If the display is triggered correctly, check that the back-porch level of the displayed video signal is at approximately ground level. If not, run SELF CAL and check again. If there is a large offset present, troubleshoot CH 2 Preamp U320 and U230 (schematic diagram 9).
4. Set the offset voltage for –1.5 V offset, and verify that the back-porch level is offset from ground –1.5 V.
5. Set TV CLAMP ON. Is the back-porch level clamped to ground level? If so, the TV clamp is functioning.

Table 6-7 (cont)

6. Did the CH 2 signal display change vertical position by any amount when TV CLAMP was turned on? If not, check that BPCLAMP is HI with TV CLAMP ON. Troubleshoot A12U750 (schematic diagram 20) if not correct.
7. Check that pin 3 of U410A has a 10 V positive pulse at the beginning of the back porch of the applied video signal (waveform 165). If not, troubleshoot U410A and associated components.
8. Set the test scope BW Limit to 20 MHz and the Volts/Div to 50 mV. Check U520 pin 3 for a CH 2 PO signal that is a replica of the applied video signal. If not present, troubleshoot the CH 2 Preamplifier Pickoff circuitry and the signal path between it and pin 3.
9. Check that pin 6 of U520 is approximately 0 V with the TV CLAMP OFF and approximately −130 mV with the TV CLAMP ON. If not switching correctly between CLAMP ON and CLAMP OFF, troubleshoot U410C, Q420, and U520.
10. Switch CH 2 INVERT ON check pin 6 of U520 again as in step 9. If not correct, troubleshoot U514, U410B, U410E and the CH 2 INV signal (should be HI with CH 2 INVERT ON).
11. Check U710D pin 14 for approximately 0 V with CLAMP OFF and approximately −130 mV with CLAMP ON. If not correct, replace U710. Check that the Source of Q710 follows pin 14 of U710D for CLAMP ON and CLAMP OFF. If not, troubleshoot Q710, U710A, and associated components.

Pressing the INIT PANEL button in the SAVE/RECALL SETUP control menu sets up all the front-panel controls and menu selection in the predefined states shown in Table 6-8.

Table 6-8

INIT PANEL States

STORAGE Mode Controls	
STORAGE Mode	ACQUIRE
ACQUIRE Mode	NORMAL
REPET	OFF
AVG Number	2
ENVELOPE Number	1
SAVE ON Δ	OFF
REF1 through REF4	OFF
DELAY Controls	
DELAY by EVENTS	OFF
Δ TIME	OFF
DELAY TIME	40 μs
Δ DELAY Time	0.0
DELAY EVENTS Nr.	1

Table 6-8 (cont)

HORIZONTAL Mode Controls	
MODE	A
A SEC/DIV	1 ms
EXT CLK Expansion Factor	1
EXT CLK	OFF
POSITION Waveform	LIVE
POSITION Reference	REF 1
POSITION set to	Midscreen
VERTICAL MODE Controls	
CH 1	ON
VOLTS/DIV (both)	100 mV
VARIABLE (both)	CAL
COUPLING (both)	DC
50 Ω (both)	OFF
INVERT (both)	OFF
POSITION set to	Midscreen
Display Mode	YT
BANDWIDTH	FULL

Table 6-8 (cont)

INTENSITY Controls	
SELECT	DISP
DISP Intensity	40%
READOUT Intensity	50%
GRAT Illum	0%
INTENS Level	80%
VECTORS	ON
WORD RECOGNIZER (SET WORD)	
Word Match	Don't Care (all x)
RADIX	HEX
CLOCK	ASYNC
CURSOR Controls	
CURSOR/DELAY Knob	CURSOR POSITION
CURSOR FUNCTION	All off
VOLTS UNITS	VOLTS
TIME UNITS	SEC
SLOPE UNITS	VOLTS/SEC
CURSOR Mode	Δ
ATTACH CURSORS TO:	CH 1
X-Axis Cursor Position	±3 divisions
Y-Axis Cursor Position	±3 divisions
TIME Cursor Position	±4 divisions
VOLTS Ref Value	1.0 V
TIME Ref Value	1.0 SEC
SLOPE Ref Value	1.0 V/SEC
GPIB SETUP (OUTPUT)	
DEBUG	OFF
LONG	ON
PATH	ON
RQS Mask	ON
OPC Mask	ON
CER Mask	ON
EXR Mask	ON
EXW Mask	ON
INR Mask	ON
USER Mask	OFF
PID Mask	OFF
DEVDEP Mask	OFF
Data Encoding (ENCDG)	RPBINARY
Data Target	REF 1
Data Source	CH 1
FASTXMIT	OFF
CURVE ONLY	OFF

Table 6-8 (cont)

TRIGGER Controls	
A/B TRIG set for	A
A TRIG MODE	AUTO LEVEL
B TRIG MODE	RUNS AFTER
SOURCE (both)	CH 1
COUPLING (both)	DC
SLOPE (both)	+ (plus)
TRIG POSITION	1/2 (512)
LEVEL (both)	0.0
EXT GAIN (both)	÷1
HOLDOFF	Minimum
VIDEO OPTION Setup (SET TV)	
Interlaced Coupling	FIELD1
Noninterlaced Coupling	FIELD1
TV SYNC	− (minus)
CLAMP	OFF
Line Count	525
Line Start	Prefld
X-Y PLOTTER Setup (OUTPUT)	
Plot Graticule	ON
Plot Readout	OFF
PENLIFT	OPEN

OPTIONS AND ACCESSORIES

OPTIONS DESCRIPTION

This section contains a general description of available options for the 2430 Digital Storage Oscilloscope at time of manual publication. The options are:

Options A1-A5	International Power Cords
Option 1R	Rackmounting
Option 05	Video Option
Option 11	Probe Power

Operating instructions for the Video Option and the Word Recognizer Probe optional accessory are found in the Options Section of the 2430 Operators Manual. A complete list of standard accessories supplied with the instrument and a list of suggested optional accessories, each identified by part number, is included in this section.

Additional information about instrument options, option availability, and other accessories can be obtained from the current Tektronix Products Catalog or by contacting /our local Tektronix Field Office or representative.

OPTIONS A1-A5 INTERNATIONAL POWER CORDS

Instruments are shipped with the detachable power-cord configuration ordered by the customer. Descriptive information about the international power-cord options is provided in Section 2, "Preparation for Use." The following list identifies the Tektronix part number for the available power cords.

Option A1 (Universal Euro)	
Power cord (2.5 m)	161-0104-06
Option A2 (UK)	
Power cord (2.5 m)	161-0104-07
Option A3 (Australian)	
Power cord (2.5 m)	161-0104-05
Option A4 (North American)	
Power cord (2.5 m)	161-0104-08
Option A5 (Switzerland)	
Power cord (2.5 m)	161-0154-00

OPTION 1R RACKMOUNTED 2430

When the 2430 Digital Oscilloscope is ordered with Option 1R, it is shipped in a configuration that permits easy installation into a 19-inch-wide equipment rack. An optional rackmounting kit may be ordered to convert the standard 2430 to a rackmounted instrument. Installation instructions for rackmounting are provided in the documentation supplied with the rackmounting kit and the 1R Option.

The rear-support kit also is supplied for use when rackmounting the 2430. Using this rear-support kit enables the rackmounted instrument to meet all electrical and environmental specifications of the standard 2430.

Connector-mounting holes are provided in the front panel of the rackmounted instrument. These holes enable convenient accessing of the rear panel BNC connectors and directing the Vertical Channel and External Trigger input connectors to rear access in an electronics equipment rack. The selection of signals that are routed through the rackmounting front panel is left to the user. Additional cabling and connectors required to implement any through-panel access must be user supplied; however, the necessary items may be separately ordered from Tektronix, Inc.

OPTION 05 VIDEO OPTION

Option 05 provides an aid in examining composite video signals. With the Video Option installed, all basic instrument functions remain the same. Changes to any of the control menus by the installation of Option 05 are detailed in the description of the affected menus in Section 3 of the Operators Manual, "Controls, Connectors, and Indicators." Features of this option include a sync separator, back-porch clamp circuitry, TV trigger coupling modes, and adjustment for closer tolerance on the 20 MHz BANDWIDTH LIMIT. This option permits the user to trigger on a specific line number within a TV field and provides sync-polarity switching for either sync-negative or sync-positive composite video signals. Circuit descriptions and schematics for the Video Option are located in the appropriate sections in this Service Manual.

OPTION 11
PROBE POWER

Option 11 provides two probe-power connectors on the rear panel of the instrument. Voltages supplied at the PROBE POWER connectors meet the power requirements of standard Tektronix active oscilloscope probes.

OPTIONAL WORD RECOGNIZER PROBE ACCESSORY

The Word Recognizer Probe optional accessory is used to obtain triggering on a selected parallel TTL data word. A word length of 16-bits plus a 17th qualifier bit is recognizable, with each bit selectable as 0, 1, or X (don't care). Recognition may be either synchronous with an external clock signal (rising or falling edge) or asynchronous. All the required hardware and firmware for using the Word Recognizer Probe is included in the standard 2430 Digital Oscilloscope; it is only necessary to purchase the Word Recognizer Probe optional accessory. More specific information on the Word Recognizer Probe, including electrical specification, is provided in the Instruction Sheet supplied with the probe. Operating instructions for use of the word recognition capabilities of the 2430 are included in the 2430 Operators Manual in both Section 3 (Controls, Connectors, and Indicators) and Section 7 (Options and Accessories).

STANDARD ACCESSORIES

The following standard accessories are provided with each instrument.

	Part Number
2 Probes, 10X, 1.3 meter, with accessories	P6133
1 Accessory pouch, snap	016-0692-0(
1 Accessory pouch, ziploc	016-0537-00
1 Operators manual	070-4918-00
1 Instrument Interfacing guide	070-5705-00
1 User Reference guide	070-5497-00
1 Fuse, 5 A, 250 V, AGC/3AG	159-0014-00
1 Crt filter, blue plastic (installed)	378-0199-03
1 Crt filter, clear plastic	378-0208-00
1 Front cover	200-2742-00
1 CCIR graticule (with Video option)	378-0199-00
1 NTSC graticule (with Video option)	378-0199-05

RACKMOUNTING ACCESSORIES

The following accessories are available to rackmount an instrument that is not purchased as a 1R option.

	Part Number
Rackmounting conversion kit	016-0825-00
Rackmounting rear-support kit (included in the conversion kit)	016-0096-00

OPTIONAL ACCESSORIES

The following optional accessories are recommendec for use with the 2430 Digital Oscilloscope.

	Part Number
Service manual	070-4917-00
Word Recognizer probe	010-6407-01
Oscilloscope camera	
C-5C Option 01 or	016-0357-01
C7 Option 03 with Option 30	016-0799-01
SCOPE-MOBILE cart	K212
Carrying strap	346-0058-00

REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

CROSS INDEX-MFR. CODE NUMBER TO MANUFACTURER

The Mfr. Code Number to Manufacturer index for the Electrical Parts List is located immediately after this page. The Cross Index provides codes, names and addresses of manufacturers of components listed in the Electrical Parts List.

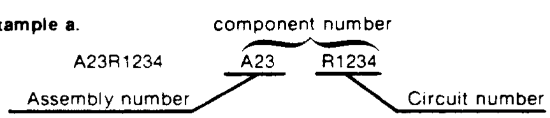
ABBREVIATIONS

Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the Electrical Parts List)

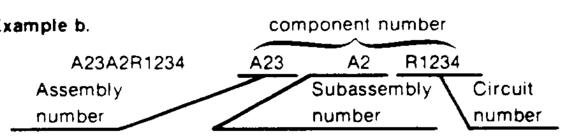
A numbering method has been used to identify assemblies, subassemblies and parts. Examples of this numbering method and typical expansions are illustrated by the following:

Example a.



Read: Resistor 1234 of Assembly 23

Example b.



Read: Resistor 1234 of Subassembly 2 of Assembly 23

Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the Mechanical Parts List. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

TEKTRONIX PART NO. (column two of the Electrical Parts List)

Indicates part number to be used when ordering replacement part from Tektronix.

SERIAL/MODEL NO. (columns three and four of the Electrical Parts List)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

NAME & DESCRIPTION (column five of the Electrical Parts List)

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

MFR. CODE (column six of the Electrical Parts List)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

MFR. PART NUMBER (column seven of the Electrical Parts List)

Indicates actual manufacturers part number.

CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
00213	NYTRONICS COMPONENTS GROUP INC SUBSIDIARY OF NYTRONICS INC	ORANGE ST	DARLINGTON SC 29532
00779	AMP INC	2800 FULLING MILL PO BOX 3608	HARRISBURG PA 17105
00853	SANGAMO WESTON INC COMPONENTS DIV	SANGAMO RD PO BOX 128	PICKENS SC 29671-9716
01121	ALLEN-BRADLEY CO	1201 S 2ND ST	MILWAUKEE WI 53204-2410
01281	TRW ELECTRONICS AND DEFENSE SECTOR RF DEVICES	14520 AVIATION BLVD	LAWNDALE CA 90260-1121
01295	TEXAS INSTRUMENTS INC SEMICONDUCTOR GROUP	13500 N CENTRAL EXP PO BOX 655012	DALLAS TX 75265
01537	MOTOROLA COMMUNICATIONS AND ELECTRONICS INC	2553 N EDGINGTON ST	FRANKLIN PARK IL 60131-3401
02113	COILCRAFT INC	1102 SILVER LAKE RD	CARY IL 60013-1658
02735	RCA CORP SOLID STATE DIVISION	ROUTE 202	SOMERVILLE NJ 08876
03508	GENERAL ELECTRIC CO SEMI-CONDUCTOR PRODUCTS DEPT	W GENESEE ST	AUBURN NY 13021
03888	PYROFILM DIV DIV OF KDI ELECTRONICS INC	60 S JEFFERSON RD	WHIPPANY NJ 07981-1001
04222	AVX CERAMICS DIV OF AVX CORP	19TH AVE SOUTH P O BOX 867	MYRTLE BEACH SC 29577
04713	MOTOROLA INC SEMICONDUCTOR PRODUCTS SECTOR	5005 E MCDOWELL RD	PHOENIX AZ 85008-4229
05292	ITT COMPONENTS DIV		CLIFTON NJ
05397	UNION CARBIDE CORP MATERIALS SYSTEMS DIV	11901 MADISON AVE	CLEVELAND OH 44101
05828	GENERAL INSTRUMENT CORP GOVERNMENT SYSTEMS DIV	600 W JOHN ST	HICKSVILLE NY 11802
06665	PRECISION MONOLITHICS INC SUB OF BOURNS INC	1500 SPACE PARK DR	SANTA CLARA CA 95050
07263	FAIRCHILD SEMICONDUCTOR CORP NORTH AMERICAN SALES SUB OF SCHLUMBERGER LTD MS 118	10400 RIDGEVIEW CT	CUPERTINO CA 95014
07716	TRW INC TRW IRC FIXED RESISTORS/BURLINGTON	2850 MT PLEASANT AVE	BURLINGTON IA 52601
09019	GENERAL ELECTRIC CO POWER ELECTRONICS SYSTEMS DEPT	ELECTRONICS PARK BLDG 7	SYRACUSE NY 13221
09922	BURNDY CORP	RICHARDS AVE	NORWALK CT 06852
11236	CTS CORP BERNE DIV THICK FILM PRODUCTS GROUP	406 PARR ROAD	BERNE IN 46711-9506
12697	CLAROSTAT MFG CO INC	LOWER WASHINGTON ST	DOVER NH 03820
12954	MICROSEMI CORP - SCOTTSDALE	8700 E THOMAS RD P O BOX 1390	SCOTTSDALE AZ 85252
12969	UNITRODE CORP	5 FORBES RD	LEXINGTON MA 02173-7305
14298	INSILCO CORP ACIC DIV	PAMLICO BLDG SUITE 209 3306 EAST CHAPEL HILL NELSON HWY	RESEARCH TRIAGLE PARK NC 27709
14552	MICROSEMI CORP	2830 S FAIRVIEW ST	SANTA ANA CA 92704-5948
14752	ELECTRO CUBE INC	1710 S DEL MAR AVE	SAN GABRIEL CA 91776-3825
15454	AMETEK INC RODAN DIV	721 N POPLAR ST	ORANGE CA 92668
15513	DATA DISPLAY PRODUCTS	301 CORAL CIR	EL SEGUNDO CA 90245-4620
15636	ELEC-TROL INC	26477 N GOLDEN VALLEY RD	SAUGUS CA 91350-2621
17856	SILICONIX INC	2201 LAURELWOOD RD	SANTA CLARA CA 95054-1516
18324	SIGNETICS CORP MILITARY PRODUCTS DIV	4130 S MARKET COURT	SACRAMENTO CA 95834-1222
19701	MEPCO/CENTRALAB A NORTH AMERICAN PHILIPS CO MINERAL WELLS AIRPORT	PO BOX 760	MINERAL WELLS TX 76067-0760
20932	KYOCERA INTERNATIONAL INC	11620 SORRENTO VALLEY RD PO BOX 81543 PLANT NO 1	SAN DIEGO CA 92121
22526	DU PONT E I DE NEMOURS AND CO INC DU PONT CONNECTOR SYSTEMS DIV MILITARY PRODUCTS GROUP	515 FISHING CREEK RD	NEW CUMBERLAND PA 17070-3007

CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
24355	ANALOG DEVICES INC	RT 1 INDUSTRIAL PK PO BOX 9106	NORWOOD MA 02062
24546	CORNING GLASS WORKS	550 HIGH ST	BRADFORD PA 16701-3737
25088	SIEMENS CORP	186 WOOD AVE S	ISELIN NJ 08830-2704
27014	NATIONAL SEMICONDUCTOR CORP	2900 SEMICONDUCTOR DR	SANTA CLARA CA 95051-0606
31918	ITT SCHADOW INC	8081 WALLACE RD	EDEN PRAIRIE MN 55344-2224
32159	WEST-CAP ARIZONA	2201 E ELVIRA ROAD	TUCSON AZ 85706-7026
32997	BOURNS INC TRIMPOT DIV	1200 COLUMBIA AVE	RIVERSIDE CA 92507-2114
34335	ADVANCED MICRO DEVICES	901 THOMPSON PL	SUNNYVALE CA 94086-4518
50101	FREQUENCY SOURCES INC SEMICONDUCTOR DIV SUB OF LORAL CORP	16 MAPLE RD	CHELMSFORD MA 01824-3737
50434	HEWLETT-PACKARD CO OPTOELECTRONICS DIV	370 W TRIMBLE RD	SAN JOSE CA 95131
51406	MURATA ERIE NORTH AMERICA INC HEADQUARTERS AND GEORGIA OPERATIONS	2200 LAKE PARK DR	SMYRNA GA 30080
51642	CENTRE ENGINEERING INC	2820 E COLLEGE AVE	STATE COLLEGE PA 16801-7515
52763	STETTNER ELECTRONICS INC	6135 AIRWAYS BLVD PO BOX 21947	CHATTANOOGA TN 37421-2970
52769	SPRAGUE-GOODMAN ELECTRONICS INC	134 FULTON AVE	GARDEN CITY PARK NY 11040-5352
53387	MINNESOTA MINING AND MFG CO ELECTRONIC PRODUCTS DIV	3M CENTER	ST PAUL MN 55101-1428
54473	MATSUSHITA ELECTRIC CORP OF AMERICA	ONE PANASONIC WAY PO BOX 1501	SECAUCUS NJ 07094-2917
54583	TDK ELECTRONICS CORP	12 HARBOR PARK DR	PORT WASHINGTON NY 11550
54937	DEYOUNG MANUFACTURING INC	12920 NE 125TH WAY	KIRKLAND WA 98034-7716
55112	WESTLAKE CAPACITORS INC	5334 STERLING CENTER DRIVE	WESTLAKE VILLAGE CA 91361
55680	NICHICON /AMERICA/ CORP	927 E STATE PKY	SCHAUMBURG IL 60195-4526
56289	SPRAGUE ELECTRIC CO WORLD HEADQUARTERS	92 HAYDEN AVE	LEXINGTON MA 02173-7929
57668	ROHM CORP	16931 MILLIKEN AVE	IRVINE CA 92713
58224	XENELL CORP	11 DUNBARTON RD PO BOX 4401	CHERRY HILL NJ 08003-2107
59660	TUSONIX INC	7741 N BUSINESS PARK DR PO BOX 37144	TUCSON AZ 85740-7144
59821	MEPCO/CENTRALAB A NORTH AMERICAN PHILIPS CO	7158 MERCHANT AVE	EL PASO TX 79915-1207
60211	VOLTAGE MULTIPLIERS INC	8711 W ROOSEVELT	VISALIA CA 93291-9458
61545	AMP KEYBOARD TECHNOLOGIES INC SUB OF AMP INC	76 BLANCHARD RD PO BOX 543	BURLINGTON MA 01803-5125
62786	HITACHI AMERICA LTD	1800 BERING DRIVE	SAN JOSE CA 95122
71400	BUSSMANN DIV OF COOPER INDUSTRIES INC	114 OLD STATE RD PO BOX 14460	ST LOUIS MO 63178
71744	GENERAL INSTRUMENT CORP LAMP DIV/WORLD WIDE/	4433 N RAVENSWOOD AVE	CHICAGO IL 60640-5802
74970	JOHNSON E F CO	299 10TH AVE S W	WASECA MN 56093-2539
75042	IRC ELECTRONIC COMPONENTS PHILADELPHIA DIV TRW FIXED RESISTORS	401 N BROAD ST	PHILADELPHIA PA 19108-1001
76493	BELL INDUSTRIES INC JW MILLER DIV	19070 REYES AVE PO BOX 5825	COMPTON CA 90224-5825
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500 MS 53-111	BEAVERTON OR 97707-0001
81483	INTERNATIONAL RECTIFIER	9220 SUNSET BLVD	LOS ANGELES CA 90069-3501
81855	EAGLE-PICHER INDUSTRIES INC ELECTRONICS DIV	COUPLES DEPT C AND PORTER STS PO BOX 47	JOPLIN MO 64801
84411	AMERICAN SHIZUKI CORP OGALLALA OPERATIONS	301 WEST O ST	OGALLALA NE 69153-1844
91637	DALE ELECTRONICS INC	2064 12TH AVE PO BOX 609	COLUMBUS NE 68601-3632
93410	ESSEX GROUP ING CONTROLS DIV LEXINGTON PLANT	45-55 PLYMOUTH ST P O BOX 1007	LEXINGTON OH 44904
94617	BETTER COIL AND TRANSFORMER CORP	2001 W UNION	GOODLAND IN 47948
S4091	SANYO ELECTRIC CO LTD		OSAKA JAPAN

CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
TK0510	PANASONIC COMPANY DIV OF MATSUSHITA ELECTRIC CORP	ONE PANASONIC WAY	SECAUCUS NJ 07094
TK0515	RIFA INC	403 INTERNATIONAL PKY PO BOX 853904	RICHARDSON TX 75085-3904
TK0935	MARQUARDT SWITCHES INC	67 ALBANY ST PO BOX 465	CAZENOVIA NY 13035-1219
TK0946	SAN-O INDUSTRIAL CORP	170 WILBUR PL	BAHEMIA LONG ISLAND NY 11716
TK0987	TOPAZ SEMICONDUCTOR SUB OF HYTEK MICROSYSTEMS INC	1971 N CAPITOL AVE	SAN JOSE CA 95132-3799
TK1016	TOSHIBA AMERICA INC ELECTRONIC COMPONENTS DIV BUSINESS SECTOR	2692 DOW AVE	TUSTIN CA 92680
TK1066	STAR MICRONICS		
TK1345	ZMAN AND ASSOCIATES	7633 S 180TH	KENT WA 98032
TK1450	TOKYO COSMOS ELECTRIC CO LTD	2-268 SOBUDAI ZAWA	KANAGAWA 228 JAPAN
TK1544	COMPUTER CONNECTIONS	2427 PRATT AVE	HAYWARD CA 94544
TK1573	WILHELM WESTERMAN	PO BOX 2345 AUGUSTA-ANLAGE 56	6800 MANNHEIM 1 WEST GERMANY
TK2038	MULTICOMP INC	3005 SW 154TH TERRACE #3	BEAVERTON OR 97006
TK2042	ZMAN & ASSOCIATES	7633 S 180TH	KENT WA 98032

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Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A10	670-8163-00	B010100	B010321	CIRCUIT BD ASSY:MAIN	80009	670-8163-00
A10	670-8163-01	B010322	B010582	CIRCUIT BD ASSY:MAIN	80009	670-8163-01
A10	670-8163-02	B010583	B010808	CIRCUIT BD ASSY:MAIN	80009	670-8163-02
A10	670-8163-03	B010809	B011409	CIRCUIT BD ASSY:MAIN	80009	670-8163-03
A10	670-8163-04	B011410	B011848	CIRCUIT BD ASSY:MAIN	80009	670-8163-04
A10	670-8163-05	B011849	B012726	CIRCUIT BD ASSY:MAIN	80009	670-8163-05
A10	670-8163-06	B012727	B013501	CIRCUIT BD ASSY:MAIN	80009	670-8163-06
A10	670-8163-08	B013502	B014160	CIRCUIT BD ASSY:MAIN	80009	670-8163-08
A10	670-8163-09	B014161	B014161	CIRCUIT BD ASSY:MAIN	80009	670-8163-09
A10	670-8163-10	B014162	B014161	CIRCUIT BD ASSY:MAIN	80009	670-8163-10
A10	670-8163-11	B014162		CIRCUIT BD ASSY:MAIN	80009	670-8163-11
				(2430 ONLY)		
A10	670-8163-06	B010100	B010126	CIRCUIT BD ASSY:MAIN	80009	670-8163-06
A10	670-8163-09	B010127	B019999	CIRCUIT BD ASSY:MAIN	80009	670-8163-09
				(2430M ONLY)		
A11	670-8164-00	B010100	B010699	CIRCUIT BD ASSY:TIME BASE	80009	670-8164-00
A11	670-8164-01	B010700	B011145	CIRCUIT BD ASSY:TIME BASE	80009	670-8164-01
A11	670-8164-02	B011146	B014160	CIRCUIT BD ASSY:TIME BASE DISPLAY	80009	670-8164-02
A11	670-8164-03	B014161		CIRCUIT BD ASSY:TIME BASE	80009	670-8164-03
				(2430 ONLY)		
A11	670-8164-03	B010100	B010106	CIRCUIT BD ASSY:TIME BASE	80009	670-8164-03
A11	670-8164-04	B010107		CIRCUIT BD ASSY:TIME BASE	80009	670-8164-04
				(2430M ONLY)		
A12	670-8165-00	B010100	B012056	CIRCUIT BD ASSY:PROCESSOR	80009	670-8165-00
A12	670-8165-05	B012057	B014012	CIRCUIT BD ASSY:PROCESSOR	80009	670-8165-05
A12	670-8165-07	B014013		CIRCUIT BD ASSY:PROCESSOR	80009	670-8165-07
				(STANDARD ONLY) (DOES NOT INCLUDE FIRMWARE)		
A12	670-8165-01	B010100	B012303	CIRCUIT BD ASSY:PROCESSOR OPT 05	80009	670-8165-01
A12	670-8165-06	B012304	B014012	CIRCUIT BD ASSY:PROCESSOR OPT 05	80009	670-8165-06
A12	670-8165-08	B014013		CIRCUIT BD ASSY:PROCESSOR OPT 05	80009	670-8165-08
				(OPTION 05 ONLY)(DOES NOT INCLUDE FIRMWARE)		
A12	670-8165-03	B010100	B010104	CIRCUIT BD ASSY:PROCESSOR,STD,CIIL	80009	670-8165-03
A12	670-8165-05	B010105	B010139	CIRCUIT BD ASSY:PROCESSOR	80009	670-8165-05
A12	670-8165-07	B010140		CIRCUIT BD ASSY:PROCESSOR	80009	670-8165-07
				(2430M ONLY)(DOES NOT INCLUDE FIRMWARE)		
A13	670-8167-00	B010100	B010699	CIRCUIT BD ASSY:SIDE	80009	670-8167-00
A13	670-8167-01	B010700	B014161	CIRCUIT BD ASSY:SIDE	80009	670-8167-01
A13	670-9749-01	B014162		CIRCUIT BD ASSY:SIDE	80009	670-9749-01
				(2430 ONLY)		
A13	670-8167-01	B010100	B019999	CIRCUIT BD ASSY:SIDE	80009	670-8167-01
				(2430M ONLY)		
A14	670-8168-00	B010100	B010699	CIRCUIT BD ASSY:FRONT PANEL	80009	670-8168-00
A14	670-8168-01	B010700	B011236	CIRCUIT BD ASSY:FRONT PANEL	80009	670-8168-01
A14	670-8168-02	B011237	B012532	CIRCUIT BD ASSY:FRONT PANEL	80009	670-8168-02
A14	670-8168-03	B012533		CIRCUIT BD ASSY:FRONT PANEL	80009	670-8168-03
A16	670-8169-00	B010100	B010321	CIRCUIT BD ASSY:LV PWR SPLY	80009	670-8169-00
A16	670-8169-01	B010322	B013139	CIRCUIT BD ASSY:LV POWER SUPPLY	80009	670-8169-01
A16	670-8169-02	B013140	B013150	CIRCUIT BD ASSY:LVPS,CIIL	80009	670-8169-02
A16	670-8169-03	B013151		CIRCUIT BD ASSY:LV PWR SPLY	80009	670-8169-03
A17	670-8166-00	B010100	B010321	CIRCUIT BD ASSY:HV	80009	670-8166-00
A17	670-8166-01	B010322	B010699	CIRCUIT BD ASSY:HV	80009	670-8166-01
A17	670-8166-02	B010700	B013699	CIRCUIT BD ASSY:HV	80009	670-8166-02
A17	670-8166-04	B013700	B014160	CIRCUIT BD ASSY:HV	80009	670-8166-04
A17	670-9748-00	B014161		CIRCUIT BD ASSY:HV POWER SPLY	80009	670-9748-00
				(2430 ONLY)		
A17	670-8166-02	B010100	B010130	CIRCUIT BD ASSY:HV	80009	670-8166-02
A17	670-8166-04	B010131	B014160	CIRCUIT BD ASSY:HV	80009	670-8166-04
A17	670-9748-00	B014161		CIRCUIT BD ASSY:HV POWER SPLY	80009	670-9748-00
				(2430M ONLY)		
A18	670-8795-00	B010100	B010699	CIRCUIT BD ASSY:SCALE ILLUM	80009	670-8795-00
A18	670-8795-01	B010700	B014161	CIRCUIT BD ASSY:SCALE ILLUM	80009	670-8795-01
A18	670-7280-00	B014162		CIRCUIT BD ASSY:SCALE ILLUM	80009	670-7280-00

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
				(2430 ONLY)		
A18	670-8795-01	B010100	B019999	CIRCUIT BD ASSY:SCALE ILLUM	80009	670-8795-01
				(2430M ONLY)		

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A10	670-8163-00	B010100	B010321	CIRCUIT BD ASSY:MAIN	80009	670-8163-00
A10	670-8163-01	B010322	B010582	CIRCUIT BD ASSY:MAIN	80009	670-8163-01
A10	670-8163-02	B010583	B010808	CIRCUIT BD ASSY:MAIN	80009	670-8163-02
A10	670-8163-03	B010809	B011409	CIRCUIT BD ASSY:MAIN	80009	670-8163-03
A10	670-8163-04	B011410	B011848	CIRCUIT BD ASSY:MAIN	80009	670-8163-04
A10	670-8163-05	B011849	B012726	CIRCUIT BD ASSY:MAIN	80009	670-8163-05
A10	670-8163-06	B012727	B013501	CIRCUIT BD ASSY:MAIN	80009	670-8163-06
A10	670-8163-08	B013502	B014160	CIRCUIT BD ASSY:MAIN	80009	670-8163-08
A10	670-8163-09	B014161	B014161	CIRCUIT BD ASSY:MAIN	80009	670-8163-09
A10	670-8163-10	B014162	B014161	CIRCUIT BD ASSY:MAIN	80009	670-8163-10
A10	670-8163-11	B014162		CIRCUIT BD ASSY:MAIN (2430 ONLY)	80009	670-8163-11
A10	670-8163-06	B010100	B010126	CIRCUIT BD ASSY:MAIN	80009	670-8163-06
A10	670-8163-09	B010127	B019999	CIRCUIT BD ASSY:MAIN (2430M ONLY)	80009	670-8163-09
A10AT300	119-1445-04	B010100	B013300	ATTENUATOR,VAR:PRGM 1X-100X,10DB,CH2	80009	119-1445-04
A10AT300	119-2342-02	B0103301	B014139	ATTENUATOR,VAR:PRGM 1X-100X,DECADESTEPS	80009	119-2342-02
A10AT300	119-2342-04	B014140		ATTENUATOR,VAR:PROGRAMMABLE 1X-100X (2430 ONLY)	80009	119-2342-04
A10AT300	119-2342-02	B010100	B010145	ATTENUATOR,VAR:PRGM 1X-100X,DECADESTEPS	80009	119-2342-02
A10AT300	119-2342-04	B010146		ATTENUATOR,VAR:PROGRAMMABLE 1X-100X (2430M ONLY)	80009	119-2342-04
A10AT400	119-1445-03	B010100	B013300	ATTENUATOR,VAR:PRGM 1X-100X,10DB,CH1	80009	119-1445-03
A10AT400	119-2342-01	B0103301	B014139	ATTENUATOR,VAR:PRGM 1X-100X,DECADE STEPS	80009	119-2342-01
A10AT400	119-2342-03	B014140		ATTENUATOR,VAR:PROGRAMMABLE 1X-100X (2430 ONLY)	80009	119-2342-03
A10AT400	119-2342-01	B010100	B010145	ATTENUATOR,VAR:PRGM 1X-100X,DECADE STEPS	80009	119-2342-01
A10AT400	119-2342-03	B010146		ATTENUATOR,VAR:PROGRAMMABLE 1X-100X (2430M ONLY)	80009	119-2342-03
A10C101	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C102	281-0814-00			CAP,FXD,CER DI:100 PF,10%,100V	04222	MA101A101KAA
A10C110	290-0943-00	B010100	B013921	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C110	290-0943-02	B013922		CAP,FXD,ELCTLT:47UF,20%,25V (2430 ONLY)	55680	UVX1E470MAA1TD
A10C110	290-0943-00	B010100	B010139	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C110	290-0943-02	B010140		CAP,FXD,ELCTLT:47UF,20%,25V (2430M ONLY)	55680	UVX1E470MAA1TD
A10C111	290-0943-00	B010100	B013921	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C111	290-0943-02	B013922		CAP,FXD,ELCTLT:47UF,20%,25V (2430 ONLY)	55680	UVX1E470MAA1TD
A10C111	290-0943-00	B010100	B010139	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C111	290-0943-02	B010140		CAP,FXD,ELCTLT:47UF,20%,25V (2430M ONLY)	55680	UVX1E470MAA1TD
A10C112	290-0943-00	B010100.	B013921	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C112	290-0943-02	B013922		CAP,FXD,ELCTLT:47UF,20%,25V (2430 ONLY)	55680	UVX1E470MAA1TD
A10C112	290-0943-00	B010100	B010139	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C112	290-0943-02	B010140		CAP,FXD,ELCTLT:47UF,20%,25V (2430M ONLY)	55680	UVX1E470MAA1TD
A10C120	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C122	290-0943-00	B010100	B013921	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C122	290-0943-02	B013922		CAP,FXD,ELCTLT:47UF,20%,25V (2430 ONLY)	55680	UVX1E470MAA1TD
A10C122	290-0943-00	B010100	B010139	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C122	290-0943-02	B010140		CAP,FXD,ELCTLT:47UF,20%,25V (2430M ONLY)	55680	UVX1E470MAA1TD
A10C140	290-0943-00	B010100	B013921	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C140	290-0943-02	B013922		CAP,FXD,ELCTLT:47UF,20%,25V (2430 ONLY)	55680	UVX1E470MAA1TD
A10C140	290-0943-00	B010100	B010139	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C140	290-0943-02	B010140		CAP,FXD,ELCTLT:47UF,20%,25V (2430M ONLY)	55680	UVX1E470MAA1TD

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A10C141	290-0943-00	B010100	B013921	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C141	290-0943-02	B013922		CAP,FXD,ELCTLT:47UF,20%,25V (2430 ONLY)	55680	UVX1E470MAA1TD
A10C141	290-0943-00	B010100	B010139	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C141	290-0943-02	B010140		CAP,FXD,ELCTLT:47UF,20%,25V (2430M ONLY)	55680	UVX1E470MAA1TD
A10C143	290-0943-00	B010100	B013921	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C143	290-0943-02	B013922		CAP,FXD,ELCTLT:47UF,20%,25V (2430 ONLY)	55680	UVX1E470MAA1TD
A10C143	290-0943-00	B010100	B010139	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C143	290-0943-02	B010140		CAP,FXD,ELCTLT:47UF,20%,25V (2430M ONLY)	55680	UVX1E470MAA1TD
A10C144	281-0798-00			CAP,FXD,CER DI:51PF,1%,100V	04222	MA101A510GAA
A10C150	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C160	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C161	290-0246-00			CAP,FXD,ELCTLT:3.3UF,10%,15V	12954	D3R3EA15K1
A10C162	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C169	290-0943-00	B010100	B013921	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C169	290-0943-02	B013922		CAP,FXD,ELCTLT:47UF,20%,25V (2430 ONLY)	55680	UVX1E470MAA1TD
A10C169	290-0943-00	B010100	B010139	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C169	290-0943-02	B010140		CAP,FXD,ELCTLT:47UF,20%,25V (2430M ONLY)	55680	UVX1E470MAA1TD
A10C172	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C189	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C190	290-0943-00	B010100	B013921	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C190	290-0943-02	B013922		CAP,FXD,ELCTLT:47UF,20%,25V (2430 ONLY)	55680	UVX1E470MAA1TD
A10C190	290-0943-00	B010100	B010139	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C190	290-0943-02	B010140		CAP,FXD,ELCTLT:47UF,20%,25V (2430M ONLY)	55680	UVX1E470MAA1TD
A10C201	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C202	290-0943-00	B010100	B013921	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C202	290-0943-02	B013922		CAP,FXD,ELCTLT:47UF,20%,25V (2430 ONLY)	55680	UVX1E470MAA1TD
A10C202	290-0943-00	B010100	B010139	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C202	290-0943-02	B010140		CAP,FXD,ELCTLT:47UF,20%,25V (2430M ONLY)	55680	UVX1E470MAA1TD
A10C205	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C210	290-0943-00	B010100	B013921	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C210	290-0943-02	B013922		CAP,FXD,ELCTLT:47UF,20%,25V (2430 ONLY)	55680	UVX1E470MAA1TD
A10C210	290-0943-00	B010100	B010139	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C210	290-0943-02	B010140		CAP,FXD,ELCTLT:47UF,20%,25V (2430M ONLY)	55680	UVX1E470MAA1TD
A10C211	290-0943-00	B010100	B013921	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C211	290-0943-02	B013922		CAP,FXD,ELCTLT:47UF,20%,25V (2430 ONLY)	55680	UVX1E470MAA1TD
A10C211	290-0943-00	B010100	B010139	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C211	290-0943-02	B010140		CAP,FXD,ELCTLT:47UF,20%,25V (2430M ONLY)	55680	UVX1E470MAA1TD
A10C212	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C213	290-0943-00	B010100	B013921	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C213	290-0943-02	B013922		CAP,FXD,ELCTLT:47UF,20%,25V (2430 ONLY)	55680	UVX1E470MAA1TD
A10C213	290-0943-00	B010100	B010139	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C213	290-0943-02	B010140		CAP,FXD,ELCTLT:47UF,20%,25V (2430M ONLY)	55680	UVX1E470MAA1TD
A10C214	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C215	290-0943-00	B010100	B013921	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C215	290-0943-02	B013922		CAP,FXD,ELCTLT:47UF,20%,25V	55680	UVX1E470MAA1TD

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
				(2430 ONLY)		
A10C215	290-0943-00	B010100	B010139	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C215	290-0943-02	B010140		CAP,FXD,ELCTLT:47UF,20%,25V (2430M ONLY)	55680	UVX1E470MAA1TD
A10C216	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C220	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C222	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C223	290-0943-00	B010100	B013921	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C223	290-0943-02	B013922		CAP,FXD,ELCTLT:47UF,20%,25V (2430 ONLY)	55680	UVX1E470MAA1TD
A10C223	290-0943-00	B010100	B010139	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C223	290-0943-02	B010140		CAP,FXD,ELCTLT:47UF,20%,25V (2430M ONLY)	55680	UVX1E470MAA1TD
A10C225	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C230	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C231	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C232	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C233	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C235	281-0093-00			CAP,VAR,CER DI:5.5-18PF,350V	52763	302322237
A10C240	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C241	290-0246-00			CAP,FXD,ELCTLT:3.3UF,10%,15V	12954	D3R3EA15K1
A10C242	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C243	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C250	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C260	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C263	290-0943-00	B010100	B013921	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C263	290-0943-02	B013922		CAP,FXD,ELCTLT:47UF,20%,25V (2430 ONLY)	55680	UVX1E470MAA1TD
A10C263	290-0943-00	B010100	B010139	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C263	290-0943-02	B010140		CAP,FXD,ELCTLT:47UF,20%,25V (2430M ONLY)	55680	UVX1E470MAA1TD
A10C264	283-0203-00			CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A10C265	290-0943-00	B010100	B013921	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C265	290-0943-02	B013922		CAP,FXD,ELCTLT:47UF,20%,25V (2430 ONLY)	55680	UVX1E470MAA1TD
A10C265	290-0943-00	B010100	B010139	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C265	290-0943-02	B010140		CAP,FXD,ELCTLT:47UF,20%,25V (2430M ONLY)	55680	UVX1E470MAA1TD
A10C272	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C280	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C281	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C282	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C287	281-0798-00	B010100	B010808	CAP,FXD,CER DI:51PF,1%,100V	04222	MA101A510GAA
A10C287	281-0763-00	B010809		CAP,FXD,CER DI:47PF,10%,100V	04222	MA101A470KAA
A10C288	281-0798-00	B010100	B010808	CAP,FXD,CER DI:51PF,1%,100V	04222	MA101A510GAA
A10C288	281-0763-00	B010809		CAP,FXD,CER DI:47PF,10%,100V	04222	MA101A470KAA
A10C290	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C310	281-0909-00	B014162		CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C311	281-0064-00			CAP,VAR,PLASTIC:0.25-1.5PF,600V	52769	ER-530-013
A10C330	281-0909-00	B010127		CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C340	290-0943-00	B010100	B013921	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C340	290-0943-02	B013922		CAP,FXD,ELCTLT:47UF,20%,25V (2430 ONLY)	55680	UVX1E470MAA1TD
A10C340	290-0943-00	B010100	B010139	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C340	290-0943-02	B010140		CAP,FXD,ELCTLT:47UF,20%,25V (2430M ONLY)	55680	UVX1E470MAA1TD
A10C341	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C350	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C351	283-0158-00	B010823	B011519	CAP,FXD,CER DI:1PF,+/-0.1PF,50V	51642	100-050-NPO-109B
A10C351	283-0348-00	B011520	B012726	CAP,FXD,CER DI:0.5PF,+/-0.1PF,100V	51642	W150100NP0508B

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A10C351	281-0138-00	B012727		CAP,VAR,PLASTIC:0.3-1.2PF,600V	74970	273-0001-007
A10C352	283-0158-00	B010823	B011519	CAP,FXD,CER DI:1PF,+/-0.1PF,50V	51642	100-050-NPO-109B
A10C352	283-0348-00	B011520	B012726	CAP,FXD,CER DI:0.5PF,+/-0.1PF,100V	51642	W150100NP0508B
A10C352	281-0138-00	B012727		CAP,VAR,PLASTIC:0.3-1.2PF,600V	74970	273-0001-007
A10C353	283-0158-00	B010823	B011519	CAP,FXD,CER DI:1PF,+/-0.1PF,50V	51642	100-050-NPO-109B
A10C353	283-0348-00	B011520	B012726	CAP,FXD,CER DI:0.5PF,+/-0.1PF,100V	51642	W150100NP0508B
A10C353	281-0138-00	B012727		CAP,VAR,PLASTIC:0.3-1.2PF,600V	74970	273-0001-007
A10C354	283-0158-00	B010823	B011519	CAP,FXD,CER DI:1PF,+/-0.1PF,50V	51642	100-050-NPO-109B
A10C354	283-0348-00	B011520	B012726	CAP,FXD,CER DI:0.5PF,+/-0.1PF,100V	51642	W150100NP0508B
A10C354	281-0138-00	B012727		CAP,VAR,PLASTIC:0.3-1.2PF,600V	74970	273-0001-007
A10C361	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C370	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C371	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C372	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C375	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C380	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C390	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C391	281-0798-00			CAP,FXD,CER DI:51PF,1%,100V	04222	MA101A510GAA
A10C410	283-0203-00			CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A10C412	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C414	281-0064-00			CAP,VAR,PLASTIC:0.25-1.5PF,600V	52769	ER-530-013
A10C422	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C423	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C430	281-0909-00	B010127		CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C431	281-0093-00			CAP,VAR,CER DI:5.5-18PF,350V	52763	302322237
A10C440	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C441	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C450	283-0203-02	B012727		CAP,FXD,CER DI:0.47UF,20%,50V	05397	C330C474M5U5CA
A10C460	283-0203-02	B012727		CAP,FXD,CER DI:0.47UF,20%,50V	05397	C330C474M5U5CA
A10C464	283-0203-00			CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A10C465	290-0943-00	B010100	B013921	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C465	290-0943-02	B013922		CAP,FXD,ELCTLT:47UF,20%,25V (2430 ONLY)	55680	UVX1E470MAA1TD
A10C465	290-0943-00	B010100	B010139	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C465	290-0943-02	B010140		CAP,FXD,ELCTLT:47UF,20%,25V (2430M ONLY)	55680	UVX1E470MAA1TD
A10C471	290-0943-00	B010100	B013921	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C471	290-0943-02	B013922		CAP,FXD,ELCTLT:47UF,20%,25V (2430 ONLY)	55680	UVX1E470MAA1TD
A10C471	290-0943-00	B010100	B010139	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C471	290-0943-02	B010140		CAP,FXD,ELCTLT:47UF,20%,25V (2430M ONLY)	55680	UVX1E470MAA1TD
A10C472	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C473	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C474	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C480	290-0943-00	B010100	B013921	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C480	290-0943-02	B013922		CAP,FXD,ELCTLT:47UF,20%,25V (2430 ONLY)	55680	UVX1E470MAA1TD
A10C480	290-0943-00	B010100	B010139	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C480	290-0943-02	B010140		CAP,FXD,ELCTLT:47UF,20%,25V (2430M ONLY)	55680	UVX1E470MAA1TD
A10C481	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C483	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C484	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C488	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C490	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C491	281-0798-00			CAP,FXD,CER DI:51PF,1%,100V	04222	MA101A510GAA
A10C492	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C493	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T

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A10C500	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C509	283-0203-00			CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A10C510	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C511	290-0943-00	B010100	B013921	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C511	290-0943-02	B013922		CAP,FXD,ELCTLT:47UF,20%,25V (2430 ONLY)	55680	UVX1E470MAA1TD
A10C511	290-0943-00	B010100	B010139	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C511	290-0943-02	B010140		CAP,FXD,ELCTLT:47UF,20%,25V (2430M ONLY)	55680	UVX1E470MAA1TD
A10C512	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C522	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C523	290-0943-00	B010100	B013921	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C523	290-0943-02	B013922		CAP,FXD,ELCTLT:47UF,20%,25V (2430 ONLY)	55680	UVX1E470MAA1TD
A10C523	290-0943-00	B010100	B010139	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C523	290-0943-02	B010140		CAP,FXD,ELCTLT:47UF,20%,25V (2430M ONLY)	55680	UVX1E470MAA1TD
A10C524	290-0943-00	B010100	B013921	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C524	290-0943-02	B013922		CAP,FXD,ELCTLT:47UF,20%,25V (2430 ONLY)	55680	UVX1E470MAA1TD
A10C524	290-0943-00	B010100	B010139	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C524	290-0943-02	B010140		CAP,FXD,ELCTLT:47UF,20%,25V (2430M ONLY)	55680	UVX1E470MAA1TD
A10C530	290-0776-00			CAP,FXD,ELCTLT:22UF,+50-20 %,10V	55680	ULA1A220TAA
A10C532	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C535	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C540	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C541	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C542	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C550	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C560	281-0763-00	B010350		CAP,FXD,CER DI:47PF,10%,100V	04222	MA101A470KAA
A10C561	285-1343-00	B010100	B010126	CAP,FXD,PLASTIC:330PF,100V,5%	TK1573	FKP2 330 5% 100V
A10C561	285-1362-00	B010127		CAP,FXD,PLASTIC:560PF,2.5%,100V	TK1573	FKP2 560PF 2.5%
A10C562	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C563	285-1343-00	B010100	B010126	CAP,FXD,PLASTIC:330PF,100V,5%	TK1573	FKP2 330 5% 100V
A10C563	285-1362-00	B010127		CAP,FXD,PLASTIC:560PF,2.5%,100V	TK1573	FKP2 560PF 2.5%
A10C580	281-0852-00			CAP,FXD,CER DI:1800PF,10%,100VDC	04222	MA101C182KAA
A10C581	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C582	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C590	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C591	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C600	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C601	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C602	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C630	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C631	283-0203-00	B010100	B014160	CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A10C631	285-1301-01	B014161		CAP,FXD,MTLZD:0.47UF,10%,50V (2430 ONLY)	55112	1850.47K50ABB
A10C631	283-0203-00	B010100	B019999	CAP,FXD,CER DI:0.47UF,20%,50V (2430M ONLY)	04222	SR305SC474MAA
A10C632	283-0203-00	B010100	B014160	CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A10C632	285-1301-01	B014161		CAP,FXD,MTLZD:0.47UF,10%,50V (2430 ONLY)	55112	1850.47K50ABB
A10C632	283-0203-00	B010100	B019999	CAP,FXD,CER DI:0.47UF,20%,50V (2430M ONLY)	04222	SR305SC474MAA
A10C633	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C635	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C640	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C641	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C642	283-0203-00			CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA

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A10C643	283-0203-00			CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A10C644	283-0203-00	B010100	B014160	CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A10C644	285-1301-01	B014161		CAP,FXD,MTLZD:0.47UF,10%,50V (2430 ONLY)	55112	1850.47K50ABB
A10C644	283-0203-00	B010100	B019999	CAP,FXD,CER DI:0.47UF,20%,50V (2430M ONLY)	04222	SR305SC474MAA
A10C645	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C646	283-0203-00			CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A10C647	283-0203-00	B010100	B014160	CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A10C647	285-1301-01	B014161		CAP,FXD,MTLZD:0.47UF,10%,50V (2430 ONLY)	55112	1850.47K50ABB
A10C647	283-0203-00	B010100	B019999	CAP,FXD,CER DI:0.47UF,20%,50V (2430M ONLY)	04222	SR305SC474MAA
A10C648	283-0203-00	B010100	B014160	CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A10C648	285-1301-01	B014161		CAP,FXD,MTLZD:0.47UF,10%,50V (2430 ONLY)	55112	1850.47K50ABB
A10C648	283-0203-00	B010100	B019999	CAP,FXD,CER DI:0.47UF,20%,50V (2430M ONLY)	04222	SR305SC474MAA
A10C649	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C650	283-0203-00			CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A10C651	283-0203-00			CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A10C653	283-0203-00	B010100	B014160	CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A10C653	285-1301-01	B014161		CAP,FXD,MTLZD:0.47UF,10%,50V (2430 ONLY)	55112	1850.47K50ABB
A10C653	283-0203-00	B010100	B019999	CAP,FXD,CER DI:0.47UF,20%,50V (2430M ONLY)	04222	SR305SC474MAA
A10C654	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C655	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C656	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C660	283-0203-00	B010100	B014160	CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A10C660	285-1301-01	B014161		CAP,FXD,MTLZD:0.47UF,10%,50V (2430 ONLY)	55112	1850.47K50ABB
A10C660	283-0203-00	B010100	B019999	CAP,FXD,CER DI:0.47UF,20%,50V (2430M ONLY)	04222	SR305SC474MAA
A10C661	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C662	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C663	285-1343-00	B010100	B010126	CAP,FXD,PLASTIC:330PF,100V,5%	TK1573	FKP2 330 5% 100V
A10C663	285-1362-00	B010127		CAP,FXD,PLASTIC:560PF,2.5%,100V	TK1573	FKP2 560PF 2.5%
A10C664	285-1343-00	B010100	B010126	CAP,FXD,PLASTIC:330PF,100V,5%	TK1573	FKP2 330 5% 100V
A10C664	285-1362-00	B010127		CAP,FXD,PLASTIC:560PF,2.5%,100V	TK1573	FKP2 560PF 2.5%
A10C665	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C670	285-1343-00	B010322	B011848	CAP,FXD,PLASTIC:330PF,100V,5%	TK1573	FKP2 330 5% 100V
A10C680	285-1343-00	B010322	B011848	CAP,FXD,PLASTIC:330PF,100V,5%	TK1573	FKP2 330 5% 100V
A10C685	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C686	290-0943-00	B010100	B013921	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C686	290-0943-02	B013922		CAP,FXD,ELCTLT:47UF,20%,25V (2430 ONLY)	55680	UVX1E470MAA1TD
A10C686	290-0943-00	B010100	B010139	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C686	290-0943-02	B010140		CAP,FXD,ELCTLT:47UF,20%,25V (2430M ONLY)	55680	UVX1E470MAA1TD
A10C690	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C701	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C711	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C730	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C731	283-0203-00	B010100	B014160	CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A10C731	285-1301-01	B014161		CAP,FXD,MTLZD:0.47UF,10%,50V (2430 ONLY)	55112	1850.47K50ABB
A10C731	283-0203-00	B010100	B019999	CAP,FXD,CER DI:0.47UF,20%,50V (2430M ONLY)	04222	SR305SC474MAA
A10C732	283-0203-00	B010100	B014160	CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA

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A10C732	285-1301-01	B014161		CAP,FXD,MTLZD:0.47UF,10%,50V (2430 ONLY)	55112	1850.47K50ABB
A10C732	283-0203-00	B010100	B019999	CAP,FXD,CER DI:0.47UF,20%,50V (2430M ONLY)	04222	SR305SC474MAA
A10C733	283-0203-00	B010100	B014160	CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A10C733	285-1301-01	B014161		CAP,FXD,MTLZD:0.47UF,10%,50V (2430 ONLY)	55112	1850.47K50ABB
A10C733	283-0203-00	B010100	B019999	CAP,FXD,CER DI:0.47UF,20%,50V (2430M ONLY)	04222	SR305SC474MAA
A10C734	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C735	283-0203-00			CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A10C740	283-0203-00	B010100	B014160	CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A10C740	285-1301-01	B014161		CAP,FXD,MTLZD:0.47UF,10%,50V (2430 ONLY)	55112	1850.47K50ABB
A10C740	283-0203-00	B010100	B019999	CAP,FXD,CER DI:0.47UF,20%,50V (2430M ONLY)	04222	SR305SC474MAA
A10C741	283-0203-00	B010100	B014160	CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A10C741	285-1301-01	B014161		CAP,FXD,MTLZD:0.47UF,10%,50V (2430 ONLY)	55112	1850.47K50ABB
A10C741	283-0203-00	B010100	B019999	CAP,FXD,CER DI:0.47UF,20%,50V (2430M ONLY)	04222	SR305SC474MAA
A10C742	283-0203-00			CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A10C743	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C744	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C745	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C746	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C747	283-0203-00	B010100	B014160	CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A10C747	285-1301-01	B014161		CAP,FXD,MTLZD:0.47UF,10%,50V (2430 ONLY)	55112	1850.47K50ABB
A10C747	283-0203-00	B010100	B019999	CAP,FXD,CER DI:0.47UF,20%,50V (2430M ONLY)	04222	SR305SC474MAA
A10C748	283-0203-00			CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A10C751	281-0814-00			CAP,FXD,CER DI:100 PF,10%,100V	04222	MA101A101KAA
A10C752	283-0203-00	B010100	B014160	CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A10C752	285-1301-01	B014161		CAP,FXD,MTLZD:0.47UF,10%,50V (2430 ONLY)	55112	1850.47K50ABB
A10C752	283-0203-00	B010100	B019999	CAP,FXD,CER DI:0.47UF,20%,50V (2430M ONLY)	04222	SR305SC474MAA
A10C753	283-0203-00	B010100	B014160	CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A10C753	285-1301-01	B014161		CAP,FXD,MTLZD:0.47UF,10%,50V (2430 ONLY)	55112	1850.47K50ABB
A10C753	283-0203-00	B010100	B019999	CAP,FXD,CER DI:0.47UF,20%,50V (2430M ONLY)	04222	SR305SC474MAA
A10C760	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C761	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C762	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C763	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C765	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C766	290-0943-00	B010100	B013921	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C766	290-0943-02	B013922		CAP,FXD,ELCTLT:47UF,20%,25V (2430 ONLY)	55680	UVX1E470MAA1TD
A10C766	290-0943-00	B010100	B010139	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C766	290-0943-02	B010140		CAP,FXD,ELCTLT:47UF,20%,25V (2430M ONLY)	55680	UVX1E470MAA1TD
A10C768	290-0943-00	B010100	B013921	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C768	290-0943-02	B013922		CAP,FXD,ELCTLT:47UF,20%,25V (2430 ONLY)	55680	UVX1E470MAA1TD
A10C768	290-0943-00	B010100	B010139	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C768	290-0943-02	B010140		CAP,FXD,ELCTLT:47UF,20%,25V (2430M ONLY)	55680	UVX1E470MAA1TD
A10C770	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C771	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T

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A10C772	285-1343-00	B010322	B011848	CAP,FXD,PLASTIC:330PF,100V,5%	TK1573	FKP2 330 5% 100V
A10C774	281-0851-00			CAP,FXD,CER DI:180PF,5%,100VDC	04222	MA101A181JAA
A10C780	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C782	281-0851-00			CAP,FXD,CER DI:180PF,5%,100VDC	04222	MA101A181JAA
A10C783	285-1343-00	B010322	B011848	CAP,FXD,PLASTIC:330PF,100V,5%	TK1573	FKP2 330 5% 100V
A10C784	281-0851-00			CAP,FXD,CER DI:180PF,5%,100VDC	04222	MA101A181JAA
A10C790	290-0743-00			CAP,FXD,ELCTLT:100UF,+50%-20%,16WVDC	54473	ECE-B16V100L
A10C809	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C810	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C812	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C813	281-0757-00	B010100	B010670	CAP,FXD,CER DI:10PF,20%,100V TUBULAR,MI	04222	MA101A100MAA
A10C813	281-0763-00	B010671		CAP,FXD,CER DI:47PF,10%,100V	04222	MA101A470KAA
A10C817	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C820	283-0203-00			CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A10C821	283-0203-00	B010100	B014160	CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A10C821	285-1301-01	B014161		CAP,FXD,MTLZD:0.47UF,10%,50V (2430 ONLY)	55112	1850.47K50ABB
A10C821	283-0203-00	B010100	B019999	CAP,FXD,CER DI:0.47UF,20%,50V (2430M ONLY)	04222	SR305SC474MAA
A10C822	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C823	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C824	283-0203-00	B010100	B014160	CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A10C824	285-1301-01	B014161		CAP,FXD,MTLZD:0.47UF,10%,50V (2430 ONLY)	55112	1850.47K50ABB
A10C824	283-0203-00	B010100	B019999	CAP,FXD,CER DI:0.47UF,20%,50V (2430M ONLY)	04222	SR305SC474MAA
A10C825	283-0203-00	B010100	B014160	CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A10C825	285-1301-01	B014161		CAP,FXD,MTLZD:0.47UF,10%,50V (2430 ONLY)	55112	1850.47K50ABB
A10C825	283-0203-00	B010100	B019999	CAP,FXD,CER DI:0.47UF,20%,50V (2430M ONLY)	04222	SR305SC474MAA
A10C826	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C830	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C832	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C834	283-0203-00	B010100	B014160	CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A10C834	285-1301-01	B014161		CAP,FXD,MTLZD:0.47UF,10%,50V (2430 ONLY)	55112	1850.47K50ABB
A10C834	283-0203-00	B010100	B019999	CAP,FXD,CER DI:0.47UF,20%,50V (2430M ONLY)	04222	SR305SC474MAA
A10C835	283-0203-00	B010100	B014160	CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A10C835	285-1301-01	B014161		CAP,FXD,MTLZD:0.47UF,10%,50V (2430 ONLY)	55112	1850.47K50ABB
A10C835	283-0203-00	B010100	B019999	CAP,FXD,CER DI:0.47UF,20%,50V (2430M ONLY)	04222	SR305SC474MAA
A10C840	283-0203-00	B010100	B014160	CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A10C840	285-1301-01	B014161		CAP,FXD,MTLZD:0.47UF,10%,50V (2430 ONLY)	55112	1850.47K50ABB
A10C840	283-0203-00	B010100	B019999	CAP,FXD,CER DI:0.47UF,20%,50V (2430M ONLY)	04222	SR305SC474MAA
A10C843	283-0203-00	B010100	B014160	CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A10C843	285-1301-01	B014161		CAP,FXD,MTLZD:0.47UF,10%,50V (2430 ONLY)	55112	1850.47K50ABB
A10C843	283-0203-00	B010100	B019999	CAP,FXD,CER DI:0.47UF,20%,50V (2430M ONLY)	04222	SR305SC474MAA
A10C844	283-0203-00			CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A10C845	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C846	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C850	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C851	290-0943-00	B010100	B013921	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C851	290-0943-02	B013922		CAP,FXD,ELCTLT:47UF,20%,25V	55680	UVX1E470MAA1TD

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				(2430 ONLY)		
A10C851	290-0943-00	B010100	B010139	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A10C851	290-0943-02	B010140		CAP,FXD,ELCTLT:47UF,20%,25V	55680	UVX1E470MAA1TD
				(2430M ONLY)		
A10C870	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C871	281-0851-00			CAP,FXD,CER DI:180PF,5%,100VDC	04222	MA101A181JAA
A10C880	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A10C882	281-0851-00			CAP,FXD,CER DI:180PF,5%,100VDC	04222	MA101A181JAA
A10C1005	283-0000-00			CAP,FXD,CER DI:0.001UF,+100-0%,500V	59660	831-610-Y5U0102P
A10C1006	283-0000-00			CAP,FXD,CER DI:0.001UF,+100-0%,500V	59660	831-610-Y5U0102P
A10CR140	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR141	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR185	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR186	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR220	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR221	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR222	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR223	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR224	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR225	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR226	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR227	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR228	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR285	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR286	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR287	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR288	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR290	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR291	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR292	152-0141-02	B010100	B010349	SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR292	152-0322-00	B010350	B013917	SEMICOND DVC,DI:SCHOTTKY,SI,15V,1.2PF,DO-35	50434	5082-2672
A10CR292	152-0951-00	B013918		SEMICOND DVC DI:SCHOTTKY,SI,60V,2.25PF	80009	152-0951-00
A10CR310	152-0323-01			SEMICOND DVC,DI:SW,SI,35V,0.1A,DO-35	14552	MT5127
A10CR311	152-0323-01			SEMICOND DVC,DI:SW,SI,35V,0.1A,DO-35	14552	MT5127
A10CR392	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR410	152-0323-01			SEMICOND DVC,DI:SW,SI,35V,0.1A,DO-35	14552	MT5127
A10CR411	152-0323-01			SEMICOND DVC,DI:SW,SI,35V,0.1A,DO-35	14552	MT5127
A10CR420	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR490	152-0141-02	B010100	B010349	SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR490	152-0322-00	B010350	B013917	SEMICOND DVC,DI:SCHOTTKY,SI,15V,1.2PF,DO-35	50434	5082-2672
A10CR490	152-0951-00	B013918		SEMICOND DVC DI:SCHOTTKY,SI,60V,2.25PF	80009	152-0951-00
A10CR491	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR500	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR501	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR502	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR503	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR530	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR550	152-0141-02	B011410		SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR551	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR552	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR553	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR580	152-0650-00			SEMICOND DVC,DI:VVC,30V,11.5PF,A276	50101	U11-4101
A10CR581	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR590	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR591	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR600	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR601	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR602	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A10CR610	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR612	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR613	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR614	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR620	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR621	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR622	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR650	152-0141-02	B011410	B012726	SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR670	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR680	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR701	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR702	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR770	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR771	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR780	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR781	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR810	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR870	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR880	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10DL470	119-1823-00			DELAY LINE,ELEC:DUAL,4NS,2NS,32 AWG PTFE PR IRS	80009	119-1823-00
A10J104	131-3176-00			CONN,RCPT,ELEC:CKT BD,1 X 6,0.1 SPACING	00779	643091-1
A10J105	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 6)	22526	48283-036
A10J106	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 2)	22526	48283-036
A10J107	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 4)	22526	48283-036
A10J108	131-3152-00			CONN,RCPT,ELEC:HEADER,2 X 8 0.1 SPACING	22526	66506-043
A10J111	131-3181-00			CONN,RCPT,ELEC:HEADER,RTANG,2 X 20,0.1 CTR	22526	75867-007
A10J113	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 8)	22526	48283-036
A10J114	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 4)	22526	48283-036
A10J141	131-3182-00			CONN,RCPT,ELEC:HDR,RTANG,2 X 25,0.1 CENTER	22526	75867-008
A10J146	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 3)	22526	48283-036
A10J147	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 3)	22526	48283-036
A10J152	131-3152-00			CONN,RCPT,ELEC:HEADER,2 X 8 0.1 SPACING	22526	66506-043
A10J2006	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A10L120	108-0538-00			COIL,RF:FIXED,2.7UH	76493	JWM#B7059
A10L150	108-0538-00			COIL,RF:FIXED,2.7UH	76493	JWM#B7059
A10L200	108-0538-00			COIL,RF:FIXED,2.7UH	76493	JWM#B7059
A10L210	108-0538-00			COIL,RF:FIXED,2.7UH	76493	JWM#B7059
A10L220	108-0538-00			COIL,RF:FIXED,2.7UH	76493	JWM#B7059
A10L260	108-0538-00			COIL,RF:FIXED,2.7UH	76493	JWM#B7059
A10L261	108-0538-00			COIL,RF:FIXED,2.7UH	76493	JWM#B7059
A10L270	108-0538-00			COIL,RF:FIXED,2.7UH	76493	JWM#B7059
A10L332	108-0262-00			COIL,RF:FIXED,505NH	80009	108-0262-00
A10L340	108-0538-00			COIL,RF:FIXED,2.7UH	76493	JWM#B7059
A10L350	108-1309-00			COIL,RF:FXD,70NH,15%	TK2042	ORDER BY DESCR
A10L351	108-1309-00			COIL,RF:FXD,70NH,15%	TK2042	ORDER BY DESCR
A10L352	108-1309-00			COIL,RF:FXD,70NH,15%	TK2042	ORDER BY DESCR
A10L353	108-1309-00			COIL,RF:FXD,70NH,15%	TK2042	ORDER BY DESCR
A10L431	114-0266-00	B012727		COIL,RF:VARIABLE,400-800NH	80009	114-0266-00
A10L450	108-1309-00			COIL,RF:FXD,70NH,15%	TK2042	ORDER BY DESCR
A10L451	108-1309-00			COIL,RF:FXD,70NH,15%	TK2042	ORDER BY DESCR
A10L480	108-0538-00			COIL,RF:FIXED,2.7UH	76493	JWM#B7059

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A10L510	108-0538-00			COIL,RF:FIXED,2.7UH	76493	JWM#B7059
A10L520	108-0538-00			COIL,RF:FIXED,2.7UH	76493	JWM#B7059
A10L521	108-0538-00			COIL,RF:FIXED,2.7UH	76493	JWM#B7059
A10L530	108-0262-00			COIL,RF:FIXED,505NH	80009	108-0262-00
A10L531	108-0262-00	B010100	B012726	COIL,RF:FIXED,505NH	80009	108-0262-00
A10L531	114-0266-00	B012727		COIL,RF:VARIABLE,400-800NH	80009	114-0266-00
A10L550	108-1309-00			COIL,RF:FXD,70NH,15%	TK2042	ORDER BY DESCR
A10L551	108-1309-00			COIL,RF:FXD,70NH,15%	TK2042	ORDER BY DESCR
A10L631	108-0262-00	B010100	B012726	COIL,RF:FIXED,505NH	80009	108-0262-00
A10LR215	108-0330-00			COIL,RF:FIXED,403NH	TK2042	ORDER BY DESCR
A10LR220	108-0284-00			COIL,RF:FIXED,97NH	TK2042	ORDER BY DESCR
A10LR410	108-0325-00			COIL,RF:FIXED,489NH	TK2042	ORDER BY DESCR
A10LR421	108-0284-00	B010100	B014161	COIL,RF:FIXED,97NH	TK2042	ORDER BY DESCR
A10LR422	108-0330-00			COIL,RF:FIXED,403NH	TK2042	ORDER BY DESCR
A10LR510	108-0325-00			COIL,RF:FIXED,489NH	TK2042	ORDER BY DESCR
A10Q110	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A10Q140	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A10Q150	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A10Q151	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A10Q170	151-0221-00	B011849		TRANSISTOR:PNP,SI,TO-92	80009	151-0221-00
A10Q240	153-0547-00			SEMICOND DVC SE:MATCHED PAIR	80009	153-0547-00
A10Q250	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A10Q251	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A10Q270	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A10Q271	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A10Q287	151-0223-00			TRANSISTOR:NPN,SI,625MW,TO-92	04713	SPS8026
A10Q288	151-0223-00			TRANSISTOR:NPN,SI,625MW,TO-92	04713	SPS8026
A10Q290	151-0367-00			TRANSISTOR:NPN,SI,X-55	04713	SPS 8811
A10Q291	151-0367-00			TRANSISTOR:NPN,SI,X-55	04713	SPS 8811
A10Q372	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A10Q375	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A10Q380	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A10Q390	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A10Q391	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A10Q392	151-0367-00			TRANSISTOR:NPN,SI,X-55	04713	SPS 8811
A10Q393	151-0192-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS8801
A10Q450	151-0221-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0221-00
A10Q460	151-0221-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0221-00
A10Q490	151-0367-00			TRANSISTOR:NPN,SI,X-55	04713	SPS 8811
A10Q491	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A10Q492	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A10Q493	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A10Q494	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A10Q495	151-0192-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS8801
A10Q530	151-0622-00			TRANSISTOR:PNP,SI,40V,1A,TO-226AE/237	04713	SPS8956(MPSW51A)
A10Q535	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A10Q536	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A10Q540	151-0622-00			TRANSISTOR:PNP,SI,40V,1A,TO-226AE/237	04713	SPS8956(MPSW51A)
A10Q550	151-0221-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0221-00
A10Q551	151-0221-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0221-00
A10Q560	151-0221-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0221-00
A10Q580	151-0622-00			TRANSISTOR:PNP,SI,40V,1A,TO-226AE/237	04713	SPS8956(MPSW51A)
A10Q620	151-0622-00			TRANSISTOR:PNP,SI,40V,1A,TO-226AE/237	04713	SPS8956(MPSW51A)
A10Q621	151-0622-00			TRANSISTOR:PNP,SI,40V,1A,TO-226AE/237	04713	SPS8956(MPSW51A)
A10Q630	151-0622-00			TRANSISTOR:PNP,SI,40V,1A,TO-226AE/237	04713	SPS8956(MPSW51A)
A10Q640	151-0622-00			TRANSISTOR:PNP,SI,40V,1A,TO-226AE/237	04713	SPS8956(MPSW51A)
A10Q660	151-0223-00			TRANSISTOR:NPN,SI,625MW,TO-92	04713	SPS8026
A10Q670	151-0223-00			TRANSISTOR:NPN,SI,625MW,TO-92	04713	SPS8026

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A10Q671	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A10Q680	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A10Q770	151-0223-00			TRANSISTOR:NPN,SI,625MW,TO-92	04713	SPS8026
A10Q771	151-0216-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS8803
A10Q772	151-0216-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS8803
A10Q773	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A10Q780	151-0223-00			TRANSISTOR:NPN,SI,625MW,TO-92	04713	SPS8026
A10Q781	151-0216-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS8803
A10Q782	151-0216-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS8803
A10Q783	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A10Q810	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A10Q870	151-0223-00			TRANSISTOR:NPN,SI,625MW,TO-92	04713	SPS8026
A10Q871	151-0216-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS8803
A10Q872	151-0216-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS8803
A10Q880	151-0223-00			TRANSISTOR:NPN,SI,625MW,TO-92	04713	SPS8026
A10Q881	151-0216-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS8803
A10Q882	151-0216-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS8803
A10R89	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A10R90	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A10R110	321-1700-04			RES,FXD,FILM:10.44K OHM,0.1%,0.125W,TC=T2	19701	5033RC10K440B
A10R111	315-0301-00			RES,FXD,FILM:300 OHM,5%,0.25W	57668	NTR25J-E300E
A10R112	315-0752-00			RES,FXD,FILM:7.5K OHM,5%,0.25W	57668	NTR25J-E07K5
A10R120	315-0562-00			RES,FXD,FILM:5.6K OHM,5%,0.25W	57668	NTR25J-E05K6
A10R121	308-0755-00			RES,FXD,WW:0.75 OHM,5%,2W	75042	BWH-R7500J
A10R130	321-0275-00			RES,FXD,FILM:7.15K OHM,1%,0.125W,TC=T0	07716	CEAD71500F
A10R131	321-0333-00			RES,FXD,FILM:28.7K OHM,1%,0.125W,TC=T0	19701	5043ED28K70F
A10R132	321-0085-00			RES,FXD,FILM:75 OHM,1%,0.125W,TC=T0	57668	CRB14FXE 75 OHM
A10R133	321-0275-00			RES,FXD,FILM:7.15K OHM,1%,0.125W,TC=T0	07716	CEAD71500F
A10R134	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A10R135	321-0287-00			RES,FXD,FILM:9.53K OHM,1%,0.125W,TC=T0	19701	5033ED9K530F
A10R136	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A10R140	321-0193-00			RES,FXD,FILM:1K OHM,1%,0.125W,TC=T0	19701	5033ED1K00F
A10R141	321-0063-00			RES,FXD,FILM:44.2 OHM,0.5%,0.125W,TC=T0	91637	CMF55116G44R20F
A10R142	315-0103-00	B010100	B014160	RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R142	315-0100-00	B014161		RES,FXD,FILM:10 OHM,5%,0.25W (2430 ONLY)	19701	5043CX10RR00J
A10R142	315-0103-00	B010100	B019999	RES,FXD,FILM:10K OHM,5%,0.25W (2430M ONLY)	19701	5043CX10K00J
A10R143	321-0193-00			RES,FXD,FILM:1K OHM,1%,0.125W,TC=T0	19701	5033ED1K00F
A10R144	315-0180-00			RES,FXD,FILM:18 OHM,5%,0.25W	19701	5043CX18R00J
A10R145	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A10R146	315-0272-00			RES,FXD,FILM:2.7K OHM,5%,0.25W	57668	NTR25J-E02K7
A10R150	315-0122-00			RES,FXD,FILM:1.2K OHM,5%,0.25W	57668	NTR25J-E01K2
A10R151	315-0750-00			RES,FXD,FILM:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A10R160	315-0750-00			RES,FXD,FILM:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A10R161	315-0750-00			RES,FXD,FILM:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A10R162	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A10R163	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R165	315-0750-00			RES,FXD,FILM:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A10R170	317-0102-00	B011849	B012726	RES,FXD,CMPSN:1K OHM,5%,0125W	01121	BB1025
A10R170	315-0302-00	B012727		RES,FXD,FILM:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A10R175	315-0302-00	B011849	B012726	RES,FXD,FILM:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A10R175	315-0102-00	B012727		RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R181	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R182	315-0560-00			RES,FXD,FILM:56 OHM,5%,0.25W	57668	NTR25J-E56E0
A10R183	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R184	315-0181-00			RES,FXD,FILM:180 OHM,5%,0.25W	57668	NTR25J-E180E
A10R185	315-0560-00	B010100	B010174	RES,FXD,FILM:56 OHM,5%,0.25W	57668	NTR25J-E56E0

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A10R185	315-0390-00	B010175		RES,FXD,FILM:39 OHM,5%,0.25W	57668	NTR25J-E39E0
A10R186	315-0181-00			RES,FXD,FILM:180 OHM,5%,0.25W	57668	NTR25J-E180E
A10R201	315-0272-00			RES,FXD,FILM:2.7K OHM,5%,0.25W	57668	NTR25J-E02K7
A10R202	315-0272-00			RES,FXD,FILM:2.7K OHM,5%,0.25W	57668	NTR25J-E02K7
A10R210	321-1700-04			RES,FXD,FILM:10.44K OHM,0.1%,0.125W,TC=T2	19701	5033RC10K440B
A10R211	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A10R215	321-0054-00			RES,FXD,FILM:35.7 OHM,0.5%,0.125W,TC=T0 MI	91637	CMF55116G35R70F
A10R216	321-0122-00			RES,FXD,FILM:182 OHM,1%,0.125W,TC=T0	19701	5033ED182R0F
A10R220	301-0361-00	B010100	B012064	RES,FXD,FILM:360 OHM,5%,0.5W	19701	5053CX360R0J
A10R220	301-0361-00	B012065		RES,FXD,FILM:360 OHM,5%,0.5W	19701	5053CX360R0J
A10R222	315-0121-00			RES,FXD,FILM:120 OHM,5%,0.25W	19701	5043CX120R0J
A10R225	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A10R230	321-0310-00			RES,FXD,FILM:16.5K OHM,1%,0.125W,TC=T0	19701	5033ED16K50F
A10R231	321-0310-00			RES,FXD,FILM:16.5K OHM,1%,0.125W,TC=T0	19701	5033ED16K50F
A10R232	321-0255-00			RES,FXD,FILM:4.42K OHM,1%,0.125W,TC=T0	19701	5033ED4K420F
A10R234	321-0062-00			RES,FXD,FILM:43.2 OHM,0.5%,0.125W,TC=T0	57668	CRB14 FXE 43.2
A10R235	321-0275-00			RES,FXD,FILM:7.15K OHM,1%,0.125W,TC=T0	07716	CEAD71500F
A10R236	321-0310-00			RES,FXD,FILM:16.5K OHM,1%,0.125W,TC=T0	19701	5033ED16K50F
A10R237	321-0310-00			RES,FXD,FILM:16.5K OHM,1%,0.125W,TC=T0	19701	5033ED16K50F
A10R238	315-0750-00			RES,FXD,FILM:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A10R240	321-0139-00			RES,FXD,FILM:274 OHM,1%,0.125W,TC=T0	07716	CEAD274R0F
A10R241	321-0201-00			RES,FXD,FILM:1.21K OHM,1%,0.125W,TC=T0	19701	5043ED1K210F
A10R242	315-0750-00			RES,FXD,FILM:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A10R243	315-0750-00			RES,FXD,FILM:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A10R244	321-0385-00			RES,FXD,FILM:100K OHM,1%,0.125W,TC=T0	19701	5033ED100K0F
A10R245	315-0180-00			RES,FXD,FILM:18 OHM,5%,0.25W	19701	5043CX18R00J
A10R250	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A10R251	315-0392-00	B010100	B011495	RES,FXD,FILM:3.9K OHM,5%,0.25W	57668	NTR25J-E03K9
A10R251	315-0152-00	B011496		RES,FXD,FILM:1.5K OHM,5%,0.25W	57668	NTR25J-E01K5
A10R252	315-0750-00			RES,FXD,FILM:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A10R253	315-0750-00			RES,FXD,FILM:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A10R254	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R255	315-0750-00			RES,FXD,FILM:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A10R260	315-0750-00			RES,FXD,FILM:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A10R261	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R262	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A10R267	315-0912-00			RES,FXD,FILM:9.1K OHM,5%,0.25W	57668	NTR25J-E09K1
A10R268	315-0152-00			RES,FXD,FILM:1.5K OHM,5%,0.25W	57668	NTR25J-E01K5
A10R269	315-0103-00	B010100	B014160	RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R269	315-0100-00	B014161		RES,FXD,FILM:10 OHM,5%,0.25W (2430 ONLY))	19701	5043CX10RR00J
A10R269	315-0103-00	B010100	B019999	RES,FXD,FILM:10K OHM,5%,0.25W (2430M ONLY)	19701	5043CX10K00J
A10R270	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R271	315-0152-00			RES,FXD,FILM:1.5K OHM,5%,0.25W	57668	NTR25J-E01K5
A10R275	315-0560-00			RES,FXD,FILM:56 OHM,5%,0.25W	57668	NTR25J-E56E0
A10R276	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R278	315-0750-00			RES,FXD,FILM:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A10R280	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R281	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A10R282	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A10R283	315-0151-00			RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A10R284	315-0750-00			RES,FXD,FILM:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A10R285	307-0542-00			RES NTWK,FXD,FI:(5)10K OHM,5%,0.125W	01121	106A1030R706A103
A10R286	315-0560-00			RES,FXD,FILM:56 OHM,5%,0.25W	57668	NTR25J-E56E0
A10R287	315-0560-00			RES,FXD,FILM:56 OHM,5%,0.25W	57668	NTR25J-E56E0
A10R288	315-0560-00			RES,FXD,FILM:56 OHM,5%,0.25W	57668	NTR25J-E56E0
A10R289	315-0750-00			RES,FXD,FILM:75 OHM,5%,0.25W	57668	NTR25J-E75E0

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A10R290	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R291	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R292	315-0151-00			RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A10R293	315-0151-00			RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A10R294	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R295	315-0302-00			RES,FXD,FILM:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A10R296	315-0152-00			RES,FXD,FILM:1.5K OHM,5%,0.25W	57668	NTR25J-E01K5
A10R297	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R298	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A10R299	315-0104-00			RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K
A10R310	313-1220-00	B014162		RES,FXD,FILM:22 OHM,5%,0.2W	57668	TR20JE22E
A10R320	321-0085-00			RES,FXD,FILM:75 OHM,1%,0.125W,TC=T0	57668	CRB14FXE 75 OHM
A10R340	321-0149-00			RES,FXD,FILM:348 OHM,1%,0.125W,TC=T0	07716	CEAD348R0F
A10R341	321-0385-00			RES,FXD,FILM:100K OHM,1%,0.125W,TC=T0	19701	5033ED100K0F
A10R342	321-0385-00			RES,FXD,FILM:100K OHM,1%,0.125W,TC=T0	19701	5033ED100K0F
A10R343	321-0385-00			RES,FXD,FILM:100K OHM,1%,0.125W,TC=T0	19701	5033ED100K0F
A10R345	315-0181-00			RES,FXD,FILM:180 OHM,5%,0.25W	57668	NTR25J-E180E
A10R350	307-0717-00			RES NTWK,FXD,FI:4,100 OHM,2%,0.3W	11236	750-83-R100
A10R352	315-0302-00	B010100	B010808	RES,FXD,FILM:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A10R353	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R354	315-0302-00			RES,FXD,FILM:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A10R355	315-0302-00			RES,FXD,FILM:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A10R361	315-0750-00			RES,FXD,FILM:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A10R365	315-0390-00	B010100	B010419	RES,FXD,FILM:39 OHM,5%,0.25W	57668	NTR25J-E39E0
A10R365	315-0101-00	B010420		RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A10R366	315-0390-00			RES,FXD,FILM:39 OHM,5%,0.25W	57668	NTR25J-E39E0
A10R368	315-0560-00			RES,FXD,FILM:56 OHM,5%,0.25W	57668	NTR25J-E56E0
A10R370	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A10R371	307-0546-00			RES NTWK,FXD,FI:5,75OHM,5%,0.15 W	11236	750/770-61-R75
A10R372	315-0471-00	B010100	B014160	RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A10R372	315-0391-00	B014161		RES,FXD,FILM:390 OHM,5%,0.25W (2430 ONLY)	57668	NTR25J-E390E
A10R372	315-0471-00	B010100	B019999	RES,FXD,FILM:470 OHM,5%,0.25W (2430M ONLY)	57668	NTR25J-E470E
A10R373	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R374	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R375	315-0471-00	B010100	B014160	RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A10R375	315-0391-00	B014161		RES,FXD,FILM:390 OHM,5%,0.25W (2430 ONLY)	57668	NTR25J-E390E
A10R375	315-0471-00	B010100	B019999	RES,FXD,FILM:470 OHM,5%,0.25W (2430M ONLY)	57668	NTR25J-E470E
A10R376	315-0181-00	B010100	B014160	RES,FXD,FILM:180 OHM,5%,0.25W	57668	NTR25J-E180E
A10R376	315-0201-00	B014161		RES,FXD,FILM:200 OHM,5%,0.25W (2430 ONLY)	57668	NTR25J-E200E
A10R376	315-0181-00	B010100	B019999	RES,FXD,FILM:180 OHM,5%,0.25W (2430M ONLY)	57668	NTR25J-E180E
A10R377	315-0181-00	B010100	B014160	RES,FXD,FILM:180 OHM,5%,0.25W	57668	NTR25J-E180E
A10R377	315-0201-00	B014161		RES,FXD,FILM:200 OHM,5%,0.25W (2430 ONLY)	57668	NTR25J-E200E
A10R377	315-0181-00	B010100	B019999	RES,FXD,FILM:180 OHM,5%,0.25W (2430M ONLY)	57668	NTR25J-E180E
A10R378	321-0385-00			RES,FXD,FILM:100K OHM,1%,0.125W,TC=T0	19701	5033ED100K0F
A10R379	321-0385-00	B010100	B014161	RES,FXD,FILM:100K OHM,1%,0.125W,TC=T0	19701	5033ED100K0F
A10R379	321-0387-00	B014162		RES,FXD,FILM:105K OHM,1%,0.125W,TC=T0	07716	CEAD10502F
A10R380	315-0122-00			RES,FXD,FILM:1.2K OHM,5%,0.25W	57668	NTR25J-E01K2
A10R381	315-0362-00			RES,FXD,FILM:3.6K OHM,5%,0.25W	19701	5043CX3K600J
A10R382	315-0511-00			RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J
A10R383	315-0750-00			RES,FXD,FILM:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A10R384	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R385	315-0511-00			RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J

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A10R386	315-0151-00			RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A10R387	315-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.25W	57668	NTR25J-E02K2
A10R388	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A10R389	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A10R390	315-0301-00			RES,FXD,FILM:300 OHM,5%,0.25W	57668	NTR25J-E300E
A10R391	315-0390-00			RES,FXD,FILM:39 OHM,5%,0.25W	57668	NTR25J-E39E0
A10R392	321-0459-00			RES,FXD,FILM:590K OHM,1%,0.125W,TC=T0	19701	5043ED590K0F
A10R393	315-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.25W	57668	NTR25J-E02K2
A10R394	315-0302-00			RES,FXD,FILM:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A10R395	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R396	315-0302-00			RES,FXD,FILM:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A10R397	315-0152-00			RES,FXD,FILM:1.5K OHM,5%,0.25W	57668	NTR25J-E01K5
A10R398	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R399	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A10R420	315-0121-00			RES,FXD,FILM:120 OHM,5%,0.25W	19701	5043CX120R0J
A10R421	321-0193-00	B010100	B012064	RES,FXD,FILM:1K OHM,1%,0.125W,TC=T0	19701	5033ED1K00F
A10R421	321-0188-00	B012065		RES,FXD,FILM:887 OHM,1%,0.125W,TC=T0	07716	CEAD887R0F
A10R422	315-0152-00			RES,FXD,FILM:1.5K OHM,5%,0.25W	57668	NTR25J-E01K5
A10R425	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A10R430	321-0255-00			RES,FXD,FILM:4.42K OHM,1%,0.125W,TC=T0	19701	5033ED4K420F
A10R435	315-0180-00			RES,FXD,FILM:18 OHM,5%,0.25W	19701	5043CX18R00J
A10R440	321-0149-00			RES,FXD,FILM:348 OHM,1%,0.125W,TC=T0	07716	CEAD348R0F
A10R441	321-0385-00			RES,FXD,FILM:100K OHM,1%,0.125W,TC=T0	19701	5033ED100K0F
A10R450	307-0717-00			RES NTWK,FXD,FI:4,100 OHM,2%,0.3W	11236	750-83-R100
A10R452	315-0302-00			RES,FXD,FILM:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A10R453	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R454	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R455	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R456	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R457	321-0169-00	B012727		RES,FXD,FILM:562 OHM,1%,0.125W,TC=T0	07716	CEAD562R0F
A10R458	311-2229-00	B012727		RES,VAR,NONWW:TRMR,250 OHM,20%,0.5W LINEAR	TK1450	GF06UT 250
A10R459	321-0210-00	B012727		RES,FXD,FILM:1.50K OHM,1%,0.125W,TC=T0	19701	5033ED1K50F
A10R460	321-0210-00	B012727		RES,FXD,FILM:1.50K OHM,1%,0.125W,TC=T0	19701	5033ED1K50F
A10R461	315-0302-00			RES,FXD,FILM:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A10R462	315-0510-00			RES,FXD,FILM:51 OHM,5%,0.25W	19701	5043CX51R00J
A10R465	315-0390-00	B010100	B010419	RES,FXD,FILM:39 OHM,5%,0.25W	57668	NTR25J-E39E0
A10R465	315-0101-00	B010420		RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A10R466	315-0390-00	B010100	B010419	RES,FXD,FILM:39 OHM,5%,0.25W	57668	NTR25J-E39E0
A10R466	315-0101-00	B010420		RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A10R467	321-0385-00			RES,FXD,FILM:100K OHM,1%,0.125W,TC=T0	19701	5033ED100K0F
A10R468	321-0385-00			RES,FXD,FILM:100K OHM,1%,0.125W,TC=T0	19701	5033ED100K0F
A10R470	307-0489-00			RES NTWK,FXD,FI:7,100 OHM,20%,1.0W	11236	750-81-R100
A10R471	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A10R475	311-2227-00	B010100	B012726	RES,VAR,NONWW:TRMR,100 OHM,20%,0.5W LINEAR	TK1450	GF06UT 100
A10R475	311-2229-00	B012727		RES,VAR,NONWW:TRMR,250 OHM,20%,0.5W LINEAR	TK1450	GF06UT 250
A10R477	315-0750-00			RES,FXD,FILM:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A10R478	315-0750-00			RES,FXD,FILM:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A10R480	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R481	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R482	315-0151-00			RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A10R483	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25W	57668	NTR25J-E 2K
A10R484	315-0750-00			RES,FXD,FILM:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A10R485	315-0750-00			RES,FXD,FILM:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A10R486	315-0180-00			RES,FXD,FILM:18 OHM,5%,0.25W	19701	5043CX18R00J
A10R487	315-0180-00			RES,FXD,FILM:18 OHM,5%,0.25W	19701	5043CX18R00J
A10R488	315-0180-00			RES,FXD,FILM:18 OHM,5%,0.25W	19701	5043CX18R00J
A10R489	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A10R490	315-0151-00			RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E

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A10R491	315-0151-00			RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A10R492	315-0104-00			RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K
A10R493	321-0459-00			RES,FXD,FILM:590K OHM,1%,0.125W,TC=T0	19701	5043ED590K0F
A10R494	315-0301-00			RES,FXD,FILM:300 OHM,5%,0.25W	57668	NTR25J-E300E
A10R495	315-0390-00			RES,FXD,FILM:39 OHM,5%,0.25W	57668	NTR25J-E39E0
A10R496	315-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.25W	57668	NTR25J-E02K2
A10R497	315-0151-00			RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A10R498	315-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.25W	57668	NTR25J-E02K2
A10R499	315-0132-00			RES,FXD,FILM:1.3K OHM,5%,0.25W	57668	NTR25J-E01K3
A10R500	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A10R501	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A10R502	315-0272-00			RES,FXD,FILM:2.7K OHM,5%,0.25W	57668	NTR25J-E02K7
A10R510	315-0103-00	B010100	B014160	RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R510	315-0100-00	B014161		RES,FXD,FILM:10 OHM,5%,0.25W (2430 ONLY)	19701	5043CX10RR00J
A10R510	315-0103-00	B010100	B019999	RES,FXD,FILM:10K OHM,5%,0.25W (2430M ONLY)	19701	5043CX10K00J
A10R512	301-0361-00			RES,FXD,FILM:360 OHM,5%,0.5W	19701	5053CX360R0J
A10R515	321-0054-00			RES,FXD,FILM:35.7 OHM,0.5%,0.125W,TC=T0 MI	91637	CMF55116G35R70F
A10R516	321-0122-00			RES,FXD,FILM:182 OHM,1%,0.125W,TC=T0	19701	5033ED182R0F
A10R520	321-0130-00			RES,FXD,FILM:221 OHM,1%,0.125W,TC=T0	19701	5043ED221R0F
A10R521	321-0193-00	B010100	B012064	RES,FXD,FILM:1K OHM,1%,0.125W,TC=T0	19701	5033ED1K00F
A10R521	321-0188-00	B012065		RES,FXD,FILM:887 OHM,1%,0.125W,TC=T0	07716	CEAD887R0F
A10R522	315-0152-00			RES,FXD,FILM:1.5K OHM,5%,0.25W	57668	NTR25J-E01K5
A10R527	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R528	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R529	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R530	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A10R531	315-0103-00	B010100	B014160	RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R531	315-0100-00	B014161		RES,FXD,FILM:10 OHM,5%,0.25W (2430 ONLY)	19701	5043CX10RR00J
A10R531	315-0103-00	B010100	B019999	RES,FXD,FILM:10K OHM,5%,0.25W (2430M ONLY)	19701	5043CX10K00J
A10R532	315-0151-00			RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A10R533	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A10R534	315-0150-00			RES,FXD,FILM:15 OHM,5%,0.25W	19701	5043CX15R00J
A10R535	321-0289-00	B010100	B014160	RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A10R535	321-0292-00	B014161		RES,FXD,FILM:10.7K OHM,1%,0.125W,TC=T0 (2430 ONLY)	07716	CEAD10701F
A10R535	321-0289-00	B010100	B019999	RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0 (2430M ONLY)	19701	5033ED10K0F
A10R536	321-0330-00	B010100	B014160	RES,FXD,FILM:26.7K OHM,1%,0.125W,TC=T0	07716	CEAD26701F
A10R536	321-1332-00	B014161		RES,FXD,FILM:28.4K OHM,1%,0.125W,TC=T0 (2430 ONLY))	19701	5033ED28K40F
A10R536	321-0330-00	B010100	B019999	RES,FXD,FILM:26.7K OHM,1%,0.125W,TC=T0 (2430M ONLY)	07716	CEAD26701F
A10R540	321-0385-00			RES,FXD,FILM:100K OHM,1%,0.125W,TC=T0	19701	5033ED100K0F
A10R541	321-0385-00			RES,FXD,FILM:100K OHM,1%,0.125W,TC=T0	19701	5033ED100K0F
A10R542	321-0385-00			RES,FXD,FILM:100K OHM,1%,0.125W,TC=T0	19701	5033ED100K0F
A10R543	315-0750-00			RES,FXD,FILM:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A10R544	315-0750-00			RES,FXD,FILM:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A10R545	321-0289-00	B010100	B014160	RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A10R545	321-0292-00	B014161		RES,FXD,FILM:10.7K OHM,1%,0.125W,TC=T0 (2430 ONLY)	07716	CEAD10701F
A10R545	321-0289-00	B010100	B019999	RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0 (2430M ONLY)	19701	5033ED10K0F
A10R546	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A10R547	315-0150-00			RES,FXD,FILM:15 OHM,5%,0.25W	19701	5043CX15R00J
A10R548	315-0102-00	B011410	B012726	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R550	315-0681-00			RES,FXD,FILM:680 OHM,5%,0.25W	57668	NTR25J-E680E

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A10R551	315-0151-00			RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A10R552	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R553	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R554	315-0302-00			RES,FXD,FILM:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A10R555	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R556	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R557	315-0302-00			RES,FXD,FILM:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A10R558	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R560	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R561	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R562	315-0302-00			RES,FXD,FILM:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A10R564	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R565	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A10R566	321-0260-00			RES,FXD,FILM:4.99K OHM,1%,0.125W,TC=T0	19701	5033ED4K990F
A10R567	321-0385-00			RES,FXD,FILM:100K OHM,1%,0.125W,TC=T0	19701	5033ED100K0F
A10R568	321-0385-00			RES,FXD,FILM:100K OHM,1%,0.125W,TC=T0	19701	5033ED100K0F
A10R571	315-0750-00			RES,FXD,FILM:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A10R572	315-0750-00			RES,FXD,FILM:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A10R573	315-0750-00			RES,FXD,FILM:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A10R574	315-0750-00			RES,FXD,FILM:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A10R575	315-0750-00			RES,FXD,FILM:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A10R580	315-0132-00			RES,FXD,FILM:1.3K OHM,5%,0.25W	57668	NTR25J-E01K3
A10R581	315-0511-00			RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J
A10R584	315-0511-00			RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J
A10R585	321-0318-00			RES,FXD,FILM:20.0K OHM,1%,0.125W,TC=T0	19701	5033ED20K00F
A10R586	321-0335-00			RES,FXD,FILM:30.1K OHM,1%,0.125W,TC=T0	57668	RB14FXE30K1
A10R587	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R588	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A10R590	321-0152-00			RES,FXD,FILM:374 OHM,1%,0.125W,TC=T0	07716	CEAD374R0F
A10R592	315-0152-00			RES,FXD,FILM:1.5K OHM,5%,0.25W	57668	NTR25J-E01K5
A10R594	321-0152-00			RES,FXD,FILM:374 OHM,1%,0.125W,TC=T0	07716	CEAD374R0F
A10R595	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A10R596	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A10R598	315-0152-00			RES,FXD,FILM:1.5K OHM,5%,0.25W	57668	NTR25J-E01K5
A10R599	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A10R600	307-0706-00			RES NTWK,FXD,FI:4,10K OHM,2%,0.2W EA	01121	208B103
A10R601	307-0542-00			RES NTWK,FXD,FI:(5)10K OHM,5%,0.125W	01121	106A1030R706A103
A10R612	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A10R613	315-0561-00			RES,FXD,FILM:560 OHM,5%,0.25W	19701	5043CX560R0J
A10R614	315-0391-00			RES,FXD,FILM:390 OHM,5%,0.25W	57668	NTR25J-E390E
A10R615	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R622	307-0108-00			RES,FXD,CMPSN:6.8 OHM,5%,0.25W	01121	CB68G5
A10R623	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A10R624	315-0561-00			RES,FXD,FILM:560 OHM,5%,0.25W	19701	5043CX560R0J
A10R625	315-0391-00			RES,FXD,FILM:390 OHM,5%,0.25W	57668	NTR25J-E390E
A10R626	321-0264-00			RES,FXD,FILM:5.49K OHM,1%,0.125W,TC=T0	07716	CEAD54900C
A10R627	321-0264-00			RES,FXD,FILM:5.49K OHM,1%,0.125W,TC=T0	07716	CEAD54900C
A10R628	321-0295-00			RES,FXD,FILM:11.5K OHM,1%,0.125W,TC=T0	07716	CEAD11501F
A10R631	315-0151-00			RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A10R632	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A10R633	315-0150-00			RES,FXD,FILM:15 OHM,5%,0.25W	19701	5043CX15R00J
A10R634	321-0264-00			RES,FXD,FILM:5.49K OHM,1%,0.125W,TC=T0	07716	CEAD54900C
A10R635	321-0330-00	B010100	B014160	RES,FXD,FILM:26.7K OHM,1%,0.125W,TC=T0	07716	CEAD26701F
A10R635	321-1332-00	B014161		RES,FXD,FILM:28.4K OHM,1%,0.125W,TC=T0 (2430 ONLY)	19701	5033ED28K40F
A10R635	321-0330-00	B010100	B019999	RES,FXD,FILM:26.7K OHM,1%,0.125W,TC=T0 (2430M ONLY)	07716	CEAD26701F
A10R636	321-0289-00	B010100	B014160	RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F

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A10R636	321-0292-00	B014161		RES,FXD,FILM:10.7K OHM,1%,0.125W,TC=T0 (2430 ONLY)	07716	CEAD10701F
A10R636	321-0289-00	B010100	B019999	RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0 (2430M ONLY)	19701	5033ED10K0F
A10R637	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A10R639	321-0260-00			RES,FXD,FILM:4.99K OHM,1%,0.125W,TC=T0	19701	5033ED4K990F
A10R640	321-0330-00	B010100	B014160	RES,FXD,FILM:26.7K OHM,1%,0.125W,TC=T0	07716	CEAD26701F
A10R640	321-1332-00	B014161		RES,FXD,FILM:28.4K OHM,1%,0.125W,TC=T0 (2430 ONLY)	19701	5033ED28K40F
A10R640	321-0330-00	B010100	B019999	RES,FXD,FILM:26.7K OHM,1%,0.125W,TC=T0 (2430M ONLY)	07716	CEAD26701F
A10R641	321-0330-00	B010100	B014160	RES,FXD,FILM:26.7K OHM,1%,0.125W,TC=T0	07716	CEAD26701F
A10R641	321-1332-00	B014161		RES,FXD,FILM:28.4K OHM,1%,0.125W,TC=T0 (2430 ONLY)	19701	5033ED28K40F
A10R641	321-0330-00	B010100	B019999	RES,FXD,FILM:26.7K OHM,1%,0.125W,TC=T0 (2430M ONLY)	07716	CEAD26701F
A10R642	321-0289-00	B010100	B014160	RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A10R642	321-0292-00	B014161		RES,FXD,FILM:10.7K OHM,1%,0.125W,TC=T0 (2430 ONLY)	07716	CEAD10701F
A10R642	321-0289-00	B010100	B019999	RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0 (2430M ONLY)	19701	5033ED10K0F
A10R643	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A10R646	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A10R647	315-0150-00			RES,FXD,FILM:15 OHM,5%,0.25W	19701	5043CX15R00J
A10R648	315-0153-00			RES,FXD,FILM:15K OHM,5%,0.25W	19701	5043CX15K00J
A10R649	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A10R650	315-0102-00	B011410		RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R651	315-0151-00			RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A10R652	321-0344-00			RES,FXD,FILM:37.4K OHM,1%,0.125W,TC=T0	19701	5033ED 37K40F
A10R653	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A10R654	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R655	321-0332-07			RES,FXD,FILM:28.0K OHM,0.1%,0.125W,TC=T9	19701	5033RE28K00B
A10R656	321-0926-07			RES,FXD,FILM:4K OHM,0.1%,0.125W,TC=T9	19701	5033RE4K00B
A10R660	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R661	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A10R662	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A10R663	321-0155-00			RES,FXD,FILM:402 OHM,1%,0.125W,TC=T0	07716	CEAD402R0F
A10R664	321-0155-00			RES,FXD,FILM:402 OHM,1%,0.125W,TC=T0	07716	CEAD402R0F
A10R665	321-0128-00			RES,FXD,FILM:210 OHM,1%,0.125W,TC=T0	07716	CEAD210R0F
A10R666	315-0682-00			RES,FXD,FILM:6.8K OHM,5%,0.25W	57668	NTR25J-E06K8
A10R667	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25W	57668	NTR25J-E 2K
A10R668	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R669	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25W	57668	NTR25J-E 2K
A10R670	315-0331-00			RES,FXD,FILM:330 OHM,5%,0.25W	57668	NTR25J-E330E
A10R671	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R672	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25W	57668	NTR25J-E 2K
A10R673	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R674	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25W	57668	NTR25J-E 2K
A10R675	315-0100-00	B010322		RES,FXD,FILM:10 OHM,5%,0.25W	19701	5043CX10RR00J
A10R676	315-0331-00			RES,FXD,FILM:330 OHM,5%,0.25W	57668	NTR25J-E330E
A10R677	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R678	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25W	57668	NTR25J-E 2K
A10R679	321-0226-00	B010100	B010126	RES,FXD,FILM:2.21K OHM,1%,0.125W,TC=T0	01121	RNK2211F
A10R679	321-0230-00	B010127	B011409	RES,FXD,FILM:2.43K OHM,1%,0.125W,TC=T0	19701	5043ED2K430F
A10R679	321-0222-00	B011410	B013501	RES,FXD,FILM:2.00K OHM,1%,0.125W,TC=T0	19701	5033ED2K00F
A10R679	321-0210-00	B013502	B014161	RES,FXD,FILM:1.50K OHM,1%,0.125W,TC=T0	19701	5033ED1K50F
A10R679	321-0222-00	B014162		RES,FXD,FILM:2.00K OHM,1%,0.125W,TC=T0 (NOMINAL VALUE)(2430 ONLY)	19701	5033ED2K00F
A10R679	321-0233-00	B010420		RES,FXD,FILM:2.61K OHM,1%,0.125W,TC=T0	07716	CEAD26100F

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A10R679	321-0227-00	B010823		RES,FXD,FILM:2.26K OHM,1%,0.125W,TC=T0	01121	RNK2261F
A10R679	321-0235-00	B010823		RES,FXD,FILM:2.74K OHM,1%,0.125W,TC=T0	07716	CEAD27400F
A10R679	321-0236-00	B010823		RES,FXD,FILM:2.80K OHM,1%,0.125W,TC=T0 (TEST SELECTABLE) (2430)	07716	CEAD28000F
A10R679	321-0222-00	B010100	B010126	RES,FXD,FILM:2.00K OHM,1%,0.125W,TC=T0	19701	5033ED2K00F
A10R679	321-0210-00	B010127	B019999	RES,FXD,FILM:1.50K OHM,1%,0.125W,TC=T0 (2430M ONLY)	19701	5033ED1K50F
A10R680	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25W	57668	NTR25J-E 2K
A10R681	315-0100-00	B010322		RES,FXD,FILM:10 OHM,5%,0.25W	19701	5043CX10RR00J
A10R682	315-0331-00			RES,FXD,FILM:330 OHM,5%,0.25W	57668	NTR25J-E330E
A10R683	321-0210-00	B010100	B010126	RES,FXD,FILM:1.50K OHM,1%,0.125W,TC=T0	19701	5033ED1K50F
A10R683	321-0205-00	B010127		RES,FXD,FILM:1.33K OHM,1%,0.125W,TC=T0	19701	5033ED1K330F
A10R684	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R685	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25W	57668	NTR25J-E 2K
A10R686	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25W	57668	NTR25J-E 2K
A10R687	321-0250-00			RES,FXD,FILM:3.92K OHM,1%,0.125W,TC=T0	07716	CEAD39200F
A10R688	311-2231-00	B011410	B013501	RES,VAR,NONWW:TRMR,1K OHM,20%,0.5W LINEAR	TK1450	GF06UT 1K
A10R688	311-2232-00	B013502		RES,VAR,NONWW:TRMR,2K OHM,20%,0.5W LINEAR (2430)	TK1450	GF06UT 2K
A10R688	311-2231-00	B010100	B010126	RES,VAR,NONWW:TRMR,1K OHM,20%,0.5W LINEAR	TK1450	GF06UT 1K
A10R688	311-2232-00	B010127		RES,VAR,NONWW:TRMR,2K OHM,20%,0.5W LINEAR (2430M)	TK1450	GF06UT 2K
A10R700	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A10R710	307-0446-00			RES NTWK,FXD,FI:10K OHM,20%,(9)RES	11236	750-101-R10K
A10R726	321-0295-00			RES,FXD,FILM:11.5K OHM,1%,0.125W,TC=T0	07716	CEAD11501F
A10R730	321-0264-00			RES,FXD,FILM:5.49K OHM,1%,0.125W,TC=T0	07716	CEAD54900C
A10R731	321-0295-00			RES,FXD,FILM:11.5K OHM,1%,0.125W,TC=T0	07716	CEAD11501F
A10R732	321-0295-00			RES,FXD,FILM:11.5K OHM,1%,0.125W,TC=T0	07716	CEAD11501F
A10R734	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A10R735	321-0260-00			RES,FXD,FILM:4.99K OHM,1%,0.125W,TC=T0	19701	5033ED4K990F
A10R736	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A10R740	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A10R741	321-0260-00			RES,FXD,FILM:4.99K OHM,1%,0.125W,TC=T0	19701	5033ED4K990F
A10R742	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A10R743	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A10R750	315-0153-00			RES,FXD,FILM:15K OHM,5%,0.25W	19701	5043CX15K00J
A10R751	321-0344-00			RES,FXD,FILM:37.4K OHM,1%,0.125W,TC=T0	19701	5033ED 37K40F
A10R752	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A10R753	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A10R760	315-0753-00			RES,FXD,FILM:75K OHM,5%,0.25W	57668	NTR25J-E75K0
A10R761	321-0296-00			RES,FXD,FILM:11.8K OHM,1%,0.125W,TC=T0	07716	CEAD11801F
A10R762	321-0193-00			RES,FXD,FILM:1K OHM,1%,0.125W,TC=T0	19701	5033ED1K00F
A10R763	321-0210-00			RES,FXD,FILM:1.50K OHM,1%,0.125W,TC=T0	19701	5033ED1K50F
A10R764	321-0277-00			RES,FXD,FILM:7.50K OHM,1%,0.125W,TC=T0	24546	NA55D7501F
A10R765	321-0254-00			RES,FXD,FILM:4.32K OHM,1%,0.125W,TC=T0	07716	CEAD43200F
A10R766	321-0176-00			RES,FXD,FILM:665 OHM,1%,0.125W,TC=T0	07716	CEAD665R0F
A10R767	321-0226-00	B010100	B010126	RES,FXD,FILM:2.21K OHM,1%,0.125W,TC=T0	01121	RNK2211F
A10R767	321-0230-00	B010127	B011409	RES,FXD,FILM:2.43K OHM,1%,0.125W,TC=T0	19701	5043ED2K430F
A10R767	321-0222-00	B011410	B013501	RES,FXD,FILM:2.00K OHM,1%,0.125W,TC=T0	19701	5033ED2K00F
A10R767	321-0210-00	B013502	B014161	RES,FXD,FILM:1.50K OHM,1%,0.125W,TC=T0	19701	5033ED1K50F
A10R767	321-0222-00	B014162		RES,FXD,FILM:2.00K OHM,1%,0.125W,TC=T0 (NOMINAL VALUE)(2430 ONLY)	19701	5033ED2K00F
A10R767	321-0233-00	B010420		RES,FXD,FILM:2.61K OHM,1%,0.125W,TC=T0	07716	CEAD26100F
A10R767	321-0227-00	B010823		RES,FXD,FILM:2.26K OHM,1%,0.125W,TC=T0	01121	RNK2261F
A10R767	321-0235-00	B010823		RES,FXD,FILM:2.74K OHM,1%,0.125W,TC=T0	07716	CEAD27400F
A10R767	321-0236-00	B010823		RES,FXD,FILM:2.80K OHM,1%,0.125W,TC=T0 (TEST SELECTABLE) (2430)	07716	CEAD28000F

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A10R767	321-0222-00	B010100	B010126	RES,FXD,FILM:2.00K OHM,1%,0.125W,TC=T0	19701	5033ED2K00F
A10R767	321-0210-00	B010127	B019999	RES,FXD,FILM:1.50K OHM,1%,0.125W,TC=T0 (2430M)	19701	5033ED1K50F
A10R768	311-2231-00	B011410	B013501	RES,VAR,NONWW:TRMR,1K OHM,20%,0.5W LINEAR	TK1450	GF06UT 1K
A10R768	311-2232-00	B013502		RES,VAR,NONWW:TRMR,2K OHM,20%,0.5W LINEAR (2430)	TK1450	GF06UT 2K
A10R768	311-2231-00	B010100	B010126	RES,VAR,NONWW:TRMR,1K OHM,20%,0.5W LINEAR	TK1450	GF06UT 1K
A10R768	311-2232-00	B010127		RES,VAR,NONWW:TRMR,2K OHM,20%,0.5W LINEAR (2430M)	TK1450	GF06UT 2K
A10R769	311-2231-00	B011410	B013501	RES,VAR,NONWW:TRMR,1K OHM,20%,0.5W LINEAR	TK1450	GF06UT 1K
A10R769	311-2232-00	B013502		RES,VAR,NONWW:TRMR,2K OHM,20%,0.5W LINEAR (2430)	TK1450	GF06UT 2K
A10R769	311-2231-00	B010100	B010126	RES,VAR,NONWW:TRMR,1K OHM,20%,0.5W LINEAR	TK1450	GF06UT 1K
A10R769	311-2232-00	B010127		RES,VAR,NONWW:TRMR,2K OHM,20%,0.5W LINEAR (2430M)	TK1450	GF06UT 2K
A10R770	321-0254-00			RES,FXD,FILM:4.32K OHM,1%,0.125W,TC=T0	07716	CEAD43200F
A10R771	321-0176-00			RES,FXD,FILM:665 OHM,1%,0.125W,TC=T0	07716	CEAD665R0F
A10R772	315-0100-00	B010322		RES,FXD,FILM:10 OHM,5%,0.25W	19701	5043CX10RR00J
A10R773	315-0331-00			RES,FXD,FILM:330 OHM,5%,0.25W	57668	NTR25J-E330E
A10R774	321-0129-00			RES,FXD,FILM:215 OHM,1%,0.125W,TC=T0	07716	CEAD215R0F
A10R775	321-0210-00	B010100	B010126	RES,FXD,FILM:1.50K OHM,1%,0.125W,TC=T0	19701	5033ED1K50F
A10R775	321-0205-00	B010127		RES,FXD,FILM:1.33K OHM,1%,0.125W,TC=T0	19701	5033ED1K330F
A10R776	321-0254-00			RES,FXD,FILM:4.32K OHM,1%,0.125W,TC=T0	07716	CEAD43200F
A10R777	321-0176-00			RES,FXD,FILM:665 OHM,1%,0.125W,TC=T0	07716	CEAD665R0F
A10R778	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R779	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25W	57668	NTR25J-E 2K
A10R780	321-0254-00			RES,FXD,FILM:4.32K OHM,1%,0.125W,TC=T0	07716	CEAD43200F
A10R781	321-0176-00			RES,FXD,FILM:665 OHM,1%,0.125W,TC=T0	07716	CEAD665R0F
A10R782	321-0129-00			RES,FXD,FILM:215 OHM,1%,0.125W,TC=T0	07716	CEAD215R0F
A10R783	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25W	57668	NTR25J-E 2K
A10R784	315-0100-00	B010322		RES,FXD,FILM:10 OHM,5%,0.25W	19701	5043CX10RR00J
A10R785	315-0331-00			RES,FXD,FILM:330 OHM,5%,0.25W	57668	NTR25J-E330E
A10R786	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25W	57668	NTR25J-E 2K
A10R788	315-0391-00			RES,FXD,FILM:390 OHM,5%,0.25W	57668	NTR25J-E390E
A10R789	315-0391-00			RES,FXD,FILM:390 OHM,5%,0.25W	57668	NTR25J-E390E
A10R790	315-0821-00			RES,FXD,FILM:820 OHM,5%,0.25W	19701	5043CX820R0J
A10R800	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R809	313-1471-00	B014161		RES,FXD,FILM:470 OHM,5%,0.2W (2430 ONLY)	57668	TR20JE 470E
A10R810	307-0706-00			RES NTWK,FXD,FI:4,10K OHM,2%,0.2W EA	01121	208B103
A10R811	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R812	321-0148-00			RES,FXD,FILM:340 OHM,1%,0.125W,TC=T0	07716	CEAD340R0F
A10R813	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R814	321-0296-00			RES,FXD,FILM:11.8K OHM,1%,0.125W,TC=T0	07716	CEAD11801F
A10R815	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A10R816	321-0311-00			RES,FXD,FILM:16.9K OHM,1%,0.125W,TC=T0	07716	CEAC16901F
A10R817	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A10R818	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A10R820	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R821	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R822	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R823	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A10R824	315-0912-00			RES,FXD,FILM:9.1K OHM,5%,0.25W	57668	NTR25J-E09K1
A10R825	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R828	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R830	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A10R831	321-0260-00			RES,FXD,FILM:4.99K OHM,1%,0.125W,TC=T0	19701	5033ED4K990F
A10R832	321-0306-00			RES,FXD,FILM:15.0K OHM,1%,0.125W,TC=T0	19701	5033ED15J00F
A10R833	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A10R840	321-0306-00			RES,FXD,FILM:15.0K OHM,1%,0.125W,TC=T0	19701	5033ED15J00F
A10R841	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A10R850	315-0103-00	B010100	B014160	RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R850	315-0100-00	B014161		RES,FXD,FILM:10 OHM,5%,0.25W (2430 ONLY)	19701	5043CX10RR00J
A10R850	315-0103-00	B010100	B019999	RES,FXD,FILM:10K OHM,5%,0.25W (2430M ONLY)	19701	5043CX10K00J
A10R851	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R852	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R853	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R855	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R856	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R857	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R860	315-0123-00			RES,FXD,FILM:12K OHM,5%,0.25W	57668	NTR25J-E12K0
A10R861	321-0164-00			RES,FXD,FILM:499 OHM,1%,0.125W,TC=T0	19701	5033ED499R0F
A10R862	321-0254-00			RES,FXD,FILM:4.32K OHM,1%,0.125W,TC=T0	07716	CEAD43200F
A10R863	321-0176-00			RES,FXD,FILM:665 OHM,1%,0.125W,TC=T0	07716	CEAD665R0F
A10R867	321-0266-00	B010100	B010126	RES,FXD,FILM:5.76K OHM,1%,0.125W,TC=T0	19701	5033ED5K760F
A10R867	321-0230-00	B010127	B011409	RES,FXD,FILM:2.43K OHM,1%,0.125W,TC=T0	19701	5043ED2K430F
A10R867	321-0222-00	B011410	B013501	RES,FXD,FILM:2.00K OHM,1%,0.125W,TC=T0	19701	5033ED2K00F
A10R867	321-0210-00	B013502	B014161	RES,FXD,FILM:1.50K OHM,1%,0.125W,TC=T0	19701	5033ED1K50F
A10R867	321-0222-00	B014162		RES,FXD,FILM:2.00K OHM,1%,0.125W,TC=T0 (NOMINAL VALUE)(2430 ONLY)	19701	5033ED2K00F
A10R867	321-0233-00	B010420		RES,FXD,FILM:2.61K OHM,1%,0.125W,TC=T0	07716	CEAD26100F
A10R867	321-0227-00	B010823		RES,FXD,FILM:2.26K OHM,1%,0.125W,TC=T0	01121	RNK2261F
A10R867	321-0235-00	B010823		RES,FXD,FILM:2.74K OHM,1%,0.125W,TC=T0	07716	CEAD27400F
A10R867	321-0236-00	B010823		RES,FXD,FILM:2.80K OHM,1%,0.125W,TC=T0 (TEST SELECTABLE) (2430)	07716	CEAD28000F
A10R867	321-0222-00	B010100	B010126	RES,FXD,FILM:2.00K OHM,1%,0.125W,TC=T0	19701	5033ED2K00F
A10R867	321-0210-00	B010127	B019999	RES,FXD,FILM:1.50K OHM,1%,0.125W,TC=T0 (2430M ONLY)	19701	5033ED1K50F
A10R870	321-0254-00			RES,FXD,FILM:4.32K OHM,1%,0.125W,TC=T0	07716	CEAD43200F
A10R871	321-0176-00			RES,FXD,FILM:665 OHM,1%,0.125W,TC=T0	07716	CEAD665R0F
A10R872	321-0129-00			RES,FXD,FILM:215 OHM,1%,0.125W,TC=T0	07716	CEAD215R0F
A10R873	321-0210-00	B010100	B010126	RES,FXD,FILM:1.50K OHM,1%,0.125W,TC=T0	19701	5033ED1K50F
A10R873	321-0205-00	B010127		RES,FXD,FILM:1.33K OHM,1%,0.125W,TC=T0	19701	5033ED1K330F
A10R874	321-0254-00			RES,FXD,FILM:4.32K OHM,1%,0.125W,TC=T0	07716	CEAD43200F
A10R875	321-0176-00			RES,FXD,FILM:665 OHM,1%,0.125W,TC=T0	07716	CEAD665R0F
A10R876	307-0717-00			RES NTWK,FXD,FI:4,100 OHM,2%,0.3W	11236	750-83-R100
A10R877	311-2231-00	B011410	B013501	RES,VAR,NONWW:TRMR,1K OHM,20%,0.5W LINEAR	TK1450	GF06UT 1K
A10R877	311-2232-00	B013502		RES,VAR,NONWW:TRMR,2K OHM,20%,0.5W LINEAR (2430)	TK1450	GF06UT 2K
A10R877	311-2231-00	B010100	B010126	RES,VAR,NONWW:TRMR,1K OHM,20%,0.5W LINEAR	TK1450	GF06UT 1K
A10R877	311-2232-00	B010127		RES,VAR,NONWW:TRMR,2K OHM,20%,0.5W LINEAR (2430M)	TK1450	GF06UT 2K
A10R878	321-0226-00	B010100	B010126	RES,FXD,FILM:2.21K OHM,1%,0.125W,TC=T0	01121	RNK2211F
A10R878	321-0230-00	B010127	B011409	RES,FXD,FILM:2.43K OHM,1%,0.125W,TC=T0	19701	5043ED2K430F
A10R878	321-0222-00	B011410	B013501	RES,FXD,FILM:2.00K OHM,1%,0.125W,TC=T0	19701	5033ED2K00F
A10R878	321-0210-00	B013502	B014161	RES,FXD,FILM:1.50K OHM,1%,0.125W,TC=T0	19701	5033ED1K50F
A10R878	321-0222-00	B014162		RES,FXD,FILM:2.00K OHM,1%,0.125W,TC=T0 (NOMINAL VALUE)(2430 ONLY)	19701	5033ED2K00F
A10R878	321-0233-00	B010420		RES,FXD,FILM:2.61K OHM,1%,0.125W,TC=T0	07716	CEAD26100F
A10R878	321-0227-00	B010823		RES,FXD,FILM:2.26K OHM,1%,0.125W,TC=T0	01121	RNK2261F
A10R878	321-0235-00	B010823		RES,FXD,FILM:2.74K OHM,1%,0.125W,TC=T0	07716	CEAD27400F
A10R878	321-0236-00	B010823		RES,FXD,FILM:2.80K OHM,1%,0.125W,TC=T0 (TEST SELECTABLE) (2430)	07716	CEAD28000F
A10R878	321-0222-00	B010100	B010126	RES,FXD,FILM:2.00K OHM,1%,0.125W,TC=T0	19701	5033ED2K00F
A10R878	321-0210-00	B010127	B019999	RES,FXD,FILM:1.50K OHM,1%,0.125W,TC=T0 (2430M ONLY)	19701	5033ED1K50F

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A10R879	315-0391-00			RES,FXD,FILM:390 OHM,5%,0.25W	57668	NTR25J-E390E
A10R880	321-0254-00			RES,FXD,FILM:4.32K OHM,1%,0.125W,TC=TO	07716	CEAD43200F
A10R881	321-0176-00			RES,FXD,FILM:665 OHM,1%,0.125W,TC=TO	07716	CEAD665R0F
A10R882	321-0129-00			RES,FXD,FILM:215 OHM,1%,0.125W,TC=TO	07716	CEAD215R0F
A10R883	321-0210-00	B010100	B010126	RES,FXD,FILM:1.50K OHM,1%,0.125W,TC=TO	19701	5033ED1K50F
A10R883	321-0205-00	B010127		RES,FXD,FILM:1.33K OHM,1%,0.125W,TC=TO	19701	5033ED1K330F
A10R884	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R885	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25W	57668	NTR25J-E 2K
A10R886	307-0717-00			RES NTWK,FXD,FI:4,100 OHM,2%,0.3W	11236	750-83-R100
A10R887	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=TO	19701	5033ED10K0F
A10R888	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=TO	19701	5033ED10K0F
A10R889	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=TO	19701	5033ED10K0F
A10R890	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=TO	19701	5033ED10K0F
A10R891	315-0391-00			RES,FXD,FILM:390 OHM,5%,0.25W	57668	NTR25J-E390E
A10R1001	315-0240-00			RES,FXD,FILM:24 OHM,5%,0.25W	57668	NTR25J-E24E0
A10R1002	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A10R1003	315-0240-00			RES,FXD,FILM:24 OHM,5%,0.25W	57668	NTR25J-E24E0
A10R1004	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A10R1005	315-0474-00			RES,FXD,FILM:470K OHM,5%,0.25W (PART OF 119-1365-XX,ASSY NOT AVAIL)	19701	5043CX470K0J92U
A10R1006	315-0474-00			RES,FXD,FILM:470K OHM,5%,0.25W (PART OF 119-1365-XX,ASSY NOT AVAIL)	19701	5043CX470K0J92U
A10R1015	315-0100-00	B010175		RES,FXD,FILM:10 OHM,5%,0.25W	19701	5043CX10RR00J
A10R1015	315-0390-00			RES,FXD,FILM:39 OHM,5%,0.25W	57668	NTR25J-E39E0
A10R1015	----- -----	B010175		(R1015 IS TEST SELECTED)		
A10R1016	315-0100-00	B010175		RES,FXD,FILM:10 OHM,5%,0.25W	19701	5043CX10RR00J
A10R1016	315-0390-00			RES,FXD,FILM:39 OHM,5%,0.25W	57668	NTR25J-E39E0
A10R1016	----- -----	B010175		(R1016 IS TEST SELECTED)		
A10RT450	307-0125-00	B010100	B010808	RES,THERMAL:500 OHM,10%,NTC	15454	1DB501K-220-EC
A10S600	260-1421-00			SWITCH,PUSH:1 BTN,2 POLE,INSTRUMENT ID	59821	ORDER BY DESCR
A10S800	260-1421-00			SWITCH,PUSH:1 BTN,2 POLE,INSTRUMENT ID	59821	ORDER BY DESCR
A10S801	260-1421-00			SWITCH,PUSH:1 BTN,2 POLE,INSTRUMENT ID	59821	ORDER BY DESCR
A10T370	120-0478-00			XFMR,TOROID:	TK1345	ORDER BY DESCR
A10T371	120-0478-00			XFMR,TOROID:	TK1345	ORDER BY DESCR
A10TP163	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A10TP173	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A10TP174	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A10TP231	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A10TP281	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A10TP284	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A10TP291	131-0608-00	B010100	B012726	TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A10TP345	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A10TP347	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A10TP370	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A10TP568	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A10TP581	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A10TP585	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A10TP612	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A10TP650	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A10TP660	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A10TP832	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A10U100	155-0238-00			MICROCKT,LINEAR:TRIGGER PREAMP	80009	155-0238-00
A10U120	156-1149-01			MICROCKT,LINEAR:OPERATION AMP JFET INPUT	27014	AL160307
A10U140	156-0651-02			MICROCKT,DGTL:8-BIT PRL-OUT SER SHF RGTR	01295	SN74LS164NP3
A10U150	155-0239-01	B010100	B010582	MICROCKT,LINEAR:TRIGGER	80009	155-0239-01
A10U150	155-0239-02	B010583		MICROCKT,LINEAR:TRIGGER	80009	155-0239-02
A10U220	156-1245-00			MICROCKT,LINEAR:7 XSTR,NPN,SI,HV/HI CRNT	01295	ULN2003AN-P3
A10U221	156-0651-02			MICROCKT,DGTL:8-BIT PRL-OUT SER SHF RGTR	01295	SN74LS164NP3

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A10U230	156-0158-07			MICROCKT,LINEAR:DUAL OPNL AMPL,SCREENED	01295	MC1458JG4
A10U270	156-0651-02			MICROCKT,DGTL:8-BIT PRL-OUT SER SHF RGTR	01295	SN74LS164NP3
A10U271	156-0469-02			MICROCKT,DGTL:3/8 LINE DCDR,SCRN	01295	SN74LS138NP3
A10U272	156-0874-02			MICROCKT,DGTL:8 BIT ADDRESSABLE LATCH	04713	SN74LS259NDS
A10U280	156-0383-02			MICROCKT,DGTL:QUAD 2-INP NOR GATE,SCRN,	18324	N74LS02NB
A10U320	165-2235-00			MICROCKT,HYBRID:ASMBLD,LO NOISE VERT PREAMP	80009	165-2235-00
A10U340	----- -----			MICROCKT,HYBRID:PEAK DETECTOR (NOT REPLACEABLE - ORDER A10)		
A10U350	165-2074-00	B010100	B011409	MICROCKT,HYBRID:CCD/DRIVER ASSSEMBLY	80009	165-2074-00
A10U350	165-2074-01	B011410	B014160	MICROCKT,HYBRID:CCD/DRIVER ASSY	80009	165-2074-01
A10U350	165-2074-03	B014161		MICROCKT,HYBRID:CCD/DRIVER (2430 ONLY)	80009	165-2074-03
A10U350	165-2074-01	B010100	B019999	MICROCKT,HYBRID:CCD/DRIVER ASSY (2430M ONLY)	80009	165-2074-01
A10U360	156-1191-01			MICROCKT,LINEAR:DUAL BI-FET OP-AMP,8 DIP	80009	156-1191-01
A10U370	230-0002-50			INTEGRATED CKT:TRIGGER LOGIC,M299	80009	230-0002-50
A10U380	156-1723-00			MICROCKT,DGTL:QUAD 2 INPUT & GATE	04713	MC74F08 ND OR JD
A10U381	156-0518-00			MICROCKT,DGTL:PHASE FREQ DET,EMTR CPLLGC	04713	MC12040L
A10U390	156-1126-01			MICROCKT,LINEAR:VOLTAGE COMPARATOR,SELECTED	01295	LM311JG4
A10U420	165-2235-00			MICROCKT,HYBRID:ASMBLD,LO NOISE VERT PREAMP	80009	165-2235-00
A10U440	----- -----			MICROCKT,HYBRID:PEAK DETECTOR (NOT REPLACEABLE - ORDER A10)		
A10U450	165-2074-00	B010100	B011409	MICROCKT,HYBRID:CCD/DRIVER ASSSEMBLY	80009	165-2074-00
A10U450	165-2074-01	B011410	B014160	MICROCKT,HYBRID:CCD/DRIVER ASSY	80009	165-2074-01
A10U450	165-2074-03	B014161		MICROCKT,HYBRID:CCD/DRIVER (2430 ONLY)	80009	165-2074-03
A10U450	165-2074-01	B010100	B019999	MICROCKT,HYBRID:CCD/DRIVER ASSY (2430M ONLY)	80009	165-2074-01
A10U470	230-0001-50			INTEGRATED CKT:PHASE CLOCK TIMING,M299	80009	230-0001-50
A10U490	156-1126-01			MICROCKT,LINEAR:VOLTAGE COMPARATOR,SELECTED	01295	LM311JG4
A10U510	156-1245-00			MICROCKT,LINEAR:7 XSTR,NPN,SI,HV/HI CRNT	01295	ULN2003AN-P3
A10U511	156-0651-02			MICROCKT,DGTL:8-BIT PRL-OUT SER SHF RGTR	01295	SN74LS164NP3
A10U520	156-1245-00			MICROCKT,LINEAR:7 XSTR,NPN,SI,HV/HI CRNT	01295	ULN2003AN-P3
A10U530	156-0651-02			MICROCKT,DGTL:8-BIT PRL-OUT SER SHF RGTR	01295	SN74LS164NP3
A10U540	156-1200-01			MICROCKT,LINEAR:OPNL AMPL,QUAD BIFET	80009	156-1200-01
A10U560	156-1303-00			MICROCKT,LINEAR:QUAD ANALOG SW ARRAY	TK0987	SD5000N
A10U580	156-0158-07			MICROCKT,LINEAR:DUAL OPNL AMPL,SCREENED	01295	MC1458JG4
A10U590	156-1200-01			MICROCKT,LINEAR:OPNL AMPL,QUAD BIFET	80009	156-1200-01
A10U600	156-0513-03			MICROCKT,LINEAR:CMOS,8 CHAN ANALOG MUX	04713	MC14051BCL
A10U610	165-2024-00			MICROCKT,HYBRID:CURSOR AMPLIFIER	80009	165-2024-00
A10U630	156-1200-01			MICROCKT,LINEAR:OPNL AMPL,QUAD BIFET	80009	156-1200-01
A10U631	156-1200-01			MICROCKT,LINEAR:OPNL AMPL,QUAD BIFET	80009	156-1200-01
A10U640	156-1200-01			MICROCKT,LINEAR:OPNL AMPL,QUAD BIFET	80009	156-1200-01
A10U641	156-1200-01			MICROCKT,LINEAR:OPNL AMPL,QUAD BIFET	80009	156-1200-01
A10U650	156-1492-00			MICROCKT,LINEAR:OPNL AMPL MONO,FET-INP	24355	AD542JH
A10U651	156-0513-03			MICROCKT,LINEAR:CMOS,8 CHAN ANALOG MUX	04713	MC14051BCL
A10U660	156-1492-00			MICROCKT,LINEAR:OPNL AMPL MONO,FET-INP	24355	AD542JH
A10U661	156-1200-01			MICROCKT,LINEAR:OPNL AMPL,QUAD BIFET	80009	156-1200-01
A10U700	156-0789-02			MICROCKT,DGTL:8 BIT SR,PRL LOAD,SCREENED	04713	SN74LS165JDS
A10U770	156-1272-00			MICROCKT,LINEAR:DUAL OPERATIONAL AMPLIFIER	80009	156-1272-00
A10U775	156-1294-00			MICROCKT,LINEAR:NPN,5 XSTR ARRAY HI FREQ	02735	CA3127E
A10U780	156-1272-00			MICROCKT,LINEAR:DUAL OPERATIONAL AMPLIFIER	80009	156-1272-00
A10U785	156-1294-00			MICROCKT,LINEAR:NPN,5 XSTR ARRAY HI FREQ	02735	CA3127E
A10U810	156-1191-01			MICROCKT,LINEAR:DUAL BI-FET OP-AMP,8 DIP	80009	156-1191-01
A10U811	156-0513-03			MICROCKT,LINEAR:CMOS,8 CHAN ANALOG MUX	04713	MC14051BCL
A10U812	156-0048-00			MICROCKT,LINEAR:5 XSTR ARRAY	02735	CA3046
A10U820	156-1200-01			MICROCKT,LINEAR:OPNL AMPL,QUAD BIFET	80009	156-1200-01
A10U821	156-0513-03			MICROCKT,LINEAR:CMOS,8 CHAN ANALOG MUX	04713	MC14051BCL
A10U830	156-0513-03			MICROCKT,LINEAR:CMOS,8 CHAN ANALOG MUX	04713	MC14051BCL

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A10U831	156-0513-03			MICROCKT,LINEAR:CMOS,8 CHAN ANALOG MUX	04713	MC14051BCL
A10U840	156-1200-01			MICROCKT,LINEAR:OPNL AMPL,QUAD BIFET	80009	156-1200-01
A10U841	156-1200-01			MICROCKT,LINEAR:OPNL AMPL,QUAD BIFET	80009	156-1200-01
A10U850	156-0651-02			MICROCKT,DGTL:8-BIT PRL-OUT SER SHF RGTR	01295	SN74LS164NP3
A10U851	156-0651-02			MICROCKT,DGTL:8-BIT PRL-OUT SER SHF RGTR	01295	SN74LS164NP3
A10U860	156-1589-00			MICROCKT,LINEAR:D/A CNVRTR,12 BIT,HI SPD	06665	DAC312FR
A10U861	156-1200-01			MICROCKT,LINEAR:OPNL AMPL,QUAD BIFET	80009	156-1200-01
A10U870	156-1272-00			MICROCKT,LINEAR:DUAL OPERATIONAL AMPLIFIER	80009	156-1272-00
A10U880	156-1272-00			MICROCKT,LINEAR:DUAL OPERATIONAL AMPLIFIER	80009	156-1272-00
A10U890	156-0158-00			MICROCKT,LINEAR:DUAL OPNL AMPL	04713	MC1458P1/MC1458U
A10VR200	152-0166-00			SEMICOND DVC,DI:ZEN,SI,6.2V,5%,400MW,DO-7	04713	SZ11738RL
A10VR298	152-0278-00			SEMICOND DVC,DI:ZEN,SI,3V,5%,0.4W,DO-7	80009	152-0278-00
A10VR390	152-0662-00			SEMICOND DVC,DI:ZEN,SI,5V,1%,400MW,DO-7	04713	SZG195RL
A10VR391	152-0662-00			SEMICOND DVC,DI:ZEN,SI,5V,1%,400MW,DO-7	04713	SZG195RL
A10VR420	152-0166-00			SEMICOND DVC,DI:ZEN,SI,6.2V,5%,400MW,DO-7	04713	SZ11738RL
A10VR492	152-0662-00			SEMICOND DVC,DI:ZEN,SI,5V,1%,400MW,DO-7	04713	SZG195RL
A10VR493	152-0662-00			SEMICOND DVC,DI:ZEN,SI,5V,1%,400MW,DO-7	04713	SZG195RL
A10W110	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A10W221	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A10W370	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A10W421	131-0566-00	B014162		BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A10W511	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A10W675	131-0566-00	B010100	B010321	BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A10W681	131-0566-00	B010100	B010321	BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A10W772	131-0566-00	B010100	B010321	BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A10W784	131-0566-00	B010100	B010321	BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A10W1001	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A11	670-8164-00	B010100	B010699	CIRCUIT BD ASSY:TIME BASE	80009	670-8164-00
A11	670-8164-01	B010700	B011145	CIRCUIT BD ASSY:TIME BASE	80009	670-8164-01
A11	670-8164-02	B011146	B014160	CIRCUIT BD ASSY:TIME BASE DISPLAY	80009	670-8164-02
A11	670-8164-03	B014161		CIRCUIT BD ASSY:TIME BASE (2430 ONLY)	80009	670-8164-03
A11	670-8164-03	B010100	B010106	CIRCUIT BD ASSY:TIME BASE	80009	670-8164-03
A11	670-8164-04	B010107		CIRCUIT BD ASSY:TIME BASE (2430M ONLY)	80009	670-8164-04
A11C130	290-0967-00			CAP,FXD,ELCTLT:22UF,+50-10%,25V	55680	TLB1E220TAAANA
A11C131	290-0967-00			CAP,FXD,ELCTLT:22UF,+50-10%,25V	55680	TLB1E220TAAANA
A11C150	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C152	281-0786-00			CAP,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA
A11C154	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C166	281-0786-00			CAP,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA
A11C180	285-1344-00			CAP,FXD,PLASTIC:1000PF,100V,5%	TK1573	FKP2 1000 5% 100
A11C181	290-0808-00			CAP,FXD,ELCTLT:2.7UF,10%,20V	05397	T322B275K020AS
A11C182	290-0808-00			CAP,FXD,ELCTLT:2.7UF,10%,20V	05397	T322B275K020AS
A11C199	281-0763-00			CAP,FXD,CER DI:47PF,10%,100V	04222	MA101A470KAA
A11C213	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C223	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C231	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C240	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C243	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C250	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C260	285-1342-00			CAP,FXD,PLASTIC:220PF,100V,5%	TK1573	FKP2 220 5% 100V
A11C261	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C264	285-1342-00			CAP,FXD,PLASTIC:220PF,100V,5%	TK1573	FKP2 220 5% 100V
A11C270	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C281	281-0762-00			CAP,FXD,CER DI:27PF,20%,100V	04222	MA101A270MAA
A11C282	290-0808-00			CAP,FXD,ELCTLT:2.7UF,10%,20V	05397	T322B275K020AS
A11C284	290-0808-00			CAP,FXD,ELCTLT:2.7UF,10%,20V	05397	T322B275K020AS
A11C290	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C291	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C292	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C312	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C313	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C323	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C324	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C331	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C340	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C341	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C342	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C350	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C360	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C365	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C380	281-0810-00			CAP,FXD,CER DI:5.6PF,+/-0.5PF,100V	04222	MA101A5R6DAA
A11C390	283-0594-00			CAP,FXD,MICA DI:0.001UF,1%,100V	00853	D151F102F0
A11C392	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C400	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C401	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C402	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C414	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C415	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C416	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C420	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C422	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C450	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C460	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T

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A11C490	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C500	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C510	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C511	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C513	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C520	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C521	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C522	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C523	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C531	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C532	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C540	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C541	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C550	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C551	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C555	281-0809-00	B010100	B010259	CAP,FXD,CER DI:200 PF,5%,100V	04222	MA101A201JAA
A11C555	281-0909-00	B011146		CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C560	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C570	290-0135-00	B010100	B011145	CAP,FXD,ELCTLT:15UF,20%,20V	05397	T110B156M020AS
A11C570	290-1045-00	B011146		CAP,FXD,ELCTLT:4.7UF,10%,35V	56289	173D475X9035W
A11C571	290-0135-00	B010100	B011145	CAP,FXD,ELCTLT:15UF,20%,20V	05397	T110B156M020AS
A11C572	281-0763-00	B010100	B010259	CAP,FXD,CER DI:47PF,10%,100V	04222	MA101A470KAA
A11C595	281-0810-00			CAP,FXD,CER DI:5.6PF,+/-0.5PF,100V	04222	MA101A5R6DAA
A11C601	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C610	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C611	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C612	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C613	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C620	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C621	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C622	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C623	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C630	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C631	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C632	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C640	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C642	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C643	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C680	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C691	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C692	290-0135-00	B010100	B011145	CAP,FXD,ELCTLT:15UF,20%,20V	05397	T110B156M020AS
A11C692	290-1045-00	B011146		CAP,FXD,ELCTLT:4.7UF,10%,35V	56289	173D475X9035W
A11C694	290-0135-00	B010100	B011145	CAP,FXD,ELCTLT:15UF,20%,20V	05397	T110B156M020AS
A11C694	290-1045-00	B011146		CAP,FXD,ELCTLT:4.7UF,10%,35V	56289	173D475X9035W
A11C695	281-0909-00	B010100	B010259	CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C700	290-0967-00			CAP,FXD,ELCTLT:22UF,+50-10%,25V	55680	TLB1E220TAAANA
A11C701	290-0967-00			CAP,FXD,ELCTLT:22UF,+50-10%,25V	55680	TLB1E220TAAANA
A11C702	290-0967-00			CAP,FXD,ELCTLT:22UF,+50-10%,25V	55680	TLB1E220TAAANA
A11C703	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C711	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C712	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C720	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C730	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C731	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C732	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C740	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C770	281-0786-00	B011146		CAP,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA
A11C772	281-0909-00	B011146		CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T

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A11C774	285-1300-01	B011146		CAP,FXD,MTLZD:0.1UF,10%,63V	55112	185/0.1/K/63/ABA
A11C776	285-1300-01	B011146		CAP,FXD,MTLZD:0.1UF,10%,63V	55112	185/0.1/K/63/ABA
A11C820	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C832	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C890	281-0909-00	B011146		CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C891	281-0791-00	B011146		CAP,FXD,CER DI:270PF,10%,100V	04222	MA101C271KAA
A11C892	281-0791-00	B011146		CAP,FXD,CER DI:270PF,10%,100V	04222	MA101C271KAA
A11C900	281-0770-00			CAP,FXD,CER DI:1000PF,20%,100V	04222	MA101C102MAA
A11C901	281-0762-00			CAP,FXD,CER DI:27PF,20%,100V	04222	MA101A270MAA
A11C903	281-0791-00			CAP,FXD,CER DI:270PF,10%,100V	04222	MA101C271KAA
A11C907	281-0791-00			CAP,FXD,CER DI:270PF,10%,100V	04222	MA101C271KAA
A11C912	285-1343-00			CAP,FXD,PLASTIC:330PF,100V,5%	TK1573	FKP2 330 5% 100V
A11C915	281-0872-00	B010100	B010699	CAP,FXD,CER DI:91PF,5%,100V	04222	MC101A910J
A11C915	281-0797-00	B010700		CAP,FXD,CER DI:15PF,10%,100V	04222	SA106A150KAA
A11C920	281-0823-00			CAP,FXD,CER DI:470PF,10%,50V	04222	MA105A471KAA
A11C925	281-0786-00			CAP,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA
A11C930	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C932	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C934	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11C935	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A11CR190	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A11CR191	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A11CR193	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A11CR194	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A11CR280	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A11CR281	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A11CR283	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A11CR284	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A11J100	131-3182-00			CONN,RCPT,ELEC:HDR,RTANG,2 X 25,0.1 CENTER	22526	75867-008
A11J117	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY OF 4)	22526	48283-029
A11J121	131-3181-00			CONN,RCPT,ELEC:HEADER,RTANG,2 X 20,0.1 CTR	22526	75867-007
A11J131	131-3182-00			CONN,RCPT,ELEC:HDR,RTANG,2 X 25,0.1 CENTER	22526	75867-008
A11J132	131-0608-00	B010100	B010699	TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 3)	22526	48283-036
A11J132	131-0608-00	B010700		TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 2)	22526	48283-036
A11J148	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY OF 4)	22526	48283-029
A11L692	108-0538-00			COIL,RF:FIXED,2.7UH	76493	JWM#B7059
A11L694	108-0538-00			COIL,RF:FIXED,2.7UH	76493	JWM#B7059
A11L770	108-0538-00	B011146		COIL,RF:FIXED,2.7UH	76493	JWM#B7059
A11L780	108-0538-00	B011146		COIL,RF:FIXED,2.7UH	76493	JWM#B7059
A11L800	108-0538-00			COIL,RF:FIXED,2.7UH	76493	JWM#B7059
A11L801	108-0538-00			COIL,RF:FIXED,2.7UH	76493	JWM#B7059
A11L802	108-0538-00			COIL,RF:FIXED,2.7UH	76493	JWM#B7059
A11L803	108-0538-00			COIL,RF:FIXED,2.7UH	76493	JWM#B7059
A11Q181	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A11Q182	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A11Q285	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A11Q286	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A11R132	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A11R133	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A11R140	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A11R141	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A11R145	321-0126-00			RES,FXD,FILM:200 OHM,1%,0.125W,TC=T0	19701	5033ED200R0F
A11R151	321-0816-00			RES,FXD,FILM:5K OHM,1%,0.125W,TC=T0	24546	NA55D5001F
A11R152	321-0816-00			RES,FXD,FILM:5K OHM,1%,0.125W,TC=T0	24546	NA55D5001F

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A11R153	315-0271-00			RES,FXD,FILM:270 OHM,5%,0.25W	57668	NTR25J-E270E
A11R155	321-0816-00			RES,FXD,FILM:5K OHM,1%,0.125W,TC=T0	24546	NA55D5001F
A11R156	321-0816-00			RES,FXD,FILM:5K OHM,1%,0.125W,TC=T0	24546	NA55D5001F
A11R160	321-0816-00			RES,FXD,FILM:5K OHM,1%,0.125W,TC=T0	24546	NA55D5001F
A11R161	321-0816-00			RES,FXD,FILM:5K OHM,1%,0.125W,TC=T0	24546	NA55D5001F
A11R162	321-0222-00			RES,FXD,FILM:2.00K OHM,1%,0.125W,TC=T0	19701	5033ED2K00F
A11R163	321-0193-00			RES,FXD,FILM:1K OHM,1%,0.125W,TC=T0	19701	5033ED1K00F
A11R164	321-0193-00			RES,FXD,FILM:1K OHM,1%,0.125W,TC=T0	19701	5033ED1K00F
A11R165	321-0210-00			RES,FXD,FILM:1.50K OHM,1%,0.125W,TC=T0	19701	5033ED1K50F
A11R171	321-0193-00			RES,FXD,FILM:1K OHM,1%,0.125W,TC=T0	19701	5033ED1K00F
A11R172	321-0816-00			RES,FXD,FILM:5K OHM,1%,0.125W,TC=T0	24546	NA55D5001F
A11R192	321-0165-00			RES,FXD,FILM:511 OHM,1%,0.125W,TC=T0	07716	CEAD511R0F
A11R193	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A11R194	321-0001-00			RES,FXD,FILM:10 OHM,1%,0.125W,TC=T0	19701	5033RD10R00FMS
A11R196	321-0001-00			RES,FXD,FILM:10 OHM,1%,0.125W,TC=T0	19701	5033RD10R00FMS
A11R199	321-0093-00			RES,FXD,FILM:90.9 OHM,1%,0.125W,TC=T0	19701	5043ED90R90F
A11R223	315-0560-00			RES,FXD,FILM:56 OHM,5%,0.25W	57668	NTR25J-E56E0
A11R230	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A11R232	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A11R262	315-0271-00			RES,FXD,FILM:270 OHM,5%,0.25W	57668	NTR25J-E270E
A11R272	321-0097-00			RES,FXD,FILM:100 OHM,1%,0.125W,TC=T0	91637	CMF55116G100R0F
A11R273	321-0126-00			RES,FXD,FILM:200 OHM,1%,0.125W,TC=T0	19701	5033ED200R0F
A11R274	321-0097-00			RES,FXD,FILM:100 OHM,1%,0.125W,TC=T0	91637	CMF55116G100R0F
A11R276	311-2234-00			RES,VAR,NONWW:TRMR,5K OHM,20%,0.5W LINEAR	TK1450	GF06UT 5K
A11R280	321-0816-00			RES,FXD,FILM:5K OHM,1%,0.125W,TC=T0	24546	NA55D5001F
A11R282	321-0244-00			RES,FXD,FILM:3.40K OHM,1%,0.125W,TC=T0	19701	5043ED3K400F
A11R288	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A11R312	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A11R330	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A11R361	321-0165-00			RES,FXD,FILM:511 OHM,1%,0.125W,TC=T0	07716	CEAD511R0F
A11R362	321-0193-00			RES,FXD,FILM:1K OHM,1%,0.125W,TC=T0	19701	5033ED1K00F
A11R363	321-0193-00			RES,FXD,FILM:1K OHM,1%,0.125W,TC=T0	19701	5033ED1K00F
A11R364	321-0816-00			RES,FXD,FILM:5K OHM,1%,0.125W,TC=T0	24546	NA55D5001F
A11R366	321-0816-00			RES,FXD,FILM:5K OHM,1%,0.125W,TC=T0	24546	NA55D5001F
A11R376	311-2234-00			RES,VAR,NONWW:TRMR,5K OHM,20%,0.5W LINEAR	TK1450	GF06UT 5K
A11R380	321-0001-00			RES,FXD,FILM:10 OHM,1%,0.125W,TC=T0	19701	5033RD10R00FMS
A11R381	321-0001-00			RES,FXD,FILM:10 OHM,1%,0.125W,TC=T0	19701	5033RD10R00FMS
A11R382	321-0926-07			RES,FXD,FILM:4K OHM,0.1%,0.125W,TC=T9	19701	5033RE4K00B
A11R383	321-0816-00			RES,FXD,FILM:5K OHM,1%,0.125W,TC=T0	24546	NA55D5001F
A11R384	321-0816-00			RES,FXD,FILM:5K OHM,1%,0.125W,TC=T0	24546	NA55D5001F
A11R385	321-0278-00	B010100	B010699	RES,FXD,FILM:7.68K OHM,1%,0.125W,TC=T0	07716	CEAD76800F
A11R385	321-0276-00	B010700		RES,FXD,FILM:7.32K OHM,1%,0.125W,TC=T0	19701	5043ED7K320F
A11R400	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A11R421	307-0446-00			RES NTWK,FXD,FI:10K OHM,20%,(9)RES	11236	750-101-R10K
A11R441	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A11R450	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A11R470	321-0230-00			RES,FXD,FILM:2.43K OHM,1%,0.125W,TC=T0	19701	5043ED2K430F
A11R471	321-0273-00			RES,FXD,FILM:6.81K OHM,1%,0.125W,TC=T0	07716	CEAD68100F
A11R472	321-0300-00			RES,FXD,FILM:13.0K OHM,1%,0.125W,TC=T0	07716	CEAD13001F
A11R473	321-0377-00			RES,FXD,FILM:82.5K OHM,1%,0.125W,TC=T0	07716	CEAD82501F
A11R474	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A11R475	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A11R480	321-0243-00			RES,FXD,FILM:3.32K OHM,1%,0.125W,TC=T0	19701	5033ED3K32F
A11R481	321-0251-00			RES,FXD,FILM:4.02K OHM,1%,0.125W,TC=T0	19701	5033ED4K020F
A11R482	321-0275-00			RES,FXD,FILM:7.15K OHM,1%,0.125W,TC=T0	07716	CEAD71500F
A11R483	321-0272-00			RES,FXD,FILM:6.65K OHM,1%,0.125W,TC=T0	19701	5043ED6K650F
A11R484	321-0355-00	B010100	B010699	RES,FXD,FILM:48.7K OHM,1%,0.125W,TC=T0	07716	CEAD48701F
A11R484	321-0326-00	B010700		RES,FXD,FILM:24.3K OHM,1%,0.125W,TC=T0	19701	5043ED24K30F

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A11R485	321-0300-00			RES,FXD,FILM:13.0K OHM,1%,0.125W,TC=T0	07716	CEAD13001F
A11R490	321-0222-00			RES,FXD,FILM:2.00K OHM,1%,0.125W,TC=T0	19701	5033ED2K00F
A11R492	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A11R493	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A11R494	321-0414-00			RES,FXD,FILM:200K OHM,1%,0.125W,TC=T0	07716	CEAD20002F
A11R501	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A11R522	315-0560-00			RES,FXD,FILM:56 OHM,5%,0.25W	57668	NTR25J-E56E0
A11R530	315-0560-00			RES,FXD,FILM:56 OHM,5%,0.25W	57668	NTR25J-E56E0
A11R542	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A11R555	315-0750-00	B010100	B010259	RES,FXD,FILM:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A11R555	315-0560-00	B011146		RES,FXD,FILM:56 OHM,5%,0.25W	57668	NTR25J-E56E0
A11R570	321-0356-00			RES,FXD,FILM:49.9K OHM,1%,0.125W,TC=T0	19701	5033ED49K90F
A11R580	311-2234-00			RES,VAR,NONWW:TRMR,5K OHM,20%,0.5W LINEAR	TK1450	GF06UT 5K
A11R581	321-0097-00	B010100	B011145	RES,FXD,FILM:100 OHM,1%,0.125W,TC=T0	91637	CMF55116G100R0F
A11R581	321-0193-00	B011146		RES,FXD,FILM:1K OHM,1%,0.125W,TC=T0	19701	5033ED1K00F
A11R583	311-2236-00			RES,VAR,NONWW:TRMR,20K OHM,20%,0.5W LINEAR	TK1450	GF06UT 20K
A11R584	311-2236-00			RES,VAR,NONWW:TRMR,20K OHM,20%,0.5W LINEAR	TK1450	GF06UT 20K
A11R585	311-2236-00			RES,VAR,NONWW:TRMR,20K OHM,20%,0.5W LINEAR	TK1450	GF06UT 20K
A11R586	311-2234-00			RES,VAR,NONWW:TRMR,5K OHM,20%,0.5W LINEAR	TK1450	GF06UT 5K
A11R587	311-2236-00			RES,VAR,NONWW:TRMR,20K OHM,20%,0.5W LINEAR	TK1450	GF06UT 20K
A11R591	321-0816-00			RES,FXD,FILM:5K OHM,1%,0.125W,TC=T0	24546	NA55D5001F
A11R592	321-0816-00			RES,FXD,FILM:5K OHM,1%,0.125W,TC=T0	24546	NA55D5001F
A11R593	315-0202-02			RES,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A11R594	315-0202-02			RES,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A11R595	315-0202-02			RES,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A11R596	315-0202-02			RES,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A11R601	321-0118-00			RES,FXD,FILM:165 OHM,1%,0.125W,TC=T0	07716	CEAD165R0F
A11R603	321-0129-00			RES,FXD,FILM:215 OHM,1%,0.125W,TC=T0	07716	CEAD215R0F
A11R605	321-0097-00			RES,FXD,FILM:100 OHM,1%,0.125W,TC=T0	91637	CMF55116G100R0F
A11R607	321-0193-00			RES,FXD,FILM:1K OHM,1%,0.125W,TC=T0	19701	5033ED1K00F
A11R609	311-2231-00	B010100	B010699	RES,VAR,NONWW:TRMR,1K OHM,20%,0.5W LINEAR	TK1450	GF06UT 1K
A11R610	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A11R612	315-0750-00	B010260		RES,FXD,FILM:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A11R620	311-2231-00			RES,VAR,NONWW:TRMR,1K OHM,20%,0.5W LINEAR	TK1450	GF06UT 1K
A11R650	307-0446-00			RES NTWK,FXD,FI:10K OHM,20%,(9)RES	11236	750-101-R10K
A11R690	315-0101-00	B010100	B011145	RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A11R690	321-0097-00	B011146		RES,FXD,FILM:100 OHM,1%,0.125W,TC=T0	91637	CMF55116G100R0F
A11R713	315-0560-00			RES,FXD,FILM:56 OHM,5%,0.25W	57668	NTR25J-E56E0
A11R715	315-0560-00			RES,FXD,FILM:56 OHM,5%,0.25W	57668	NTR25J-E56E0
A11R716	315-0560-00			RES,FXD,FILM:56 OHM,5%,0.25W	57668	NTR25J-E56E0
A11R720	307-0446-00			RES NTWK,FXD,FI:10K OHM,20%,(9)RES	11236	750-101-R10K
A11R721	307-0446-00			RES NTWK,FXD,FI:10K OHM,20%,(9)RES	11236	750-101-R10K
A11R722	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A11R723	315-0560-00			RES,FXD,FILM:56 OHM,5%,0.25W	57668	NTR25J-E56E0
A11R732	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A11R780	321-0118-00	B011146		RES,FXD,FILM:165 OHM,1%,0.125W,TC=T0	07716	CEAD165R0F
A11R781	321-0143-00	B011146		RES,FXD,FILM:301 OHM,1%,0.125W,TC=T0	07716	CEAD301R0F
A11R831	315-0560-00			RES,FXD,FILM:56 OHM,5%,0.25W	57668	NTR25J-E56E0
A11R832	315-0560-00			RES,FXD,FILM:56 OHM,5%,0.25W	57668	NTR25J-E56E0
A11R833	315-0560-00			RES,FXD,FILM:56 OHM,5%,0.25W	57668	NTR25J-E56E0
A11R840	315-0560-00			RES,FXD,FILM:56 OHM,5%,0.25W	57668	NTR25J-E56E0
A11R841	315-0560-00			RES,FXD,FILM:56 OHM,5%,0.25W	57668	NTR25J-E56E0
A11R842	315-0560-00			RES,FXD,FILM:56 OHM,5%,0.25W	57668	NTR25J-E56E0
A11R843	315-0560-00			RES,FXD,FILM:56 OHM,5%,0.25W	57668	NTR25J-E56E0
A11R844	315-0560-00			RES,FXD,FILM:56 OHM,5%,0.25W	57668	NTR25J-E56E0
A11R845	315-0560-00			RES,FXD,FILM:56 OHM,5%,0.25W	57668	NTR25J-E56E0
A11R880	321-0068-00	B011146		RES,FXD,FILM:49.9 OHM,0.5%,0.125W,TC=T0	91637	CMF55116G49R90F
A11R881	321-0143-00	B011146		RES,FXD,FILM:301 OHM,1%,0.125W,TC=T0	07716	CEAD301R0F

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A11R884	321-0239-00	B011146		RES,FXD,FILM:3.01K OHM,1%,0.125W,TC=TO	19701	5043ED3K010F
A11R890	315-0560-00	B011146		RES,FXD,FILM:56 OHM,5%,0.25W	57668	NTR25J-E56E0
A11R891	315-0101-00	B011146		RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A11TP130	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A11TP133	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A11TP200	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A11TP250	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A11TP341	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A11TP400	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A11TP490	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A11TP530	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A11TP600	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A11TP601	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A11TP602	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A11TP680	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A11TP700	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A11TP710	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A11TP840	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A11U130	156-0852-02			MICROCKT,DGTL:LSTTL,HEX BUS DRIVER	01295	SN74LS367NP3
A11U140	156-0956-02			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT,SCRN	01295	SN74LS244NP3
A11U141	156-0956-02			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT,SCRN	01295	SN74LS244NP3
A11U142	156-1638-00			MICROCKT,LINEAR:10 BIT HS,MULT,D/A CONV	06665	DAC-10GX
A11U170	156-1149-00			MICROCKT,LINEAR:OPERATIONAL AMP,JFET INPUT	27014	LF351N/GLEA134
A11U210	156-0530-02			MICROCKT,DGTL:QUAD 2-INP MUX,SCRN	01295	SN74LS157NP3
A11U211	156-0422-02			MICROCKT,DGTL:UP/DOWN SYN BINARY CNTR,SCRN	18324	N74LS191NB
A11U212	156-0530-02			MICROCKT,DGTL:QUAD 2-INP MUX,SCRN	01295	SN74LS157NP3
A11U220	156-0422-02			MICROCKT,DGTL:UP/DOWN SYN BINARY CNTR,SCRN	18324	N74LS191NB
A11U221	156-0530-02			MICROCKT,DGTL:QUAD 2-INP MUX,SCRN	01295	SN74LS157NP3
A11U222	156-0422-02			MICROCKT,DGTL:UP/DOWN SYN BINARY CNTR,SCRN	18324	N74LS191NB
A11U223	156-0481-02			MICROCKT,DGTL:TRIPLE 3-INP & GATE,SCRN	01295	SN74LS11NP3
A11U230	156-0994-02			MICROCKT,DGTL:8 INPUT DATA SEL/MUX,SCRN	01295	SN74LS151NP3
A11U231	156-0844-02			MICROCKT,DGTL:SYN 4 BIT CNTR,SCRN	01295	SN74LS161A(NP3)
A11U232	160-2559-00			MICROCKT,DGTL:32 X 8 PROM,PRGM	80009	160-2559-00
A11U240	156-0852-02			MICROCKT,DGTL:LSTTL,HEX BUS DRIVER	01295	SN74LS367NP3
A11U241	156-0982-03			MICROCKT,DGTL:OCTAL-D-EDGE TRIG FF,SCRN	01295	SN74LS374N3
A11U243	156-0956-02			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT,SCRN	01295	SN74LS244NP3
A11U250	156-1638-00			MICROCKT,LINEAR:10 BIT HS,MULT,D/A CONV	06665	DAC-10GX
A11U270	156-0515-02			MICROCKT,DGTL:TRIPLE 3-CHAN MUX,SEL	80009	156-0515-02
A11U280	156-2485-00			MICROCKT,LINEAR:OPNL AMPL,INP,WIDEBAND	80009	156-2485-00
A11U281	156-0742-00			MICROCKT,LINEAR:OPNL AMPL	01295	LM318P
A11U282	156-2485-00			MICROCKT,LINEAR:OPNL AMPL,INP,WIDEBAND	80009	156-2485-00
A11U290	156-0514-02			MICROCKT,DGTL:DIFF 4 CHANNEL MUX,SEL	04713	MC14052BCP
A11U300	156-1714-00			MICROCKT,DGTL:ASTTL,SYN UP/DOWN BIN COUNTER	07263	74F191 (PCQR)
A11U312	156-0386-02			MICROCKT,DGTL:TRIPLE 3-INP NAND GATE,SCRN	07263	74LS10PCQR
A11U313	156-0452-02			MICROCKT,DGTL:4-WIDE,2-INP AOI,SCREENED	04713	SN74LS54 ND/JD
A11U314	156-1111-02			MICROCKT,DGTL:OCTAL BUS XCVR W/3 STATE OUT	01295	SN74LS245N3
A11U320	156-0956-02			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT,SCRN	01295	SN74LS244NP3
A11U321	156-0956-02			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT,SCRN	01295	SN74LS244NP3
A11U322	156-1111-02			MICROCKT,DGTL:OCTAL BUS XCVR W/3 STATE OUT	01295	SN74LS245N3
A11U323	156-0479-02			MICROCKT,DGTL:QUAD 2-INP OR GATE,SCRN	01295	SN74LS32NP3
A11U330	160-2560-00			MICROCKT,DGTL:32 X 8 PROM,PRGM	80009	160-2560-00
A11U340	156-0382-02			MICROCKT,DGTL:QUAD 2 INP NAND GATE BURN	18324	N74LS00NB
A11U350	156-0381-02			MICROCKT,DGTL:QUAD 2-INP EXCL OR GATE	07263	74LS86PCQR
A11U370	156-1200-01			MICROCKT,LINEAR:OPNL AMPL,QUAD BIFET	80009	156-1200-01
A11U392	156-1200-01			MICROCKT,LINEAR:OPNL AMPL,QUAD BIFET	80009	156-1200-01
A11U400	156-1714-00			MICROCKT,DGTL:ASTTL,SYN UP/DOWN BIN COUNTER	07263	74F191 (PCQR)
A11U401	156-1714-00			MICROCKT,DGTL:ASTTL,SYN UP/DOWN BIN COUNTER	07263	74F191 (PCQR)
A11U410	156-0910-02			MICROCKT,DGTL:DUAL DECADE COUNTER,SCRN	01295	SN74LS390N3

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A11U411	156-0386-02			MICROCKT,DGTL:TRIPLE 3-INP NAND GATE,SCRN	07263	74LS10PCQR
A11U412	156-0382-02			MICROCKT,DGTL:QUAD 2 INP NAND GATE BURN	18324	N74LS00NB
A11U413	156-0385-02			MICROCKT,DGTL:HEX INVERTER,SCRN	07263	74LS04PCQR
A11U414	156-0388-03			MICROCKT,DGTL:DUAL D FLIP-FLOP,SCRN	01295	SN74LS74ANP3
A11U415	156-0388-03			MICROCKT,DGTL:DUAL D FLIP-FLOP,SCRN	01295	SN74LS74ANP3
A11U416	156-1172-01			MICROCKT,DGTL:DUAL 4 BIT BIN CNTR,SCRN	01295	SN74LS393NP3
A11U420	160-2558-00			MICROCKT,DGTL:4096 X 8 EPROM,PRGM	80009	160-2558-00
A11U421	156-0480-02			MICROCKT,DGTL:QUAD 2-INP & GATE,SCRN,	01295	SN74LS08NP3
A11U422	156-0479-02			MICROCKT,DGTL:QUAD 2-INP OR GATE,SCRN	01295	SN74LS32NP3
A11U423	156-1373-01			MICROCKT,DGTL:QUAD BUS BFR GATES	27014	DM74LS125 NA+
A11U430	156-1228-00			MICROCKT,DGTL:NMOS,4096 X 1 STATIC RAM	34335	AM2147-70DC
A11U431	156-2016-00			MICROCKT,DGTL:NMOS,2048 X 8 SRAM	TK1016	TMM2016AP-10
A11U440	156-2016-00			MICROCKT,DGTL:NMOS,2048 X 8 SRAM	TK1016	TMM2016AP-10
A11U441	156-0982-03			MICROCKT,DGTL:OCTAL-D-EDGE TRIG FF,SCRN	01295	SN74LS374N3
A11U442	156-0382-02			MICROCKT,DGTL:QUAD 2 INP NAND GATE BURN	18324	N74LS00NB
A11U450	156-0480-02			MICROCKT,DGTL:QUAD 2-INP & GATE,SCRN,	01295	SN74LS08NP3
A11U460	156-1200-01			MICROCKT,LINEAR:OPNL AMPL,QUAD BIFET	80009	156-1200-01
A11U500	156-0382-02			MICROCKT,DGTL:QUAD 2 INP NAND GATE BURN	18324	N74LS00NB
A11U501	156-0530-02			MICROCKT,DGTL:QUAD 2-INP MUX,SCRN	01295	SN74LS157NP3
A11U502	156-0982-03			MICROCKT,DGTL:OCTAL-D-EDGE TRIG FF,SCRN	01295	SN74LS374N3
A11U510	156-0388-03			MICROCKT,DGTL:DUAL D FLIP-FLOP,SCRN	01295	SN74LS74ANP3
A11U511	156-0388-03			MICROCKT,DGTL:DUAL D FLIP-FLOP,SCRN	01295	SN74LS74ANP3
A11U512	156-0479-02			MICROCKT,DGTL:QUAD 2-INP OR GATE,SCRN	01295	SN74LS32NP3
A11U513	156-1722-00			MICROCKT,DGTL:HEX INVERTER	04713	MC74F04ND
A11U520	156-1611-00			MICROCKT,DGTL:ASTTL,DUAL D TYPE EDGE-TRIG	80009	156-1611-00
A11U521	156-1611-00			MICROCKT,DGTL:ASTTL,DUAL D TYPE EDGE-TRIG	80009	156-1611-00
A11U522	156-1724-00			MICROCKT,DGTL:QUAD 2 INPUT OR GATE	04713	MC74F32ND
A11U523	156-0118-03			MICROCKT,DGTL:1 DUAL J-K FF,BURN-IN	01295	SN74S112JP4
A11U530	156-0913-02			MICROCKT,DGTL:OCTAL D FF W/ENABLE,SCRN	01295	SN74LS377NP3
A11U531	156-1277-00			MICROCKT,DGTL:LSTTL,3-STATE OCTAL BFR,SCRN	27014	DM81LS95ANA+
A11U532	156-1277-00			MICROCKT,DGTL:LSTTL,3-STATE OCTAL BFR,SCRN	27014	DM81LS95ANA+
A11U540	156-0913-02			MICROCKT,DGTL:OCTAL D FF W/ENABLE,SCRN	01295	SN74LS377NP3
A11U541	156-0865-02			MICROCKT,DGTL:OCTAL D FF W/CLEAR,SCRN	01295	SN74LS273NP3
A11U542	156-1277-00			MICROCKT,DGTL:LSTTL,3-STATE OCTAL BFR,SCRN	27014	DM81LS95ANA+
A11U550	156-0469-02			MICROCKT,DGTL:3/8 LINE DCDR,SCRN	01295	SN74LS138NP3
A11U560	156-1590-00	B010100	B011145	MICROCKT,LINEAR:A/D CONV,400NS,8-BIT	01281	TDS5427/1001J8C
A11U560	156-2800-00	B011146		MICROCKT,INTFC:BIPOLAR,A/D CONV,8 BIT FLASH	80009	156-2800-00
A11U600	156-2016-00			MICROCKT,DGTL:NMOS,2048 X 8 SRAM	TK1016	TMM2016AP-10
A11U601	156-0982-03			MICROCKT,DGTL:OCTAL-D-EDGE TRIG FF,SCRN	01295	SN74LS374N3
A11U610	156-1111-02			MICROCKT,DGTL:OCTAL BUS XCVR W/3 STATE OUT	01295	SN74LS245N3
A11U612	156-0118-03			MICROCKT,DGTL:1 DUAL J-K FF,BURN-IN	01295	SN74S112JP4
A11U613	156-0956-02			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT,SCRN	01295	SN74LS244NP3
A11U615	156-0118-03			MICROCKT,DGTL:1 DUAL J-K FF,BURN-IN	01295	SN74S112JP4
A11U620	156-1707-00			MICROCKT,DGTL:QUAD 2-INPUT NAND GATE,SCRN	04713	MC7400(NDORJD)
A11U621	156-1935-00			MICROCKT,DGTL:SYNC PRESETTABLE BINARY CNTR	04713	MC74F163ND/JD
A11U622	156-1935-00			MICROCKT,DGTL:SYNC PRESETTABLE BINARY CNTR	04713	MC74F163ND/JD
A11U623	156-1663-00			MICROCKT,DGTL:ASTTL,TPL 3-INP & GATE	04713	MC74F11ND/JD
A11U630	156-0982-03			MICROCKT,DGTL:OCTAL-D-EDGE TRIG FF,SCRN	01295	SN74LS374N3
A11U631	156-0982-03			MICROCKT,DGTL:OCTAL-D-EDGE TRIG FF,SCRN	01295	SN74LS374N3
A11U632	156-0982-03			MICROCKT,DGTL:OCTAL-D-EDGE TRIG FF,SCRN	01295	SN74LS374N3
A11U640	156-0982-03			MICROCKT,DGTL:OCTAL-D-EDGE TRIG FF,SCRN	01295	SN74LS374N3
A11U641	156-1111-02			MICROCKT,DGTL:OCTAL BUS XCVR W/3 STATE OUT	01295	SN74LS245N3
A11U642	156-1961-00			MICROCKT,DGTL:BIDIRECTIONAL UNIV SHF RGTR	07263	74F194P
A11U650	156-0386-02			MICROCKT,DGTL:TRIPLE 3-INP NAND GATE,SCRN	07263	74LS10PCQR
A11U651	156-0388-03			MICROCKT,DGTL:DUAL D FLIP-FLOP,SCRN	01295	SN74LS74ANP3
A11U670	156-2381-00			MICROCKT,DGTL:STD CELL TIME BASE DSPLY	80009	156-2381-00
A11U680	156-0956-02			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT,SCRN	01295	SN74LS244NP3
A11U710	156-1973-00			MICROCKT,DGTL:STTL,QUAD D FF	07263	74F175PCQR

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A11U711	156-1800-00			MICROCKT,DGTL:ASTTL,QUAD 2 INP EXCL OR GATE	18324	N74F86(NB OR JB)
A11U712	156-1723-00			MICROCKT,DGTL:QUAD 2 INPUT & GATE	04713	MC74F08 ND OR JD
A11U720	156-1611-00			MICROCKT,DGTL:ASTTL,DUAL D TYPE EDGE-TRIG	80009	156-1611-00
A11U721	156-1935-00			MICROCKT,DGTL:SYNC PRESETTABLE BINARY CNTR	04713	MC74F163ND/JD
A11U722	156-1662-00			MICROCKT,DGTL:ASTTL,DUAL 4 INP MUX	04713	MC74F153 ND/JD
A11U730	156-1961-00			MICROCKT,DGTL:BIDIRECTIONAL UNIV SHF RGTR	07263	74F194P
A11U731	156-1723-00			MICROCKT,DGTL:QUAD 2 INPUT & GATE	04713	MC74F08 ND OR JD
A11U732	156-0953-02			MICROCKT,DGTL:4 BIT MAGNITUDE CMPRTR,SCRN	01295	SN74LS85NP3
A11U740	156-0953-02			MICROCKT,DGTL:4 BIT MAGNITUDE CMPRTR,SCRN	01295	SN74LS85NP3
A11U780	156-2804-00	B011146		MICROCKT,LI:OP AMP,WIDEBAND,HI SLEW RATE	80009	156-2804-00
A11U830	156-1961-00			MICROCKT,DGTL:BIDIRECTIONAL UNIV SHF RGTR	07263	74F194P
A11U831	156-1961-00			MICROCKT,DGTL:BIDIRECTIONAL UNIV SHF RGTR	07263	74F194P
A11U832	156-1722-00			MICROCKT,DGTL:HEX INVERTER	04713	MC74F04ND
A11U880	156-1149-01	B011146		MICROCKT,LINEAR:OPERATION AMP JFET INPUT	27014	AL160307
A11W140	175-9026-00			CA ASSY,SP,ELEC:50,28 AWG,6.5 L	80009	175-9026-00
A11W609	131-0566-00	B010700		BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A11Y611	119-1460-00	B010100	B013588	OSCILLATOR,RF:40.0MHZ	01537	K1100AM 40 MHz
A11Y611	119-2430-00	B013589		OSCILLATOR,RF:XSTL CONT,40MHZ,0.001% (2430 ONLY)	01537	K1144 AM-40MHZ
A11Y611	119-1460-00	B010100	B010130	OSCILLATOR,RF:40.0MHZ	01537	K1100AM 40 MHz
A11Y611	119-2430-00	B010131		OSCILLATOR,RF:XSTL CONT,40MHZ,0.001% (2430M ONLY)	01537	K1144 AM-40MHZ

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A12	670-8165-00	B010100	B012056	CIRCUIT BD ASSY:PROCESSOR	80009	670-8165-00
A12	670-8165-05	B012057	B014012	CIRCUIT BD ASSY:PROCESSOR	80009	670-8165-05
A12	670-8165-07	B014013		CIRCUIT BD ASSY:PROCESSOR (STANDARD ONLY) (DOES NOT INCLUDE FIRMWARE)	80009	670-8165-07
A12	670-8165-01	B010100	B012303	CIRCUIT BD ASSY:PROCESSOR OPT 05	80009	670-8165-01
A12	670-8165-06	B012304	B014012	CIRCUIT BD ASSY:PROCESSOR OPT 05	80009	670-8165-06
A12	670-8165-08	B014013		CIRCUIT BD ASSY:PROCESSOR OPT 05 (OPTION 05 ONLY)(DOES NOT INCLUDE FIRMWARE)	80009	670-8165-08
A12	670-8165-03	B010100	B010104	CIRCUIT BD ASSY:PROCESSOR,STD,CIIL	80009	670-8165-03
A12	670-8165-05	B010105	B010139	CIRCUIT BD ASSY:PROCESSOR	80009	670-8165-05
A12	670-8165-07	B010140		CIRCUIT BD ASSY:PROCESSOR (2430M ONLY)(DOES NOT INCLUDE FIRMWARE)	80009	670-8165-07
A12BT800	146-0049-00			BATTERY,STORAGE:3.5V,750MAH	81855	LTC-7P
A12C116	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C118	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C120	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C122	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C124	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C150	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C202	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C204	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C206	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C208	285-1238-00			CAP,FXD,PLASTIC:0.22UF,20%,100V	14752	C2598
A12C210	285-1238-00			CAP,FXD,PLASTIC:0.22UF,20%,100V	14752	C2598
A12C217	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V (OPTION 05 ONLY)	04222	MA201C103KAA
A12C218	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V (OPTION 05 ONLY)	04222	MA205E104MAA
A12C238	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C308	281-0785-00			CAP,FXD,CER DI:68PF,10%,100V (OPTION 05 ONLY)	04222	MA101A680KAA
A12C322	290-0183-00			CAP,FXD,ELCTLT:1UF,10%,35V (OPTION 05 ONLY)	05397	T3228105K035AS
A12C324	281-0861-00			CAP,FXD,CER DI:270PF,5%,50V (OPTION 05 ONLY)	54583	MA12C0G1H271J
A12C325	281-0820-00			CAP,FXD,CER DI:680 PF,10%,50V (OPTION 05 ONLY)	04222	SA105C681KAA
A12C328	281-0813-00			CAP,FXD,CER DI:0.047UF,20%,50V (OPTION 05 ONLY)	05397	C412C473M5V2CA
A12C330	281-0812-00			CAP,FXD,CER DI:1000PF,10%,100V (OPTION 05 ONLY)	04222	MA101C102KAA
A12C332	281-0814-00			CAP,FXD,CER DI:100 PF,10%,100V (OPTION 05 ONLY)	04222	MA101A101KAA
A12C336	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C342	281-0757-00			CAP,FXD,CER DI:10PF,20%,100V TUBULAR,MI	04222	MA101A100MAA
A12C344	283-0107-00			CAP,FXD,CER DI:51PF,5%,200V	04222	SR206A510JAA
A12C348	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C354	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C358	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C360	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C370	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C372	283-0051-00			CAP,FXD,CER DI:0.0033UF,5%,100V	04222	SR301A332JAA
A12C374	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C386	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C402	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V (OPTION 05 ONLY)	04222	MA205E104MAA
A12C414	281-0863-00			CAP,FXD,CER DI:240PF,5%,100V (OPTION 05 ONLY)	04222	SA101A241JAA
A12C416	281-0792-00			CAP,FXD,CER DI:82PF,10%,100V (OPTION 05 ONLY)	04222	SA101A820KAA

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A12C418	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V (OPTION 05 ONLY)	04222	MA205E104MAA
A12C424	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V (OPTION 05 ONLY)	04222	MA205E104MAA
A12C426	290-0183-00			CAP,FXD,ELCTLT:1UF,10%,35V (OPTION 05 ONLY)	05397	T322B105K035AS
A12C452	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C462	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C464	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C466	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C472	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C474	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C484	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C510	281-0814-00			CAP,FXD,CER DI:100 PF,10%,100V (OPTION 05 ONLY)	04222	MA101A101KAA
A12C512	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V (OPTION 05 ONLY)	04222	MA205E104MAA
A12C514	281-0786-00			CAP,FXD,CER DI:150PF,10%,100V (OPTION 05 ONLY)	04222	MA101A151KAA
A12C520	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V (OPTION 05 ONLY)	04222	MA201C103KAA
A12C522	281-0826-00			CAP,FXD,CER DI:2200PF,10%,100V (OPTION 05 ONLY)	20932	401EM100AD222K
A12C526	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V (OPTION 05 ONLY)	04222	MA205E104MAA
A12C528	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C532	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C542	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C550	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C572	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C580	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C582	290-0943-00	B010100	B013921	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A12C582	290-0943-02	B013922		CAP,FXD,ELCTLT:47UF,20%,25V (2430 ONLY)	55680	UVX1E470MAA1TD
A12C582	290-0943-00	B010100	B010139	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A12C582	290-0943-02	B010140		CAP,FXD,ELCTLT:47UF,20%,25V (2430M ONLY)	55680	UVX1E470MAA1TD
A12C586	281-0814-00			CAP,FXD,CER DI:100 PF,10%,100V	04222	MA101A101KAA
A12C590	290-0943-00	B010100	B013921	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A12C590	290-0943-02	B013922		CAP,FXD,ELCTLT:47UF,20%,25V (2430 ONLY)	55680	UVX1E470MAA1TD
A12C590	290-0943-00	B010100	B010139	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A12C590	290-0943-02	B010140		CAP,FXD,ELCTLT:47UF,20%,25V (2430M ONLY)	55680	UVX1E470MAA1TD
A12C592	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C606	281-0788-00			CAP,FXD,CER DI:470PF,10%,100V (OPTION 05 ONLY)	04222	SA101C471KAA
A12C608	281-0814-00			CAP,FXD,CER DI:100 PF,10%,100V (OPTION 05 ONLY)	04222	MA101A101KAA
A12C609	281-0786-00			CAP,FXD,CER DI:150PF,10%,100V (OPTION 05 ONLY)	04222	MA101A151KAA
A12C612	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V (OPTION 05 ONLY)	04222	MA205E104MAA
A12C620	290-0188-00			CAP,FXD,ELCTLT:0.1UF,10%,35V (STANDARD ONLY)	05397	T322A104K035AS
A12C620	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V (OPTION 05 ONLY)	04222	MA205E104MAA
A12C622	290-0246-00			CAP,FXD,ELCTLT:3.3UF,10%,15V (OPTION 05 ONLY)	12954	D3R3EA15K1
A12C624	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V (OPTION 05 ONLY)	04222	MA205E104MAA

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A12C626	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C646	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C664	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C670	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C712	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V (OPTION 05 ONLY)	04222	MA205E104MAA
A12C713	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V (OPTION 05 ONLY)	04222	MA205E104MAA
A12C714	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V (OPTION 05 ONLY)	04222	MA205E104MAA
A12C716	290-0808-00			CAP,FXD,ELCTLT:2.7UF,10%,20V (OPTION 05 ONLY)	05397	T322B275K020AS
A12C719	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V (OPTION 05 ONLY)	04222	MA205E104MAA
A12C720	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C748	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C764	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C766	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C774	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C780	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C790	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C850	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C862	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C882	290-0943-00	B010100	B013921	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A12C882	290-0943-02	B013922		CAP,FXD,ELCTLT:47UF,20%,25V (2430 ONLY)	55680	UVX1E470MAA1TD
A12C882	290-0943-00	B010100	B010139	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A12C882	290-0943-02	B010140		CAP,FXD,ELCTLT:47UF,20%,25V (2430M ONLY)	55680	UVX1E470MAA1TD
A12C884	290-0943-00	B010100	B013921	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A12C884	290-0943-02	B013922		CAP,FXD,ELCTLT:47UF,20%,25V (2430 ONLY)	55680	UVX1E470MAA1TD
A12C884	290-0943-00	B010100	B010139	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A12C884	290-0943-02	B010140		CAP,FXD,ELCTLT:47UF,20%,25V (2430M ONLY)	55680	UVX1E470MAA1TD
A12C886	290-0943-00	B010100	B013921	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A12C886	290-0943-02	B013922		CAP,FXD,ELCTLT:47UF,20%,25V (2430 ONLY)	55680	UVX1E470MAA1TD
A12C886	290-0943-00	B010100	B010139	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A12C886	290-0943-02	B010140		CAP,FXD,ELCTLT:47UF,20%,25V (2430M ONLY)	55680	UVX1E470MAA1TD
A12C894	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C896	290-1044-00			CAP,FXD,ELCTLT:1UF,+40-20%,5.5VDC	TK0510	EECW5R5D105
A12C904	290-0943-00	B010100	B013921	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A12C904	290-0943-02	B013922		CAP,FXD,ELCTLT:47UF,20%,25V (2430 ONLY)	55680	UVX1E470MAA1TD
A12C904	290-0943-00	B010100	B010139	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A12C904	290-0943-02	B010140		CAP,FXD,ELCTLT:47UF,20%,25V (2430M ONLY)	55680	UVX1E470MAA1TD
A12C936	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12C938	290-0188-00	B010100	B010399	CAP,FXD,ELCTLT:0.1UF,10%,35V	05397	T322A104K035AS
A12C938	290-0244-00	B010400		CAP,FXD,ELCTLT:0.47UF,5%,35V	56289	173D474X5035U
A12C948	281-0757-00			CAP,FXD,CER DI:10PF,20%,100V TUBULAR,MI	04222	MA101A100MAA
A12C950	283-0107-00			CAP,FXD,CER DI:51PF,5%,200V	04222	SR206A510JAA
A12C964	290-0943-00	B010100	B013921	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A12C964	290-0943-02	B013922		CAP,FXD,ELCTLT:47UF,20%,25V (2430 ONLY)	55680	UVX1E470MAA1TD
A12C964	290-0943-00	B010100	B010139	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A12C964	290-0943-02	B010140		CAP,FXD,ELCTLT:47UF,20%,25V (2430M ONLY)	55680	UVX1E470MAA1TD

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A12C980	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A12CR224	152-0322-00	B010100	B013917	SEMICOND DVC,DI:SCHOTTKY,SI,15V,1.2PF,DO-35	50434	5082-2672
A12CR224	152-0951-00	B013918		SEMICOND DVC DI:SCHOTTKY,SI,60V,2.25PF (OPTION 05 ONLY)	80009	152-0951-00
A12CR244	152-0322-00	B010100	B013917	SEMICOND DVC,DI:SCHOTTKY,SI,15V,1.2PF,DO-35	50434	5082-2672
A12CR244	152-0951-00	B013918		SEMICOND DVC DI:SCHOTTKY,SI,60V,2.25PF	80009	152-0951-00
A12CR300	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A12CR324	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35 (OPTION 05 ONLY)	03508	DA2527 (1N4152)
A12CR325	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35 (OPTION 05 ONLY)	03508	DA2527 (1N4152)
A12CR326	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35 (OPTION 05 ONLY)	03508	DA2527 (1N4152)
A12CR328	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35 (OPTION 05 ONLY)	03508	DA2527 (1N4152)
A12CR329	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35 (OPTION 05 ONLY)	03508	DA2527 (1N4152)
A12CR332	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35 (OPTION 05 ONLY)	03508	DA2527 (1N4152)
A12CR334	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35 (OPTION 05 ONLY)	03508	DA2527 (1N4152)
A12CR336	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35 (OPTION 05 ONLY)	03508	DA2527 (1N4152)
A12CR400	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A12CR422	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35 (OPTION 05 ONLY)	03508	DA2527 (1N4152)
A12CR502	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35 (OPTION 05 ONLY)	03508	DA2527 (1N4152)
A12CR510	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35 (OPTION 05 ONLY)	03508	DA2527 (1N4152)
A12CR512	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35 (OPTION 05 ONLY)	03508	DA2527 (1N4152)
A12CR526	152-0460-00			SEMICOND DVC,DI:FE,SI,25V,1MA,TO-7 (OPTION 05 ONLY)	04713	SCL072
A12CR594	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A12CR606	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35 (OPTION 05 ONLY)	03508	DA2527 (1N4152)
A12CR612	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35 (OPTION 05 ONLY)	03508	DA2527 (1N4152)
A12CR620	152-0460-00			SEMICOND DVC,DI:FE,SI,25V,1MA,TO-7 (OPTION 05 ONLY)	04713	SCL072
A12CR715	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35 (OPTION 05 ONLY)	03508	DA2527 (1N4152)
A12CR722	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A12CR784	152-0322-00	B010100	B013917	SEMICOND DVC,DI:SCHOTTKY,SI,15V,1.2PF,DO-35	50434	5082-2672
A12CR784	152-0951-00	B013918		SEMICOND DVC DI:SCHOTTKY,SI,60V,2.25PF	80009	152-0951-00
A12CR792	152-0322-00	B010100	B013917	SEMICOND DVC,DI:SCHOTTKY,SI,15V,1.2PF,DO-35	50434	5082-2672
A12CR792	152-0951-00	B013918		SEMICOND DVC DI:SCHOTTKY,SI,60V,2.25PF	80009	152-0951-00
A12CR802	152-0322-00	B010100	B013917	SEMICOND DVC,DI:SCHOTTKY,SI,15V,1.2PF,DO-35	50434	5082-2672
A12CR802	152-0951-00	B013918		SEMICOND DVC DI:SCHOTTKY,SI,60V,2.25PF	80009	152-0951-00
A12CR900	152-0322-00	B010100	B013917	SEMICOND DVC,DI:SCHOTTKY,SI,15V,1.2PF,DO-35	50434	5082-2672
A12CR900	152-0951-00	B013918		SEMICOND DVC DI:SCHOTTKY,SI,60V,2.25PF	80009	152-0951-00
A12CR902	152-0322-00	B010100	B013917	SEMICOND DVC,DI:SCHOTTKY,SI,15V,1.2PF,DO-35	50434	5082-2672
A12CR902	152-0951-00	B013918		SEMICOND DVC DI:SCHOTTKY,SI,60V,2.25PF	80009	152-0951-00
A12CR936	152-0322-00	B010100	B013917	SEMICOND DVC,DI:SCHOTTKY,SI,15V,1.2PF,DO-35	50434	5082-2672
A12CR936	152-0951-00	B013918		SEMICOND DVC DI:SCHOTTKY,SI,60V,2.25PF	80009	152-0951-00
A12CR940	152-0141-02	B014013		SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A12CR941	152-0141-02	B014013		SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A12CR942	152-0141-02	B014013		SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A12CR944	152-0322-00	B010100	B013917	SEMICOND DVC,DI:SCHOTTKY,SI,15V,1.2PF,DO-35	50434	5082-2672

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A12CR944	152-0951-00	B013918		SEMICOND DVC DI:SCHOTTKY,SI,60V,2.25PF	80009	152-0951-00
A12CR992	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A12DL580	119-1804-00			DELAY LINE,ELEC:10NS,100 OHM,3 SIP	56289	62Z03A010H
A12J103	131-3182-00			CONN,RCPT,ELEC:HDR,RTANG,2 X 25,0.1 CENTER	22526	75867-008
A12J120	131-3181-00			CONN,RCPT,ELEC:HEADER,RTANG,2 X 20,0.1 CTR	22526	75867-007
A12J123	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 8) (OPTION 05 ONLY)	22526	48283-036
A12J124	131-0608-00	B012057		TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A12J124	131-0608-00	B012305		TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (OPTION 05 ONLY)	22526	48283-036
A12J125	131-0608-00	B010100	B010299	TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 16)	22526	48283-036
A12J125	131-0608-00	B010300		TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 15)	22526	48283-036
A12J126	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 3)	22526	48283-036
A12J127	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 4)	22526	48283-036
A12J128	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 2)	22526	48283-036
A12J129	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 2)	22526	48283-036
A12J181	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 24)	22526	48283-036
A12J184	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 2)	22526	48283-036
A12J207	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 4)	22526	48283-036
A12J790	131-0608-00	B010100	B012056	TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 4)	22526	48283-036
A12J790	131-0608-00	B010100	B012303	TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 4) (OPTION 05 ONLY)	22526	48283-036
A12K302	148-0076-00			RLY,REED:FRM A,250MA,100V,COIL,5V,500 OHM	15636	R4060-1
A12L976	108-0538-00			COIL,RF:FIXED,2.7UH	76493	JWM#B7059
A12L984	108-0538-00			COIL,RF:FIXED,2.7UH	76493	JWM#B7059
A12L990	108-0538-00			COIL,RF:FIXED,2.7UH	76493	JWM#B7059
A12L992	108-0538-00			COIL,RF:FIXED,2.7UH	76493	JWM#B7059
A12LS498	119-1427-01			XDCR,AUDIO:1-4.2KHZ,30MA,6V	TK1066	QMB-06
A12Q244	151-0223-00			TRANSISTOR:NPN,SI,625MW,TO-92	04713	SPS8026
A12Q330	151-0188-00			TRANSISTOR:PNP,SI,TO-92 (OPTION 05 ONLY)	80009	151-0188-00
A12Q332	151-0223-00			TRANSISTOR:NPN,SI,625MW,TO-92	04713	SPS8026
A12Q402	151-0192-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS8801
A12Q419	151-1059-00			TRANSISTOR:FET,N-CHAN,TO-106 (OPTION 05 ONLY)	04713	ORDER BY DESCR
A12Q420	151-1059-00			TRANSISTOR:FET,N-CHAN,TO-106 (OPTION 05 ONLY)	04713	ORDER BY DESCR
A12Q422	151-0188-00			TRANSISTOR:PNP,SI,TO-92 (OPTION 05 ONLY)	80009	151-0188-00
A12Q502	151-0188-00			TRANSISTOR:PNP,SI,TO-92 (OPTION 05 ONLY)	80009	151-0188-00
A12Q504	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A12Q510	151-0188-00			TRANSISTOR:PNP,SI,TO-92 (OPTION 05 ONLY)	80009	151-0188-00
A12Q512	151-0188-00			TRANSISTOR:PNP,SI,TO-92 (OPTION 05 ONLY)	80009	151-0188-00
A12Q514	151-1059-00			TRANSISTOR:FET,N-CHAN,TO-106 (OPTION 05 ONLY)	04713	ORDER BY DESCR
A12Q588	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00

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A12Q592	151-0254-00	B010100	B010299	TRANSISTOR:DARLINGTON,NPN,SI,625MW,TO-92	03508	X38L3118
A12Q592	151-0254-03	B010300		TRANSISTOR:DARLINGTON,NPN,SI	TK1016	MPSA14, TPE2
A12Q594	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A12Q596	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A12Q612	151-0188-00			TRANSISTOR:PNP,SI,TO-92 (OPTION 05 ONLY)	80009	151-0188-00
A12Q710	151-1059-00			TRANSISTOR:FET,N-CHAN,TO-106 (OPTION 05 ONLY)	04713	ORDER BY DESCR
A12Q720	151-0223-00			TRANSISTOR:NPN,SI,625MW,TO-92	04713	SPS8026
A12Q782	151-0622-00			TRANSISTOR:PNP,SI,40V,1A,TO-226AE/237	04713	SPS8956(MPSW51A)
A12Q804	151-0622-00			TRANSISTOR:PNP,SI,40V,1A,TO-226AE/237	04713	SPS8956(MPSW51A)
A12Q806	151-0192-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS8801
A12Q842	151-0223-00			TRANSISTOR:NPN,SI,625MW,TO-92	04713	SPS8026
A12Q960	151-0223-00			TRANSISTOR:NPN,SI,625MW,TO-92	04713	SPS8026
A12R102	315-0621-00			RES,FXD,FILM:620 OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E620E
A12R104	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A12R106	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A12R116	315-0154-00			RES,FXD,FILM:150K OHM,5%,0.25W	57668	NTR25J-E150K
A12R120	315-0154-00			RES,FXD,FILM:150K OHM,5%,0.25W	57668	NTR25J-E150K
A12R122	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A12R124	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A12R130	321-0334-00			RES,FXD,FILM:29.4K OHM,1%,0.125W,TC=T0	07716	CEAD29401F
A12R132	321-0318-00			RES,FXD,FILM:20.0K OHM,1%,0.125W,TC=T0	19701	5033ED20K00F
A12R140	315-0241-00			RES,FXD,FILM:240 OHM,5%,0.25W	19701	5043CX240R0J
A12R142	315-0241-00			RES,FXD,FILM:240 OHM,5%,0.25W	19701	5043CX240R0J
A12R208	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25JE01K0
A12R210	315-0123-00			RES,FXD,FILM:12K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E12K0
A12R212	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25JE01K0
A12R214	315-0683-00			RES,FXD,FILM:68K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E68K0
A12R218	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E 100E
A12R224	315-0393-00			RES,FXD,FILM:39K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E39K0
A12R226	315-0104-00			RES,FXD,FILM:100K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E100K
A12R228	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25JE01K0
A12R234	315-0751-00			RES,FXD,FILM:750 OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E750E
A12R244	315-0473-00			RES,FXD,FILM:47K OHM,5%,0.25W	57668	NTR25J-E47K0
A12R246	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A12R274	315-0153-00			RES,FXD,FILM:15K OHM,5%,0.25W	19701	5043CX15K00J
A12R276	315-0104-00			RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K
A12R300	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A12R308	315-0162-00			RES,FXD,FILM:1.6K OHM,5%,0.25W (OPTION 05 ONLY)	19701	5043CX1K600J
A12R314	315-0474-00			RES,FXD,FILM:470K OHM,5%,0.25W (OPTION 05 ONLY)	19701	5043CX470K0J92U
A12R320	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25W	57668	NTR25J-E 2K
A12R321	315-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E02K2
A12R322	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W (OPTION 05 ONLY)	19701	5043CX10K00J
A12R323	315-0514-00			RES,FXD,FILM:510K OHM,5%,0.25W (OPTION 05 ONLY)	19701	5043CX510K0J

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A12R324	315-0123-00			RES,FXD,FILM:12K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E12K0
A12R325	315-0154-00			RES,FXD,FILM:150K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E150K
A12R326	315-0563-00			RES,FXD,FILM:56K OHM,5%,0.25W (OPTION 05 ONLY)	19701	5043CX56K00J
A12R327	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E04K7
A12R328	315-0203-00			RES,FXD,FILM:20K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E 20K
A12R329	315-0824-00			RES,FXD,FILM:820K OHM,5%,0.25W (OPTION 05 ONLY)	19701	5043CX820K0J
A12R330	315-0683-00			RES,FXD,FILM:68K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E68K0
A12R332	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A12R334	315-0272-00			RES,FXD,FILM:2.7K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E02K7
A12R336	315-0333-00			RES,FXD,FILM:33K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E33K0
A12R338	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W (OPTION 05 ONLY)	19701	5043CX10K00J
A12R342	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A12R344	321-0222-00			RES,FXD,FILM:2.00K OHM,1%,0.125W,TC=T0	19701	5033ED2K00F
A12R346	321-0193-00			RES,FXD,FILM:1K OHM,1%,0.125W,TC=T0	19701	5033ED1K00F
A12R348	321-0222-00			RES,FXD,FILM:2.00K OHM,1%,0.125W,TC=T0	19701	5033ED2K00F
A12R370	315-0201-00			RES,FXD,FILM:200 OHM,5%,0.25W	57668	NTR25J-E200E
A12R374	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A12R376	315-0201-00			RES,FXD,FILM:200 OHM,5%,0.25W	57668	NTR25J-E200E
A12R378	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A12R400	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A12R401	307-0104-00			RES,FXD,CMPSN:3.3 OHM,5%,0.25W (OPTION 05 ONLY)	01121	CB33G5
A12R402	315-0223-00			RES,FXD,FILM:22K OHM,5%,0.25W (OPTION 05 ONLY)	19701	5043CX22K00J92U
A12R403	315-0332-00			RES,FXD,FILM:3.3K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E03K3
A12R404	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E470E
A12R405	315-0182-00			RES,FXD,FILM:1.8K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E1K8
A12R406	315-0911-00			RES,FXD,FILM:910 OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E910E
A12R407	315-0123-00			RES,FXD,FILM:12K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E12K0
A12R408	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E05K1
A12R409	315-0112-00			RES,FXD,FILM:1.1K OHM,5%,0.25W (OPTION 05 ONLY)	19701	5043CX1K100J
A12R410	315-0243-00			RES,FXD,FILM:24K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E24K0
A12R411	315-0243-00			RES,FXD,FILM:24K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E24K0
A12R412	315-0104-00			RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K
A12R413	315-0104-00			RES,FXD,FILM:100K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E100K
A12R414	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W (OPTION 05 ONLY)	19701	5043CX10K00J
A12R415	315-0273-00			RES,FXD,FILM:27K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E27K0
A12R416	315-0104-00			RES,FXD,FILM:100K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E100K

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A12R417	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W (OPTION 05 ONLY)	19701	5043CX10K00J
A12R418	315-0391-00			RES,FXD,FILM:390 OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E390E
A12R419	315-0112-00			RES,FXD,FILM:1.1K OHM,5%,0.25W (OPTION 05 ONLY)	19701	5043CX1K100J
A12R420	315-0104-00			RES,FXD,FILM:100K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E100K
A12R421	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W (OPTION 05 ONLY)	19701	5043CX10K00J
A12R422	315-0392-00			RES,FXD,FILM:3.9K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E03K9
A12R423	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25JE01K0
A12R424	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W (OPTION 05 ONLY)	19701	5043CX10K00J
A12R425	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W (OPTION 05 ONLY)	19701	5043CX10K00J
A12R426	315-0203-00			RES,FXD,FILM:20K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E 20K
A12R427	315-0163-00			RES,FXD,FILM:16K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E 16K
A12R428	315-0334-00			RES,FXD,FILM:330K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E 330K
A12R429	315-0204-00			RES,FXD,FILM:200K OHM,5%,0.25W (OPTION 05 ONLY)	19701	5043CX200K0J
A12R474	307-0446-00			RES NTWK,FXD,FI:10K OHM,20%,(9)RES	11236	750-101-R10K
A12R502	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25JE01K0
A12R506	315-0432-00			RES,FXD,FILM:4.3K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E04K3
A12R512	315-0153-00			RES,FXD,FILM:15K OHM,5%,0.25W (OPTION 05 ONLY)	19701	5043CX15K00J
A12R524	315-0511-00			RES,FXD,FILM:510 OHM,5%,0.25W (OPTION 05 ONLY)	19701	5043CX510R0J
A12R529	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E 100E
A12R572	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A12R580	315-0241-00			RES,FXD,FILM:240 OHM,5%,0.25W	19701	5043CX240R0J
A12R582	315-0241-00			RES,FXD,FILM:240 OHM,5%,0.25W	19701	5043CX240R0J
A12R584	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A12R590	307-0446-00			RES NTWK,FXD,FI:10K OHM,20%,(9)RES	11236	750-101-R10K
A12R592	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A12R594	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A12R596	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A12R597	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A12R598	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A12R602	315-0122-00			RES,FXD,FILM:1.2K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E01K2
A12R603	315-0392-00			RES,FXD,FILM:3.9K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E03K9
A12R604	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E04K7
A12R606	315-0303-00			RES,FXD,FILM:30K OHM,5%,0.25W (OPTION 05 ONLY)	19701	5043CX30K00J
A12R607	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25JE01K0
A12R608	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25JE01K0
A12R609	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25JE01K0

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A12R610	315-0394-00			RES,FXD,FILM:390K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E390K
A12R612	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W (OPTION 05 ONLY)	19701	5043CX10K00J
A12R613	315-0201-00			RES,FXD,FILM:200 OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E200E
A12R614	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E470E
A12R616	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E47E0
A12R617	315-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E02K2
A12R622	321-0226-00			RES,FXD,FILM:2.21K OHM,1%,0.125W,TC=T0 (OPTION 05 ONLY)	01121	RNK2211F
A12R624	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25W (OPTION 05 ONLY)	19701	5043CX10RR00J
A12R626	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E 100E
A12R628	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A12R646	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A12R648	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A12R700	321-0251-00			RES,FXD,FILM:4.02K OHM,1%,0.125W,TC=T0 (OPTION 05 ONLY)	19701	5033ED4K020F
A12R711	315-0475-00			RES,FXD,FILM:4.7M OHM,5%,0.25W (OPTION 05 ONLY)	01121	CB4755
A12R712	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25JE01K0
A12R713	315-0564-00			RES,FXD,FILM:560K OHM,5%,0.25W (OPTION 05 ONLY)	19701	5043CX560K0J
A12R714	315-0394-00			RES,FXD,FILM:390K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E390K
A12R715	315-0392-00			RES,FXD,FILM:3.9K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25J-E03K9
A12R716	315-0101-00	B010100	B010399	RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A12R716	315-0620-00	B010400		RES,FXD,FILM:62 OHM,5%,0.25W	19701	5043CX63R00J
A12R717	315-0181-00			RES,FXD,FILM:180 OHM,5%,0.25W	57668	NTR25J-E180E
A12R718	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A12R719	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25W (OPTION 05 ONLY)	19701	5043CX10RR00J
A12R722	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A12R742	307-0446-00			RES NTWK,FXD,FI:10K OHM,20%,(9)RES	11236	750-101-R10K
A12R744	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A12R746	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A12R748	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A12R764	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A12R784	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A12R786	315-0561-00			RES,FXD,FILM:560 OHM,5%,0.25W	19701	5043CX560R0J
A12R792	315-0151-00			RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A12R794	315-0151-00			RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A12R796	315-0151-00			RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A12R800	315-0561-00			RES,FXD,FILM:560 OHM,5%,0.25W	19701	5043CX560R0J
A12R802	315-0106-00			RES,FXD,FILM:10M OHM,5%,0.25W	01121	CB1065
A12R810	315-0121-00			RES,FXD,FILM:120 OHM,5%,0.25W (OPTION 05 ONLY)	19701	5043CX120R0J
A12R812	321-0155-00			RES,FXD,FILM:402 OHM,1%,0.125W,TC=T0	07716	CEAD402R0F
A12R814	321-0097-00			RES,FXD,FILM:100 OHM,1%,0.125W,TC=T0	91637	CMF55116G100R0F
A12R816	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W (OPTION 05 ONLY)	57668	NTR25JE01K0
A12R820	315-0560-00			RES,FXD,FILM:56 OHM,5%,0.25W	57668	NTR25J-E56E0
A12R822	315-0560-00			RES,FXD,FILM:56 OHM,5%,0.25W	57668	NTR25J-E56E0

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A12R830	307-0675-00			RES NTWK,FXD,FI:9,1K OHM,2%1.25W	11236	750-101-R1K OHM
A12R894	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A12R896	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A12R900	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A12R936	315-0564-00	B010100	B010399	RES,FXD,FILM:560K OHM,5%,0.25W	19701	5043CX560K0J
A12R936	315-0104-00	B010400	B012056	RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K
A12R936	315-0204-00	B012057		RES,FXD,FILM:200K OHM,5%,0.25W (STANDARD ONLY)	19701	5043CX200K0J
A12R936	315-0104-00	B010100	B012303	RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K
A12R936	315-0204-00	B012304		RES,FXD,FILM:200K OHM,5%,0.25W (OPTION 05 ONLY)	19701	5043CX200K0J
A12R938	315-0114-00	B010100	B010399	RES,FXD,FILM:110K OHM,5%,0.25W	19701	5043CX110K0J
A12R938	321-0643-00	B010400	B014012	RES,FXD,FILM:22.1K OHM,0.25%,0.125W,TC=9	19701	5033RE22K10C
A12R938	321-0318-00	B014013		RES,FXD,FILM:20.0K OHM,1%,0.125W,TC=T0	19701	5033ED20K00F
A12R940	315-0562-00	B010100	B014012	RES,FXD,FILM:5.6K OHM,5%,0.25W	57668	NTR25J-E05K6
A12R941	315-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.25W	57668	NTR25J-E02K2
A12R942	315-0243-00			RES,FXD,FILM:24K OHM,5%,0.25W	57668	NTR25J-E24K0
A12R943	321-0243-00			RES,FXD,FILM:3.32K OHM,1%,0.125W,TC=T0	19701	5033ED3K32F
A12R944	321-0273-00			RES,FXD,FILM:6.81K OHM,1%,0.125W,TC=T0	07716	CEAD68100F
A12R945	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A12R946	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A12R948	315-0183-00			RES,FXD,FILM:18K OHM,5%,0.25W	19701	5043CX18K00J
A12R952	321-0222-00			RES,FXD,FILM:2.00K OHM,1%,0.125W,TC=T0	19701	5033ED2K00F
A12R954	321-0193-00			RES,FXD,FILM:1K OHM,1%,0.125W,TC=T0	19701	5033ED1K00F
A12R956	321-0222-00			RES,FXD,FILM:2.00K OHM,1%,0.125W,TC=T0	19701	5033ED2K00F
A12R957	315-0103-00	B012057		RES,FXD,FILM:10K OHM,5%,0.25W (STANDARD ONLY)	19701	5043CX10K00J
A12R957	315-0103-00	B012305		RES,FXD,FILM:10K OHM,5%,0.25W (OPTION 05 ONLY)	19701	5043CX10K00J
A12TP332	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A12TP370	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A12TP371	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A12TP372	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A12TP373	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A12TP374	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A12TP375	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A12TP562	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A12TP572	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A12TP574	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A12TP578	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A12TP580	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A12TP842	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A12TP902	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A12U120	156-1200-01			MICROCKT,LINEAR:OPNL AMPL,QUAD BIFET	80009	156-1200-01
A12U130	156-0515-02			MICROCKT,DGTL:TRIPLE 3-CHAN MUX,SEL	80009	156-0515-02
A12U220	156-0366-02			MICROCKT,DGTL:CMOS,DUAL D FLIP-FLOP,SCRN (OPTION 05 ONLY)	02735	CD4013BFX
A12U250	156-0739-02			MICROCKT,DGTL:QUAD 2 INP OR GATE,SCREENED	18324	N74S32(NB OR FB)
A12U254	156-0323-02			MICROCKT,DGTL:HEX INVERTER,BURN-IN	18324	N74S04(NB OR FB)
A12U260	156-1220-01			MICROCKT,DGTL:HEX BUS DRIVER,SCREENED	01295	SN74LS365NP3
A12U262	156-1220-01			MICROCKT,DGTL:HEX BUS DRIVER,SCREENED	01295	SN74LS365NP3
A12U264	156-0739-02			MICROCKT,DGTL:QUAD 2 INP OR GATE,SCREENED	18324	N74S32(NB OR FB)
A12U270	156-0323-02			MICROCKT,DGTL:HEX INVERTER,BURN-IN	18324	N74S04(NB OR FB)
A12U274	156-0402-00			MICROCKT,LINEAR:TIMER	27014	LM555CN
A12U308	156-0575-03			MICROCKT,DGTL:3 INPUT NOR GATE,SELECTED (OPTION 05 ONLY)	02735	CD4025BFX
A12U310	156-0366-02			MICROCKT,DGTL:CMOS,DUAL D FLIP-FLOP,SCRN (OPTION 05 ONLY)	02735	CD4013BFX
A12U314	156-0704-00			MICROCKT,LINEAR:CMOS,PHASE LOCK LOOP	04713	MC14046CP

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A12U332	156-0479-02			MICROCKT,DGTL:QUAD 2-INP OR GATE,SCRN	01295	SN74LS32NP3
A12U350	156-2274-00			MICROCKT,DGTL:CMOS,8192 X 8 SRAM	62786	HM6264LP-12
A12U352	156-1725-00			MICROCKT,DGTL:OCTAL BIDIRECTIONAL XCVR	04713	MC74F245ND
A12U360	156-1725-00			MICROCKT,DGTL:OCTAL BIDIRECTIONAL XCVR	04713	MC74F245ND
A12U364	156-1721-00			MICROCKT,DGTL:ASTTL,OCTAL TRANSPARENT LATCH	04713	MC74F373ND
A12U410	156-1381-00			MICROCKT,LINEAR:3 NPN,2 PNP,XSTR ARRAY (OPTION 05 ONLY)	02735	CA3096AE-17
A12U420	156-1381-00			MICROCKT,LINEAR:3 NPN,2 PNP,XSTR ARRAY (OPTION 05 ONLY)	02735	CA3096AE-17
A12U424	156-0385-02			MICROCKT,DGTL:HEX INVERTER,SCRN	07263	74LS04PCQR
A12U430	156-0366-02			MICROCKT,DGTL:CMOS,DUAL D FLIP-FLOP,SCRN (OPTION 05 ONLY)	02735	CD4013BFX
A12U432	156-2016-00			MICROCKT,DGTL:NMOS,2048 X 8 SRAM	TK1016	TMM2016AP-10
A12U440	156-2016-00			MICROCKT,DGTL:NMOS,2048 X 8 SRAM	TK1016	TMM2016AP-10
A12U470	156-2380-00			MICROCKT,DGTL:CUST WAVEFORM PROCESSOR	80009	156-2380-00
A12U480	160-2556-00	B010100	B010435	MICROCKT,DGTL:2048 X 8 PROM,PRGM	80009	160-2556-00
A12U480	160-2556-01	B010436	B011409	MICROCKT,DGTL:STTL,4096 X 8 PROM,PRGM	80009	160-2556-01
A12U480	160-2556-02	B011410		MICROCKT,DGTL:STTL,4096 X 8 PROM,PRGM (STANDARD AND OPTION 05 ONLY)	80009	160-2556-02
A12U480	160-4173-00	B010100	B020099	MICROCKT,DGTL:32768 X 8 EPROM,PRGM (2430M ONLY) (NOT PART OF CIRCUIT BOARD)	80009	160-4173-00
A12U490	160-2557-00	B010100	B010435	MICROCKT,DGTL:2048 X 8 PROM,PRGM	80009	160-2557-00
A12U490	160-2557-01	B010436	B011409	MICROCKT,DGTL:STTL,4096 X 8 PROM,PRGM	80009	160-2557-01
A12U490	160-2557-02	B011410		MICROCKT,DGTL:STTL,4096 X 8 PROM,PRGM (STANDARD AND OPTION 05 ONLY)	80009	160-2557-02
A12U490	160-4174-00	B010100	B020099	MICROCKT,DGTL:32768 X 8 PROM,PRGM (2430M ONLY) (NOT PART OF CIRCUIT BOARD)	80009	160-4174-00
A12U504	156-0912-01			MICROCKT,LINEAR:OPNL AMPL,SCREENED (OPTION 05 ONLY)	02735	CA3080EX-98
A12U510	156-0912-01			MICROCKT,LINEAR:OPNL AMPL,SCREENED (OPTION 05 ONLY)	02735	CA3080EX-98
A12U514	156-0912-01			MICROCKT,LINEAR:OPNL AMPL,SCREENED (OPTION 05 ONLY)	02735	CA3080EX-98
A12U520	156-0912-01			MICROCKT,LINEAR:OPNL AMPL,SCREENED (OPTION 05 ONLY)	02735	CA3080EX-98
A12U524	156-0388-03			MICROCKT,DGTL:DUAL D FLIP-FLOP,SCRN (OPTION 05 ONLY)	01295	SN74LS74ANP3
A12U530	156-1426-00			MICROCKT,DGTL:NMOS,PROGRAMMABLE TIMER MDL (OPTION 05 ONLY)	04713	MC68B40 (L OR P)
A12U532	156-1111-02			MICROCKT,DGTL:OCTAL BUS XCVR W/3 STATE OUT	01295	SN74LS245N3
A12U540	156-0469-02			MICROCKT,DGTL:3/8 LINE DCDR,SCRN	01295	SN74LS138NP3
A12U541	156-0382-02			MICROCKT,DGTL:QUAD 2 INP NAND GATE BURN (OPTION 05 ONLY)	18324	N74LS00NB
A12U542	156-1962-00			MICROCKT,DGTL:OCTAL BUFFER/LINE DRIVER,SCRN	04713	MC74F244N
A12U550	156-1326-00			MICROCKT,DGTL:LSTTL,QUAD D TYPE FF,SCRN	01295	SN74LS379 N3
A12U552	156-1111-02			MICROCKT,DGTL:OCTAL BUS XCVR W/3 STATE OUT	01295	SN74LS245N3
A12U560	156-1962-00			MICROCKT,DGTL:OCTAL BUFFER/LINE DRIVER,SCRN	04713	MC74F244N
A12U562	156-1721-00			MICROCKT,DGTL:ASTTL,OCTAL TRANSPARENT LATCH	04713	MC74F373ND
A12U564	156-0956-02			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT,SCRN	01295	SN74LS244NP3
A12U570	156-0694-02			MICROCKT,DGTL:DECODER/3 LINE TO 8 LINE,SCRN	01295	SN74S138N3/J4
A12U572	156-1722-00			MICROCKT,DGTL:HEX INVERTER	04713	MC74F04ND
A12U580	156-0459-02			MICROCKT,DGTL:QUAD 2 INPUT & GATE,BURN IN	18324	N74S08(NB OR FB)
A12U610	156-0048-00			MICROCKT,LINEAR:5 XSTR ARRAY (OPTION 05 ONLY)	02735	CA3046
A12U612	156-1349-00			MICROCKT,LINEAR:DUAL INDEP DIFF AMPL (OPTION 05 ONLY)	02735	CA3054-98
A12U624	156-1414-02			MICROCKT,DGTL:OCTAL GPIB BUS XCVR,SCRN	27014	DS75160A N
A12U630	156-1444-01			MICROCKT,DGTL:NMOS,GPIB INTFC CONTROLLER	01295	TMS9914A (NL

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A12U632	156-0956-02			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT,SCRN	01295	SN74LS244NP3
A12U640	156-1494-01			MICROCKT,DGTL:8-BIT MICROPRC,SCRN	04713	MC68B09
A12U650	156-1111-02			MICROCKT,DGTL:OCTAL BUS XCVR W/3 STATE OUT	01295	SN74LS245N3
A12U654	156-0956-02			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT,SCRN	01295	SN74LS244NP3
A12U660	156-1111-02			MICROCKT,DGTL:OCTAL BUS XCVR W/3 STATE OUT	01295	SN74LS245N3
A12U664	156-2015-00			MICROCKT,DGTL:CMOS,2048 X 8 SRAM	TK1016	TC5517APL-2
A12U668	156-2016-00			MICROCKT,DGTL:NMOS,2048 X 8 SRAM	TK1016	TMM2016AP-10
A12U670	160-2555-00	B010100	B010435	MICROCKT,DGTL:16384 X 8 EPROM,PRGM	80009	160-2555-00
A12U670	160-2555-01	B010436	B011409	MICROCKT,DGTL:16384 X 8 EPROM,PRGM	80009	160-2555-01
A12U670	160-2555-02	B011410	B014160	MICROCKT,DGTL:16384 X 8 EPROM,PRGM	80009	160-2555-02
A12U670	160-2555-03	B014161	B014161	MICROCKT,DGTL:16384 X 8 EPROM,PRGM	80009	160-2555-03
A12U670	160-2555-05	B014162		MICROCKT,DGTL:16384 X 8 EPROM,PRGM (STANDARD AND OPTION 05 ONLY)	80009	160-2555-05
A12U670	160-4168-00	B010100	B014161	MICROCKT,DGTL:16384 X 8 EPROM,PRGM	80009	160-4168-00
A12U670	160-4168-02	B014162		MICROCKT,DGTL:16384 X 8 EPROM,PRGM (2430M ONLY) (NOT PART OF INSTRUMENT)	80009	160-4168-02
A12U680	160-2551-00	B010100	B010435	MICROCKT,DGTL:16384 X 8 EPROM,PRGM	80009	160-2551-00
A12U680	160-2551-01	B010436	B011409	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-2551-01
A12U680	160-2551-02	B011410	B014160	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-2551-02
A12U680	160-2551-03	B014161	B014161	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-2551-03
A12U680	160-2551-05	B014162		MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM (STANDARD AND OPTION 05 ONLY)	80009	160-2551-05
A12U680	160-4169-00	B010100	B014161	MICROCKT,DGTL:16384 X 8 EPROM,PRGM	80009	160-4169-00
A12U680	160-4169-02	B014162		MICROCKT,DGTL:16384 X 8 EPROM,PRGM (2430M ONLY) (NOT PART OF CIRCUIT BOARD)	80009	160-4169-02
A12U682	160-2552-00	B010100	B010435	MICROCKT,DGTL:16384 X 8 EPROM,PRGM	80009	160-2552-00
A12U682	160-2552-01	B010436	B011409	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-2552-01
A12U682	160-2552-02	B011410	B014160	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-2552-02
A12U682	160-2552-03	B014161	B014161	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-2552-03
A12U682	160-2552-05	B014162		MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM (STANDARD AND OPTION 05 ONLY)	80009	160-2552-05
A12U682	160-4170-00	B010100	B014161	MICROCKT,DGTL:16384 X 8 EPROM,PRGM	80009	160-4170-00
A12U682	160-4170-02	B014162		MICROCKT,DGTL:16384 X 8 EPROM,PRGM (2430M ONLY) (NOT PART OF CIRCUIT BOARD)	80009	160-4170-02
A12U690	160-2553-00	B010100	B010435	MICROCKT,DGTL:16384 X 8 EPROM,PRGM	80009	160-2553-00
A12U690	160-2553-01	B010436	B011409	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-2553-01
A12U690	160-2553-02	B011410	B014160	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-2553-02
A12U690	160-2553-03	B014161	B014161	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-2553-03
A12U690	160-2553-05	B014162		MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM (STANDARD AND OPTION 05 ONLY)	80009	160-2553-05
A12U690	160-4171-00	B010100	B014161	MICROCKT,DGTL:16384 X 8 EPROM,PRGM	80009	160-4171-00
A12U690	160-4171-02	B014162		MICROCKT,DGTL:16384 X 8 EPROM,PRGM (2430M ONLY) (NOT PART OF CIRCUIT BOARD)	80009	160-4171-02
A12U692	160-2554-00	B010100	B010435	MICROCKT,DGTL:16384 X 8 EPROM,PRGM	80009	160-2554-00
A12U692	160-2554-01	B010436	B011409	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-2554-01
A12U692	160-2554-02	B011410	B014160	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-2554-02
A12U692	160-2554-03	B014161	B014161	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-2554-03
A12U692	160-2554-05	B014162		MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM (STANDARD AND OPTION 05 ONLY)	80009	160-2554-05
A12U692	160-4172-00	B010100	B014161	MICROCKT,DGTL:16384 X 8 EPROM,PRGM	80009	160-4172-00
A12U692	160-4172-02	B014162		MICROCKT,DGTL:16384 X 8 EPROM,PRGM (2430M ONLY) (NOT PART OF INSTRUMENT)	80009	160-4172-02
A12U710	156-1200-01			MICROCKT,LINEAR:OPNL AMPL,QUAD BIFET (OPTION 05 ONLY)	80009	156-1200-01
A12U720	156-2013-00			MICROCKT,DGTL:STTL,IEEE-488 XCVR	27014	DS75162AN

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A12U730	156-0956-02			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT,SCRN	01295	SN74LS244NP3
A12U750	156-0865-02			MICROCKT,DGTL:OCTAL D FF W/CLEAR,SCRN	01295	SN74LS273NP3
A12U754	156-0865-02			MICROCKT,DGTL:OCTAL D FF W/CLEAR,SCRN	01295	SN74LS273NP3
A12U760	156-0865-02			MICROCKT,DGTL:OCTAL D FF W/CLEAR,SCRN	01295	SN74LS273NP3
A12U830	156-0914-02			MICROCKT,DGTL:OCT ST BFR W/3 STATE OUT,SCRN	80009	156-0914-02
A12U840	156-1724-00			MICROCKT,DGTL:QUAD 2 INPUT OR GATE	04713	MC74F32ND
A12U844	156-1216-01			MICROCKT,DGTL:QUAD 2 INP NAND BFR,SCRN	01295	SN74S37JP4
A12U850	156-0985-01			MICROCKT,DGTL:DUAL 5-INPUT NOR GATE,SCRN	04713	SN74LS260NDS
A12U854	156-0956-02			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT,SCRN	01295	SN74LS244NP3
A12U860	156-0865-02			MICROCKT,DGTL:OCTAL D FF W/CLEAR,SCRN	01295	SN74LS273NP3
A12U862	156-0478-02			MICROCKT,DGTL:DUAL 4-INP & GATE,SCRN	01295	SN74LS21NP3
A12U866	156-0323-02			MICROCKT,DGTL:HEX INVERTER,BURN-IN	18324	N74S04(NB OR FB)
A12U870	156-0180-04			MICROCKT,DGTL:QUAD 2 INP NAND GATE,	18324	N74S00(NB OR FB)
A12U874	156-0382-02			MICROCKT,DGTL:QUAD 2 INP NAND GATE BURN	18324	N74LS00NB
A12U880	156-0480-02			MICROCKT,DGTL:QUAD 2-INP & GATE,SCRN,	01295	SN74LS08NP3
A12U884	156-0469-02			MICROCKT,DGTL:3/8 LINE DCDR,SCRN	01295	SN74LS138NP3
A12U890	156-0693-02			MICROCKT,DGTL:DUAL 2 TO 4 LINE DCDR/DEMUX	01295	SN74S139NP3
A12U894	156-0388-03			MICROCKT,DGTL:DUAL D FLIP-FLOP,SCRN	01295	SN74LS74ANP3
A12U940	156-1191-01			MICROCKT,LINEAR:DUAL BI-FET OP-AMP,8 DIP	80009	156-1191-01
A12VR234	152-0166-00			SEMICOND DVC,DI:ZEN,SI,6.2V,5%,400MW,DO-7 (OPTION 05 ONLY)	04713	SZ11738RL
A12VR717	152-0278-00			SEMICOND DVC,DI:ZEN,SI,3V,5%,0.4W,DO-7	80009	152-0278-00
A12VR816	152-0175-00			SEMICOND DVC,DI:ZEN,SI,5.6V,5%,0.5W,DO-7 (OPTION 05 ONLY)	14552	TD3810976
A12W123	175-9358-00			CA ASSY,SP,ELEC:8,26 AWG,15.0 L,RIBBON (OPTION 05 ONLY)	80009	175-9358-00
A12W130	175-9025-00			CA ASSY,SP,ELEC:50, 28 AWG,1.7 L	80009	175-9025-00
A12W378	131-0566-00	B010100	B010399	BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A12W380	131-0566-00	B010400		BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07

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A13	670-8167-00	B010100	B010699	CIRCUIT BD ASSY:SIDE	80009	670-8167-00
A13	670-8167-01	B010700	B014161	CIRCUIT BD ASSY:SIDE	80009	670-8167-01
A13	670-9749-01	B014162		CIRCUIT BD ASSY:SIDE (2430 ONLY)	80009	670-9749-01
A13	670-8167-01	B010100	B019999	CIRCUIT BD ASSY:SIDE (2430M ONLY)	80009	670-8167-01
A13C700	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A13C701	281-0775-00	B010100	B013899	CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A13C701	283-0177-05	B013900		CAP,FXD,CER DI:1UF,+80-20%,25V (2430 ONLY)	04222	SR302E105ZAATR
A13C701	281-0775-00	B010100	B010139	CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A13C701	283-0177-05	B010140		CAP,FXD,CER DI:1UF,+80-20%,25V (2430M ONLY)	04222	SR302E105ZAATR
A13C702	290-0967-00			CAP,FXD,ELCTLT:22UF,+50-10%,25V	55680	TLB1E220TAAANA
A13C731	290-0967-00			CAP,FXD,ELCTLT:22UF,+50-10%,25V	55680	TLB1E220TAAANA
A13C781	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A13C800	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A13C801	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A13C811	281-0814-00			CAP,FXD,CER DI:100 PF,10%,100V	04222	MA101A101KAA
A13C812	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A13C813	281-0814-00			CAP,FXD,CER DI:100 PF,10%,100V	04222	MA101A101KAA
A13C831	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A13C832	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A13C833	281-0757-00			CAP,FXD,CER DI:10PF,20%,100V TUBULAR,MI	04222	MA101A100MAA
A13C841	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A13C842	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A13C843	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A13C852	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A13C861	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A13C864	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A13C871	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A13C872	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A13C873	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A13C881	290-0183-00			CAP,FXD,ELCTLT:1UF,10%,35V	05397	T322B105K035AS
A13C882	281-0865-00			CAP,FXD,CER DI:1000PF,5%,100V	04222	MA101A102JAA
A13C883	281-0814-00			CAP,FXD,CER DI:100 PF,10%,100V	04222	MA101A101KAA
A13C884	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A13C885	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A13CR761	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A13CR771	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A13CR772	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A13CR773	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A13J150	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 26)	22526	48283-036
A13J155	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 3)	22526	48283-036
A13J156	131-0707-00	B010258	B010299	CONTACT,ELEC:22-26 AWG,BRS,CU BE GLD PL	22526	47439-000
A13J156	131-0608-00	B010300		TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A13Q761	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A13Q771	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A13Q772	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A13Q773	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A13Q781	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A13Q782	151-1121-00			TRANSISTOR:FE,N CHANNEL,SI,TO-92	17856	V10206
A13Q783	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A13Q831	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A13R701	315-0103-00	B010100	B014126	RES,FXD,FILM:10K OHM,5%,0.25W (2430 ONLY)	19701	5043CX10K00J
A13R701	315-0103-00	B010100	B010145	RES,FXD,FILM:10K OHM,5%,0.25W (2430M ONLY)	19701	5043CX10K00J

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A13R711	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A13R731	321-1682-07			RES,FXD,FILM:5.7K OHM,0.1%,0.125W,TC=T9	19701	5033RE5K701B
A13R732	321-0641-07			RES,FXD,FILM:1.8K OHM,0.1,0.125W,TC=T9	07716	CEAE 18000B
A13R741	315-0162-00			RES,FXD,FILM:1.6K OHM,5%,0.25W	19701	5043CX1K600J
A13R761	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A13R762	321-1489-00			RES,FXD,FILM:1.23M,1%,0.125W,TC=T0	01121	CC1234FY
A13R771	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A13R772	321-0293-00			RES,FXD,FILM:11.0K OHM,1%,0.125W,TC=T0	07716	CEAD11001F
A13R773	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A13R774	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A13R775	321-0393-00			RES,FXD,FILM:121K OHM,1%,0.125W,TC=T0	19701	5043ED121K0F
A13R780	321-1720-00			RES,FXD,FILM:3.24M OHM,1%,0.125W,TC=T0	14298	AME57G32403F-T/R
A13R781	321-0556-00			RES,FXD,FILM:6.04M OHM,1.0%,0.125W,TC=T0	03888	PME60 6.04M 1%
A13R782	321-0556-00			RES,FXD,FILM:6.04M OHM,1.0%,0.125W,TC=T0	03888	PME60 6.04M 1%
A13R783	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A13R784	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A13R800	307-0648-00			RES NTWK,FXD,FI:8,100 OHM,2%,0.125 W	01121	316B101
A13R801	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A13R802	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A13R803	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A13R804	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A13R805	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A13R806	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A13R807	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A13R808	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A13R809	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A13R810	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A13R811	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A13R812	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A13R813	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A13R814	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A13R815	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A13R831	321-0657-07			RES,FXD,FILM:60 OHM,0.1%,0.125W,TC=T9	57668	RB14BZE 60E
A13R832	321-0808-03			RES,FXD,FILM:300 OHM,0.25%,0.125W,TC=T2	57668	RB14CYE 300E
A13R833	321-0282-00			RES,FXD,FILM:8.45K OHM,1%,0.125W,TC=T0	07716	CFAD84500F
A13R834	321-0293-00			RES,FXD,FILM:11.0K OHM,1%,0.125W,TC=T0	07716	CEAD11001F
A13R835	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A13R841	315-0621-00			RES,FXD,FILM:620 OHM,5%,0.25W	57668	NTR25J-E620E
A13R842	315-0162-00			RES,FXD,FILM:1.6K OHM,5%,0.25W	19701	5043CX1K600J
A13R843	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A13R844	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A13R861	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A13R862	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A13R863	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A13R871	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A13R881	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A13R882	321-0271-00			RES,FXD,FILM:6.49K OHM,1%,0.125W,TC=T0	07716	CEAD64900F
A13R883	321-0245-00			RES,FXD,FILM:3.48K OHM,1%,0.125W,TC=T0	19701	5033ED3K48F
A13R884	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A13R885	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A13R886	315-0183-00			RES,FXD,FILM:18K OHM,5%,0.25W	19701	5043CX18K00J
A13R887	315-0183-00			RES,FXD,FILM:18K OHM,5%,0.25W	19701	5043CX18K00J
A13R888	315-0162-00			RES,FXD,FILM:1.6K OHM,5%,0.25W	19701	5043CX1K600J
A13R889	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A13TP701	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A13TP702	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A13TP811	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A13TP812	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A13TP813	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A13TP814	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A13TP815	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A13TP821	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A13TP822	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A13TP823	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A13TP824	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A13TP825	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A13TP826	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A13TP827	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A13TP871	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A13TP881	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A13U700	160-2405-00	B010100	B014126	MICROCKT,DGTL:8 BIT MICROCOMPUTER W/CLOCK	04713	MC6805R3P
A13U700	160-2405-01	B014127		MICROCKT,DGTL:8 BIT MICROCOMPUTER W/CLOCK (2430 ONLY)	80009	160-2405-01
A13U700	160-2405-00	B010100	B010145	MICROCKT,DGTL:8 BIT MICROCOMPUTER W/CLOCK	04713	MC6805R3P
A13U700	160-2405-01	B010146	B019999	MICROCKT,DGTL:8 BIT MICROCOMPUTER W/CLOCK (2430M ONLY)	80009	160-2405-01
A13U731	156-1149-01			MICROCKT,LINEAR:OPERATION AMP JFET INPUT	27014	AL160307
A13U741	156-1221-00			MICROCKT,DGTL:LSTTL,HEX D-TYPE FF,SCRN	01295	SN74LS378N3
A13U742	156-1065-01			MICROCKT,DGTL:OCTAL D TYPE TRANS LATCHES	04713	SN74LS373 ND/JD
A13U751	156-0956-02			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT,SCRN	01295	SN74LS244NP3
A13U752	156-1277-00			MICROCKT,DGTL:LSTTL,3-STATE OCTAL BFR,SCRN	27014	DM81LS95ANA+
A13U753	156-1277-00			MICROCKT,DGTL:LSTTL,3-STATE OCTAL BFR,SCRN	27014	DM81LS95ANA+
A13U761	156-1277-00			MICROCKT,DGTL:LSTTL,3-STATE OCTAL BFR,SCRN	27014	DM81LS95ANA+
A13U762	156-1221-00			MICROCKT,DGTL:LSTTL,HEX D-TYPE FF,SCRN	01295	SN74LS378N3
A13U781	156-0469-02			MICROCKT,DGTL:3/8 LINE DCDR,SCRN	01295	SN74LS138NP3
A13U831	156-0048-00			MICROCKT,LINEAR:5 XSTR ARRAY	02735	CA3046
A13U841	156-1611-00			MICROCKT,DGTL:ASTTL,DUAL D TYPE EDGE-TRIG	80009	156-1611-00
A13U842	156-1611-00			MICROCKT,DGTL:ASTTL,DUAL D TYPE EDGE-TRIG	80009	156-1611-00
A13U851	156-1724-00			MICROCKT,DGTL:QUAD 2 INPUT OR GATE	04713	MC74F32ND
A13U852	156-1172-01			MICROCKT,DGTL:DUAL 4 BIT BIN CNTR,SCRN	01295	SN74LS393NP3
A13U853	156-1172-01			MICROCKT,DGTL:DUAL 4 BIT BIN CNTR,SCRN	01295	SN74LS393NP3
A13U861	156-0388-03			MICROCKT,DGTL:DUAL D FLIP-FLOP,SCRN	01295	SN74LS74ANP3
A13U862	156-0383-02			MICROCKT,DGTL:QUAD 2-INP NOR GATE,SCRN,	18324	N74LS02NB
A13U871	156-1126-01			MICROCKT,LINEAR:VOLTAGE COMPARATOR,SELECTED	01295	LM311JG4
A13U872	156-0388-03			MICROCKT,DGTL:DUAL D FLIP-FLOP,SCRN	01295	SN74LS74ANP3
A13U881	156-1126-01			MICROCKT,LINEAR:VOLTAGE COMPARATOR,SELECTED	01295	LM311JG4
A13VR841	152-0195-00			SEMICOND DVC,DI:ZEN,SI,5.1V,5%,0.4W,DO-7	04713	SZ11755RL
A13W101	175-9023-00			CA ASSY,SP,ELEC:50,28 AWG,8.675 L	80009	175-9023-00
A13W110	175-9027-00			CA ASSY,SP,ELEC:40,28 AWG,1.4 L	80009	175-9027-00
A13W122	175-9024-00			CA ASSY,SP,ELEC:40,28 AWG,3.5 L	80009	175-9024-00
A13W701	131-0566-00	B014127		BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L (2430 ONLY)	24546	OMA 07
A13W701	131-0566-00	B010146	B019999	BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L (2430M ONLY)	24546	OMA 07
A13W800	131-0566-00	B010100	B014126	BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L (2430 ONLY)	24546	OMA 07
A13W800	131-0566-00	B010100	B010145	BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L (2430M ONLY)	24546	OMA 07
A13W860	131-0566-00	B010100	B010321	BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A13XU700	136-0757-00	B014127		SKT,PL-IN ELEK:MICROCIRCUIT,40 DIP (2430 ONLY)	09922	DILB40P-108
A13XU700	136-0757-00	B010146	B019999	SKT,PL-IN ELEK:MICROCIRCUIT,40 DIP (2430M ONLY)	09922	DILB40P-108

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A14	670-8168-00	B010100	B010699	CIRCUIT BD ASSY:FRONT PANEL	80009	670-8168-00
A14	670-8168-01	B010700	B011236	CIRCUIT BD ASSY:FRONT PANEL	80009	670-8168-01
A14	670-8168-02	B011237	B012532	CIRCUIT BD ASSY:FRONT PANEL	80009	670-8168-02
A14	670-8168-03	B012533		CIRCUIT BD ASSY:FRONT PANEL	80009	670-8168-03
A14C902	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A14C903	290-0943-00	B010100	B013921	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A14C903	290-0943-02	B013922		CAP,FXD,ELCTLT:47UF,20%,25V (2430 ONLY)	55680	UVX1E470MAA1TD
A14C903	290-0943-00	B010100	B010139	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A14C903	290-0943-02	B010140		CAP,FXD,ELCTLT:47UF,20%,25V (2430M ONLY)	55680	UVX1E470MAA1TD
A14C904	290-0943-00	B010100	B013921	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A14C904	290-0943-02	B013922		CAP,FXD,ELCTLT:47UF,20%,25V (2430 ONLY)	55680	UVX1E470MAA1TD
A14C904	290-0943-00	B010100	B010139	CAP,FXD,ELCTLT:47UF,+50-20%,25V	55680	ULB1E470TAAANA
A14C904	290-0943-02	B010140		CAP,FXD,ELCTLT:47UF,20%,25V (2430M ONLY)	55680	UVX1E470MAA1TD
A14C905	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A14C906	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A14CR901	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR902	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR903	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR904	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR907	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR908	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR909	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR911	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR912	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR913	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR914	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR916	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR917	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR918	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR919	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR921	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR922	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR923	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR924	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR927	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR928	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR929	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR932	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR933	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR934	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR937	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR938	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR939	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR942	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR943	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR944	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR947	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR948	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR949	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR952	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR953	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR954	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR957	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR958	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR959	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A14CR962	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR963	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR964	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR967	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR968	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR969	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14DS901	150-1109-00			LT EMITTING DIO:GREEN,30MA	50434	QLMP-0549
A14DS902	150-1109-00			LT EMITTING DIO:GREEN,30MA	50434	QLMP-0549
A14DS903	150-1109-00			LT EMITTING DIO:GREEN,30MA	50434	QLMP-0549
A14DS904	150-1109-00			LT EMITTING DIO:GREEN,30MA	50434	QLMP-0549
A14DS906	150-1109-00			LT EMITTING DIO:GREEN,30MA	50434	QLMP-0549
A14R901	311-2181-00			RES,VAR,NONWW:LINEAR,5K OHM,30%,0.25W	32997	91Z2D-Z45-EA0020
A14R902	311-2181-00			RES,VAR,NONWW:LINEAR,5K OHM,30%,0.25W	32997	91Z2D-Z45-EA0020
A14R903	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A14R904	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A14R913	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A14R914	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A14R916	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A14R917	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A14R918	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A14R919	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A14R922	315-0151-00	B010100	B011236	RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A14R922	315-0101-00	B011237		RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A14R923	315-0151-00	B010100	B011236	RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A14R923	315-0101-00	B011237		RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A14R924	315-0151-00	B010100	B011236	RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A14R924	315-0101-00	B011237		RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A14R927	315-0151-00	B010100	B011236	RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A14R927	315-0101-00	B011237		RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A14R928	315-0151-00	B010100	B011236	RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A14R928	315-0101-00	B011237		RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A14R930	315-0151-00			RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A14R933	315-0151-00			RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A14R934	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A14R935	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A14R936	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A14R937	315-0151-00			RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A14S901	263-0099-00			SW-VAR RES ASSY:	80009	263-0099-00
A14S902	263-0099-00			SW-VAR RES ASSY:	80009	263-0099-00
A14S903	263-0099-00			SW-VAR RES ASSY:	80009	263-0099-00
A14S904	263-0099-00			SW-VAR RES ASSY:	80009	263-0099-00
A14S907	260-2088-00			SWITCH,PUSH:1 BTN,1 POLE,TRIGGER	59821	2LL199NB021068
A14S908	260-2088-00			SWITCH,PUSH:1 BTN,1 POLE,TRIGGER	59821	2LL199NB021068
A14S909	260-2088-00			SWITCH,PUSH:1 BTN,1 POLE,TRIGGER	59821	2LL199NB021068
A14S911	260-2088-00			SWITCH,PUSH:1 BTN,1 POLE,TRIGGER	59821	2LL199NB021068
A14S912	260-2088-00			SWITCH,PUSH:1 BTN,1 POLE,TRIGGER	59821	2LL199NB021068
A14S913	260-2088-00			SWITCH,PUSH:1 BTN,1 POLE,TRIGGER	59821	2LL199NB021068
A14S914	260-2088-00			SWITCH,PUSH:1 BTN,1 POLE,TRIGGER	59821	2LL199NB021068
A14S916	260-2088-00			SWITCH,PUSH:1 BTN,1 POLE,TRIGGER	59821	2LL199NB021068
A14S917	260-2088-00			SWITCH,PUSH:1 BTN,1 POLE,TRIGGER	59821	2LL199NB021068
A14S918	260-2088-00			SWITCH,PUSH:1 BTN,1 POLE,TRIGGER	59821	2LL199NB021068
A14S919	260-2088-00			SWITCH,PUSH:1 BTN,1 POLE,TRIGGER	59821	2LL199NB021068
A14S921	260-2088-00			SWITCH,PUSH:1 BTN,1 POLE,TRIGGER	59821	2LL199NB021068
A14S922	260-2088-00			SWITCH,PUSH:1 BTN,1 POLE,TRIGGER	59821	2LL199NB021068
A14S923	260-2088-00			SWITCH,PUSH:1 BTN,1 POLE,TRIGGER	59821	2LL199NB021068
A14S924	260-2088-00			SWITCH,PUSH:1 BTN,1 POLE,TRIGGER	59821	2LL199NB021068
A14S927	260-2088-00			SWITCH,PUSH:1 BTN,1 POLE,TRIGGER	59821	2LL199NB021068
A14S928	260-2088-00			SWITCH,PUSH:1 BTN,1 POLE,TRIGGER	59821	2LL199NB021068

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A14S929	260-2088-00			SWITCH,PUSH:1 BTN,1 POLE,TRIGGER	59821	2LL199NB021068
A14S932	260-2088-00			SWITCH,PUSH:1 BTN,1 POLE,TRIGGER	59821	2LL199NB021068
A14S933	260-2088-00			SWITCH,PUSH:1 BTN,1 POLE,TRIGGER	59821	2LL199NB021068
A14S934	260-2224-00			SWITCH,ROTARY:GRAY CODE,OUTPUT	80009	260-2224-00
A14S942	260-2088-00			SWITCH,PUSH:1 BTN,1 POLE,TRIGGER	59821	2LL199NB021068
A14S943	260-2088-00			SWITCH,PUSH:1 BTN,1 POLE,TRIGGER	59821	2LL199NB021068
A14S944	260-2224-00			SWITCH,ROTARY:GRAY CODE,OUTPUT	80009	260-2224-00
A14S952	260-2088-00			SWITCH,PUSH:1 BTN,1 POLE,TRIGGER	59821	2LL199NB021068
A14S953	260-2088-00			SWITCH,PUSH:1 BTN,1 POLE,TRIGGER	59821	2LL199NB021068
A14S954	260-2224-00			SWITCH,ROTARY:GRAY CODE,OUTPUT	80009	260-2224-00
A14S962	260-2088-00			SWITCH,PUSH:1 BTN,1 POLE,TRIGGER	59821	2LL199NB021068
A14S963	260-2088-00			SWITCH,PUSH:1 BTN,1 POLE,TRIGGER	59821	2LL199NB021068
A14S964	260-2088-00			SWITCH,PUSH:1 BTN,1 POLE,TRIGGER	59821	2LL199NB021068
A14S967	260-2088-00			SWITCH,PUSH:1 BTN,1 POLE,TRIGGER	59821	2LL199NB021068
A14S968	260-2088-00			SWITCH,PUSH:1 BTN,1 POLE,TRIGGER	59821	2LL199NB021068
A14S969	260-2088-00			SWITCH,PUSH:1 BTN,1 POLE,TRIGGER	59821	2LL199NB021068
A14U902	156-0513-03			MICROCKT,LINEAR:CMOS,8 CHAN ANALOG MUX	04713	MC14051BCL
A14U903	156-0469-02			MICROCKT,DGTL:3/8 LINE DCDR,SCRN	01295	SN74LS138NP3
A14U904	156-0625-01			MICROCKT,DGTL:8 BIT PRL LOAD SHIFT RGTR	27014	74C165NA+
A14W151	175-9022-00			CA ASSY,SP,ELEC:26,28 AWG,18.95 L	80009	175-9022-00

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A16	670-8169-00	B010100	B010321	CIRCUIT BD ASSY:LV PWR SPLY	80009	670-8169-00
A16	670-8169-01	B010322	B013139	CIRCUIT BD ASSY:LV POWER SUPPLY	80009	670-8169-01
A16	670-8169-02	B013140	B013150	CIRCUIT BD ASSY:LVPS,CIIL	80009	670-8169-02
A16	670-8169-03	B013151		CIRCUIT BD ASSY:LV PWR SPLY	80009	670-8169-03
A16C105	290-1022-00			CAP,FXD,ELCTLT:680UF,+50-10%,200V	00853	DCM681T200AL2PC
A16C128	290-0183-00			CAP,FXD,ELCTLT:1UF,10%,35V	05397	T3228105K035AS
A16C137	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A16C138	290-0183-00			CAP,FXD,ELCTLT:1UF,10%,35V	05397	T3228105K035AS
A16C144	281-0812-00			CAP,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A16C145	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A16C175	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A16C184	290-0183-00			CAP,FXD,ELCTLT:1UF,10%,35V	05397	T3228105K035AS
A16C185	281-0812-00			CAP,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A16C195	281-0812-00			CAP,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A16C197	281-0812-00			CAP,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A16C218	285-1192-00			CAP,FXD,PPR DI:0.0022 UF,20%,250VAC	TK0515	PME271Y510
A16C223	283-0078-00			CAP,FXD,CER DI:0.001UF,20%,500V	59660	0801 547X5F0102M
A16C225	285-1192-00			CAP,FXD,PPR DI:0.0022 UF,20%,250VAC	TK0515	PME271Y510
A16C227	281-0812-00			CAP,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A16C238	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A16C244	290-0798-00			CAP,FXD,ELCTLT:180UF,+100-10%,40V	56289	672D187H040DM5C
A16C260	290-0945-00			CAP,FXD,ELCTLT:840UF 10 + 100 %,12V	00853	301EN841U012B2
A16C305	290-1022-00			CAP,FXD,ELCTLT:680UF,+50-10%,200V	00853	DCM681T200AL2PC
A16C328	285-1254-00	B010100	B013139	CAP,FXD,PLASTIC:0.22UF,10%,400WVDC	56289	730P0167
A16C328	285-1384-00	B013140		CAP,FXD,PLASTIC:0.27UF,10%,440V	84411	TEK-265
A16C368	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A16C384	281-0812-00			CAP,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A16C405	285-1321-00	B010100	B013139	CAP,FXD,PLASTIC:0.1UF,10%,100V	14752	935D1B104K
A16C405	285-1383-00	B013140		CAP,FXD,PLASTIC:0.1UF,10%,100V	84411	TEK-291
A16C455	290-0877-00			CAP,FXD,ELCTLT:1200UF,+100-10%,6.3V	56289	672D371
A16C460	290-0800-00			CAP,FXD,ELCTLT:250UF,+100-10%,20V	56289	672D257H020DM5C
A16C461	290-0942-00			CAP,FXD,ELCTLT:100UF,+100-10%,25V	55680	UPA1E101MAH
A16C483	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A16C485	281-0812-00			CAP,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A16C487	290-0942-00			CAP,FXD,ELCTLT:100UF,+100-10%,25V	55680	UPA1E101MAH
A16C494	290-0942-00			CAP,FXD,ELCTLT:100UF,+100-10%,25V	55680	UPA1E101MAH
A16C525	285-1187-00			CAP,FXD,MTLZD:0.47 UF,10%,100 V	05292	PMT 3R .47K 100
A16C528	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A16C550	290-0942-00			CAP,FXD,ELCTLT:100UF,+100-10%,25V	55680	UPA1E101MAH
A16C553	290-0945-00			CAP,FXD,ELCTLT:840UF 10 + 100 %,12V	00853	301EN841U012B2
A16C575	281-0812-00	B010100	B010321	CAP,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A16C575	281-0773-00	B010322		CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A16C584	281-0812-00			CAP,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A16C585	290-0942-00			CAP,FXD,ELCTLT:100UF,+100-10%,25V	55680	UPA1E101MAH
A16C594	290-0942-00			CAP,FXD,ELCTLT:100UF,+100-10%,25V	55680	UPA1E101MAH
A16C595	290-0942-00			CAP,FXD,ELCTLT:100UF,+100-10%,25V	55680	UPA1E101MAH
A16C628	285-1245-00			CAP,FXD,PLASTIC:0.01UF,10%,400V	55112	171/.01/K/400/C
A16C650	290-0942-00			CAP,FXD,ELCTLT:100UF,+100-10%,25V	55680	UPA1E101MAH
A16C664	290-1045-00			CAP,FXD,ELCTLT:4.7UF,10%,35V	56289	173D475X9035W
A16C675	281-0812-00			CAP,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A16C683	281-0812-00			CAP,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A16C694	290-0942-00			CAP,FXD,ELCTLT:100UF,+100-10%,25V	55680	UPA1E101MAH
A16C706	285-1222-00			CAP,FXD,PLASTIC:0.068UF,20%,250V	55112	158/.068/M/250/H
A16C728	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A16C750	290-0798-00			CAP,FXD,ELCTLT:180UF,+100-10%,40V	56289	672D187H040DM5C
A16C756	290-0798-00			CAP,FXD,ELCTLT:180UF,+100-10%,40V	56289	672D187H040DM5C
A16C764	290-1045-00			CAP,FXD,ELCTLT:4.7UF,10%,35V	56289	173D475X9035W
A16C816	285-1222-00			CAP,FXD,PLASTIC:0.068UF,20%,250V	55112	158/.068/M/250/H

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A16C823	281-0812-00			CAP,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A16C829	290-0183-00			CAP,FXD,ELCTLT:1UF,10%,35V	05397	T3228105K035AS
A16C835	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A16C856	290-0800-00			CAP,FXD,ELCTLT:250UF,+100-10%,20V	56289	672D257H020DM5C
A16C873	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A16C890	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A16C900	290-0183-00			CAP,FXD,ELCTLT:1UF,10%,35V	05397	T3228105K035AS
A16C901	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A16C929	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A16C944	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A16C947	290-0942-00			CAP,FXD,ELCTLT:100UF,+100-10%,25V	55680	UPA1E101MAH
A16C956	290-0800-00			CAP,FXD,ELCTLT:250UF,+100-10%,20V	56289	672D257H020DM5C
A16CR239	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A16CR245	152-0333-00			SEMICOND DVC,DI:SW,SI,55V,200MA,DO-35	07263	FDH-6012
A16CR265	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A16CR266	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A16CR354	152-0794-00			SEMICOND DVC,DI:RECT,SI,10A,30V,TO-220	81483	95-4269
A16CR426	152-0808-00			SEMICOND DVC,DI:RECT,SI,400V,1.5 A,50 NS	01281	DSR3400X
A16CR450	152-0398-00			SEMICOND DVC,DI:RECT,SI,200V,1A	04713	SR3609RL
A16CR465	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A16CR466	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A16CR483	152-0066-00			SEMICOND DVC,DI:RECT,SI,400V,1A,DO-41	05828	GP10G-020
A16CR484	152-0066-00			SEMICOND DVC,DI:RECT,SI,400V,1A,DO-41	05828	GP10G-020
A16CR485	152-0066-00			SEMICOND DVC,DI:RECT,SI,400V,1A,DO-41	05828	GP10G-020
A16CR510	152-0750-00			SEMICOND DVC,DI:RECT BRDG,600V,3A,FAST RCVY	05828	RKBPC606-12
A16CR550	152-0398-00			SEMICOND DVC,DI:RECT,SI,200V,1A	04713	SR3609RL
A16CR551	152-0867-00			SEMICOND DVC,DI:DUAL RECT,SI,30V,8A,TO-220	80009	152-0867-00
A16CR575	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A16CR576	152-0066-00			SEMICOND DVC,DI:RECT,SI,400V,1A,DO-41	05828	GP10G-020
A16CR583	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A16CR586	152-0066-00			SEMICOND DVC,DI:RECT,SI,400V,1A,DO-41	05828	GP10G-020
A16CR588	152-0066-00			SEMICOND DVC,DI:RECT,SI,400V,1A,DO-41	05828	GP10G-020
A16CR630	152-0400-00			SEMICOND DVC,DI:RECT,SI,400V,1A	04713	SR1977K
A16CR631	152-0400-00			SEMICOND DVC,DI:RECT,SI,400V,1A	04713	SR1977K
A16CR650	152-0398-00			SEMICOND DVC,DI:RECT,SI,200V,1A	04713	SR3609RL
A16CR651	152-0398-00			SEMICOND DVC,DI:RECT,SI,200V,1A	04713	SR3609RL
A16CR683	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A16CR684	152-0066-00			SEMICOND DVC,DI:RECT,SI,400V,1A,DO-41	05828	GP10G-020
A16CR685	152-0066-00			SEMICOND DVC,DI:RECT,SI,400V,1A,DO-41	05828	GP10G-020
A16CR723	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A16CR724	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A16CR730	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A16CR750	152-0398-00			SEMICOND DVC,DI:RECT,SI,200V,1A	04713	SR3609RL
A16CR751	152-0398-00			SEMICOND DVC,DI:RECT,SI,200V,1A	04713	SR3609RL
A16CR765	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A16CR766	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A16CR796	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A16CR823	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A16CR824	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A16CR845	152-0867-00			SEMICOND DVC,DI:DUAL RECT,SI,30V,8A,TO-220	80009	152-0867-00
A16CR846	152-0794-00			SEMICOND DVC,DI:RECT,SI,10A,30V,TO-220	81483	95-4269
A16CR865	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A16CR866	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A16CR896	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A16CR930	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A16E609	119-0181-00			ARSR,ELEC SURGE:230,GAS FILLED	25088	B1-A230
A16E616	119-0181-00			ARSR,ELEC SURGE:230,GAS FILLED	25088	B1-A230
A16F269	159-0236-00			FUSE,WIRE LEAD:10A,125V,FAST	TK0946	SP5-10A

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A16F961	159-0235-00			FUSE,WIRE LEAD:0.75A,125V,FAST	80009	159-0235-00
A16J102	131-3147-00			CONN,RCPT,ELEC:HEADER,2 X 25,0.1 SPACING	53387	3596-6002
A16J166	131-0608-00	B010100	B010321	TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 10)	22526	48283-036
A16J166	131-0608-00	B010322		TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 9)	22526	48283-036
A16L256	108-1234-00			COIL,RF:FIXED,5UH	80009	108-1234-00
A16L556	108-1234-00			COIL,RF:FIXED,5UH	80009	108-1234-00
A16L557	108-1233-00			COIL,RF:FIXED,27UH,10%	02113	ORDER BY DESCR
A16L656	108-1233-00			COIL,RF:FIXED,27UH,10%	02113	ORDER BY DESCR
A16L709	108-1209-00			COIL,RF:FXD TOROIDAL,80UH MIN,3A DC	94617	ORDER BY DESCR
A16L715	108-1209-00			COIL,RF:FXD TOROIDAL,80UH MIN,3A DC	94617	ORDER BY DESCR
A16L756	108-1233-00			COIL,RF:FIXED,27UH,10%	02113	ORDER BY DESCR
A16L945	108-1233-00			COIL,RF:FIXED,27UH,10%	02113	ORDER BY DESCR
A16L950	108-1233-00			COIL,RF:FIXED,27UH,10%	02113	ORDER BY DESCR
A16P30	131-2427-00			TERM,QIK DISC.:CKT BD,BRASS	00779	62409-1
A16P60	131-2427-00			TERM,QIK DISC.:CKT BD,BRASS	00779	62409-1
A16P70	131-2427-00			TERM,QIK DISC.:CKT BD,BRASS	00779	62409-1
A16P80	131-2427-00			TERM,QIK DISC.:CKT BD,BRASS	00779	62409-1
A16Q148	151-0432-00			TRANSISTOR:NPN,SI,625MW,TO-92	04713	SPS8512
A16Q240	151-0301-00			TRANSISTOR:PNP,SI,TO-18	04713	ST898
A16Q279	151-0798-00			TRANSISTOR:PNP,SI,TO-220	S4091	2SB826 Q OR R
A16Q295	151-0341-00			TRANSISTOR:NPN,SI,TO-106	04713	SPS6919
A16Q365	151-0134-00			TRANSISTOR:PNP,SI,TO-39	04713	SM3195
A16Q421	151-1152-00			TRANSISTOR:MOSFE,N-CHANNEL,SI,TO-220	04713	IRF820
A16Q423	151-1152-00			TRANSISTOR:MOSFE,N-CHANNEL,SI,TO-220	04713	IRF820
A16Q465	151-0103-00			TRANSISTOR:NPN,SI,TO-5	80009	151-0103-00
A16Q479	151-0797-00			TRANSISTOR:NPN,SI,TO-220	S4091	2SD1062 Q OR R
A16Q521	151-1141-00			TRANSISTOR:FE,N-CHANNEL,SI,TO-220	04713	STP3000
A16Q665	151-0134-00			TRANSISTOR:PNP,SI,TO-39	04713	SM3195
A16Q721	151-1141-00			TRANSISTOR:FE,N-CHANNEL,SI,TO-220	04713	STP3000
A16Q779	151-0798-00			TRANSISTOR:PNP,SI,TO-220	S4091	2SB826 Q OR R
A16Q836	151-0103-00			TRANSISTOR:NPN,SI,TO-5	80009	151-0103-00
A16Q870	151-0103-00			TRANSISTOR:NPN,SI,TO-5	80009	151-0103-00
A16Q879	151-0797-00			TRANSISTOR:NPN,SI,TO-220	S4091	2SD1062 Q OR R
A16R117	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A16R128	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A16R129	321-0430-00			RES,FXD,FILM:294K OHM,1%,0.125W,TC=T0	07716	CEAD29402F
A16R137	321-0932-00			RES,FXD,FILM:2.5K OHM,1%,0.125W,TC=T0	24546	NA55D2501F
A16R144	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A16R145	321-0356-00			RES,FXD,FILM:49.9K OHM,1%,0.125W,TC=T0	19701	5033ED49K90F
A16R146	321-0420-00			RES,FXD,FILM:232K OHM,1%,0.125W,TC=T0	07716	CEAD23202F
A16R164	321-0289-07			RES,FXD,FILM:10.0K OHM,0.1%,0.125W,TC=T9	19701	5033RE10K00B
A16R165	321-0816-07			RES,FXD,FILM:5K OHM,0.1%,0.125W,TC=T9	19701	5033RE5K000B
A16R166	321-0242-00			RES,FXD,FILM:3.24K OHM,1%,0.125W,TC=T0	19701	5043ED3K240F
A16R167	315-0474-00			RES,FXD,FILM:470K OHM,5%,0.25W	19701	5043CX470K0J92U
A16R185	315-0753-00			RES,FXD,FILM:75K OHM,5%,0.25W	57668	NTR25J-E75K0
A16R186	321-0335-00			RES,FXD,FILM:30.1K OHM,1%,0.125W,TC=T0	57668	RB14FXE30K1
A16R187	321-0337-00			RES,FXD,FILM:31.6K OHM,1%,0.125W,TC=T0	07716	CEAD31601F
A16R195	315-0474-00			RES,FXD,FILM:470K OHM,5%,0.25W	19701	5043CX470K0J92U
A16R217	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A16R223	305-0104-00			RES,FXD,CMPSN:100K OHM,5%,2W	01121	HB1045
A16R226	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A16R227	321-0193-00			RES,FXD,FILM:1K OHM,1%,0.125W,TC=T0	19701	5033ED1K00F
A16R228	321-0335-00			RES,FXD,FILM:30.1K OHM,1%,0.125W,TC=T0	57668	RB14FXE30K1
A16R238	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A16R244	315-0753-00			RES,FXD,FILM:75K OHM,5%,0.25W	57668	NTR25J-E75K0
A16R245	321-0932-00			RES,FXD,FILM:2.5K OHM,1%,0.125W,TC=T0	24546	NA55D2501F

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A16R265	321-0932-00			RES,FXD,FILM:2.5K OHM,1%,0.125W,TC=T0	24546	NA55D2501F
A16R275	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A16R276	321-0143-00			RES,FXD,FILM:301 OHM,1%,0.125W,TC=T0	07716	CEAD301R0F
A16R277	321-0420-00			RES,FXD,FILM:232K OHM,1%,0.125W,TC=T0	07716	CEAD23202F
A16R278	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25W	19701	5043CX10RR00J
A16R285	321-0356-00			RES,FXD,FILM:49.9K OHM,1%,0.125W,TC=T0	19701	5033ED49K90F
A16R293	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A16R295	321-0932-00			RES,FXD,FILM:2.5K OHM,1%,0.125W,TC=T0	24546	NA55D2501F
A16R296	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A16R323	321-0932-00			RES,FXD,FILM:2.5K OHM,1%,0.125W,TC=T0	24546	NA55D2501F
A16R324	321-0143-00			RES,FXD,FILM:301 OHM,1%,0.125W,TC=T0	07716	CEAD301R0F
A16R325	323-0436-00			RES,FXD,FILM:340K OHM,1%,0.5W,TC=T0	91637	MFF1226G34002F
A16R368	321-0210-00			RES,FXD,FILM:1.50K OHM,1%,0.125W,TC=T0	19701	5033ED1K50F
A16R369	321-0184-00			RES,FXD,FILM:806 OHM,1%,0.125W,TC=T0	19701	5033ED806R0F
A16R374	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25W	19701	5043CX10RR00J
A16R376	308-0839-00			RES,FXD,WW:0.1 OHM,5%,1.0W	75042	BW-20-R1000J
A16R388	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A16R394	321-0337-00			RES,FXD,FILM:31.6K OHM,1%,0.125W,TC=T0	07716	CEAD31601F
A16R395	321-0932-00			RES,FXD,FILM:2.5K OHM,1%,0.125W,TC=T0	24546	NA55D2501F
A16R396	321-0337-00			RES,FXD,FILM:31.6K OHM,1%,0.125W,TC=T0	07716	CEAD31601F
A16R400	315-0474-00			RES,FXD,FILM:470K OHM,5%,0.25W	19701	5043CX470K0J92U
A16R405	308-0703-00			RES,FXD,WW:1.8 OHM,5%,2W	75042	BWH 1.8 OHM 5%
A16R410	315-0474-00			RES,FXD,FILM:470K OHM,5%,0.25W	19701	5043CX470K0J92U
A16R428	305-0221-00			RES,FXD,CMPSN:220 OHM,5%,2W	01121	HB2215
A16R429	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A16R434	321-0242-00			RES,FXD,FILM:3.24K OHM,1%,0.125W,TC=T0	19701	5043ED3K240F
A16R435	321-0242-00			RES,FXD,FILM:3.24K OHM,1%,0.125W,TC=T0	19701	5043ED3K240F
A16R436	321-0385-00			RES,FXD,FILM:100K OHM,1%,0.125W,TC=T0	19701	5033ED100K0F
A16R465	321-0184-00			RES,FXD,FILM:806 OHM,1%,0.125W,TC=T0	19701	5033ED806R0F
A16R466	321-0242-00			RES,FXD,FILM:3.24K OHM,1%,0.125W,TC=T0	19701	5043ED3K240F
A16R473	308-0839-00			RES,FXD,WW:0.1 OHM,5%,1.0W	75042	BW-20-R1000J
A16R474	321-0143-00			RES,FXD,FILM:301 OHM,1%,0.125W,TC=T0	07716	CEAD301R0F
A16R475	321-0335-00			RES,FXD,FILM:30.1K OHM,1%,0.125W,TC=T0	57668	RB14FXE30K1
A16R476	321-0193-00			RES,FXD,FILM:1K OHM,1%,0.125W,TC=T0	19701	5033ED1K00F
A16R477	321-0385-00			RES,FXD,FILM:100K OHM,1%,0.125W,TC=T0	19701	5033ED100K0F
A16R478	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25W	19701	5043CX10RR00J
A16R483	321-0106-00			RES,FXD,FILM:124 OHM 1%,0.125W,TC=T0	07716	CEAD124R0F
A16R505	321-0385-00			RES,FXD,FILM:100K OHM,1%,0.125W,TC=T0	19701	5033ED100K0F
A16R516	321-0356-00			RES,FXD,FILM:49.9K OHM,1%,0.125W,TC=T0	19701	5033ED49K90F
A16R518	321-0356-00			RES,FXD,FILM:49.9K OHM,1%,0.125W,TC=T0	19701	5033ED49K90F
A16R565	321-0816-00			RES,FXD,FILM:5K OHM,1%,0.125W,TC=T0	24546	NA55D5001F
A16R566	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25W	19701	5043CX10RR00J
A16R575	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A16R576	321-0816-00			RES,FXD,FILM:5K OHM,1%,0.125W,TC=T0	24546	NA55D5001F
A16R578	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25W	19701	5043CX10RR00J
A16R624	321-0143-00			RES,FXD,FILM:301 OHM,1%,0.125W,TC=T0	07716	CEAD301R0F
A16R627	306-0154-00			RES,FXD,CMPSN:150K OHM,10%,2W	01121	HB1541
A16R640	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A16R675	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A16R676	321-0816-00			RES,FXD,FILM:5K OHM,1%,0.125W,TC=T0	24546	NA55D5001F
A16R684	321-0193-00			RES,FXD,FILM:1K OHM,1%,0.125W,TC=T0	19701	5033ED1K00F
A16R686	321-0306-00			RES,FXD,FILM:15.0K OHM,1%,0.125W,TC=T0	19701	5033ED15J00F
A16R688	321-0280-00			RES,FXD,FILM:8.06K OHM,1%,0.125W,TC=T0	19701	5033ED8K060F
A16R713	301-0680-00			RES,FXD,FILM:68 OHM,5%,0.5W	19701	5053CX68R00J
A16R723	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A16R724	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A16R727	308-0843-00			RES,FXD,WW:0.2 OHM,5%,1/0W	91637	RS1A-90-R2J
A16R728	321-0184-00			RES,FXD,FILM:806 OHM,1%,0.125W,TC=T0	19701	5033ED806R0F

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A16R758	308-0223-00			RES,FXD,WW:35 OHM,5%,3W	00213	1240S-35-5
A16R760	308-0555-00			RES,FXD,WW:5 OHM,5%,3W	00213	1200S-5.0-5
A16R765	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25W	19701	5043CX10RR00J
A16R769	321-0932-00			RES,FXD,FILM:2.5K OHM,1%,0.125W,TC=T0	24546	NA55D2501F
A16R773	308-0839-00			RES,FXD,WW:0.1 OHM,5%,1.0W	75042	BW-20-R1000J
A16R774	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A16R775	321-0269-00			RES,FXD,FILM:6.19K OHM,1%,0.125W,TC=T0	07716	CEAD61900F
A16R776	321-0143-00			RES,FXD,FILM:301 OHM,1%,0.125W,TC=T0	07716	CEAD301R0F
A16R777	321-0385-00			RES,FXD,FILM:100K OHM,1%,0.125W,TC=T0	19701	5033ED100K0F
A16R794	321-0306-00			RES,FXD,FILM:15.0K OHM,1%,0.125W,TC=T0	19701	5033ED15J00F
A16R795	321-0280-00			RES,FXD,FILM:8.06K OHM,1%,0.125W,TC=T0	19701	5033ED8K060F
A16R796	321-0816-00			RES,FXD,FILM:5K OHM,1%,0.125W,TC=T0	24546	NA55D5001F
A16R797	321-0816-00			RES,FXD,FILM:5K OHM,1%,0.125W,TC=T0	24546	NA55D5001F
A16R808	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A16R809	301-0300-00			RES,FXD,FILM:30 OHM,5%,0.5W	19701	5053CX30R00J
A16R815	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A16R822	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A16R823	321-0816-00			RES,FXD,FILM:5K OHM,1%,0.125W,TC=T0	24546	NA55D5001F
A16R824	321-0193-00			RES,FXD,FILM:1K OHM,1%,0.125W,TC=T0	19701	5033ED1K00F
A16R834	321-0143-00			RES,FXD,FILM:301 OHM,1%,0.125W,TC=T0	07716	CEAD301R0F
A16R835	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A16R836	321-0184-00			RES,FXD,FILM:806 OHM,1%,0.125W,TC=T0	19701	5033ED806R0F
A16R845	321-0242-00			RES,FXD,FILM:3.24K OHM,1%,0.125W,TC=T0	19701	5043ED3K240F
A16R847	321-0210-00			RES,FXD,FILM:1.50K OHM,1%,0.125W,TC=T0	19701	5033ED1K50F
A16R864	321-0932-00			RES,FXD,FILM:2.5K OHM,1%,0.125W,TC=T0	24546	NA55D2501F
A16R865	321-0816-00			RES,FXD,FILM:5K OHM,1%,0.125W,TC=T0	24546	NA55D5001F
A16R866	321-0816-00			RES,FXD,FILM:5K OHM,1%,0.125W,TC=T0	24546	NA55D5001F
A16R872	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A16R873	308-0839-00			RES,FXD,WW:0.1 OHM,5%,1.0W	75042	BW-20-R1000J
A16R874	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A16R875	321-0269-00			RES,FXD,FILM:6.19K OHM,1%,0.125W,TC=T0	07716	CEAD61900F
A16R876	321-0143-00			RES,FXD,FILM:301 OHM,1%,0.125W,TC=T0	07716	CEAD301R0F
A16R877	321-0356-00			RES,FXD,FILM:49.9K OHM,1%,0.125W,TC=T0	19701	5033ED49K90F
A16R900	321-0356-00			RES,FXD,FILM:49.9K OHM,1%,0.125W,TC=T0	19701	5033ED49K90F
A16R901	321-0184-00			RES,FXD,FILM:806 OHM,1%,0.125W,TC=T0	19701	5033ED806R0F
A16R903	321-0193-00			RES,FXD,FILM:1K OHM,1%,0.125W,TC=T0	19701	5033ED1K00F
A16R923	321-0816-00			RES,FXD,FILM:5K OHM,1%,0.125W,TC=T0	24546	NA55D5001F
A16R924	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A16R930	321-0193-00			RES,FXD,FILM:1K OHM,1%,0.125W,TC=T0	19701	5033ED1K00F
A16R934	315-0474-00			RES,FXD,FILM:470K OHM,5%,0.25W	19701	5043CX470K0J92U
A16R935	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A16R936	321-0242-00			RES,FXD,FILM:3.24K OHM,1%,0.125W,TC=T0	19701	5043ED3K240F
A16R975	321-0932-00			RES,FXD,FILM:2.5K OHM,1%,0.125W,TC=T0	24546	NA55D2501F
A16RT717	307-0157-00			RES,THERMAL:5 OHM,10%,DISC	15454	5DA5R0K270SSSIL
A16RT805	307-0157-00			RES,THERMAL:5 OHM,10%,DISC	15454	5DA5R0K270SSSIL
A16S1020	260-0724-00			SWITCH,THRMSTC:NC,OPEN 83.3,CL 66.7,10A	93410	430-367
A16T117	120-1560-00			TRANSFORMER,RF:HIGH FREQUENCY COMM MODE	02113	ORDER BY DESCR
A16T335	120-1561-00			TRANSFORMER,RF:POT CORE	02113	F5142-A
A16T415	120-1401-00			XFMR,TRIGGER:LINE,1:1 TURNS RATIO	54937	DMI 500-2044
A16T620	120-1555-00			TRANSFORMER,RF:DRIVER HIGH FREQ,GATE D	80009	120-1555-00
A16T639	120-1550-00			XFMR,PWR,STPDN:HIGH FREQUENCY	TK2038	ORDER BY DESCR
A16U155	156-0885-00	B010100	B011251	CPLR,OPTOELECTR:LED,5KV ISOLATION	04713	SOC 123A
A16U155	156-0885-05	B011252		CPLR,OPTOELECTR:LED,5KV,ISOLATION	09019	H11AX1139R
A16U170	156-0853-00			MICROCKT,LINEAR:OPNL AMPL,DUAL	04713	LM358N
A16U180	156-2186-00			MICROCKT,LINEAR:VOLT REF,10V,0.1%	27014	LM368H-10
A16U189	156-0853-00			MICROCKT,LINEAR:OPNL AMPL,DUAL	04713	LM358N
A16U233	156-2024-00			MICROCKT,LINEAR:PULSE WIDTH MOD CONTROLLER	12969	UC3525AN
A16U265	156-0885-00	B010100	B011251	CPLR,OPTOELECTR:LED,5KV ISOLATION	04713	SOC 123A

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A16U265	156-0885-05	B011252		CPLR,OPTOELECTR:LED,5KV,ISOLATION	09019	H11AX1139R
A16U270	156-0853-00			MICROCKT,LINEAR:OPNL AMPL,DUAL	04713	LM358N
A16U395	156-1225-00			MICROCKT,LINEAR:DUAL COMPARATOR	01295	LM393P
A16U470	156-0853-00			MICROCKT,LINEAR:OPNL AMPL,DUAL	04713	LM358N
A16U570	156-0853-00			MICROCKT,LINEAR:OPNL AMPL,DUAL	04713	LM358N
A16U579	156-1161-00			MICROCKT,LINEAR:VOLTAGE REGULATOR,POS,ADJ	12969	UC317T
A16U679	156-1451-00			MICROCKT,LINEAR:3-TERM NEG VOLTAGE RGLTR	27014	LM337T
A16U770	156-0853-00			MICROCKT,LINEAR:OPNL AMPL,DUAL	04713	LM358N
A16U829	156-0366-02			MICROCKT,DGTL:CMOS,DUAL D FLIP-FLOP,SCRN	02735	CD4013BFX
A16U834	156-1225-00			MICROCKT,LINEAR:DUAL COMPARATOR	01295	LM393P
A16U840	156-0411-00			MICROCKT,LINEAR:SGL SPLY COMPARATOR	04713	LM339N
A16U870	156-0853-00			MICROCKT,LINEAR:OPNL AMPL,DUAL	04713	LM358N
A16U900	156-0854-00			MICROCKT,LINEAR:OPNL AMPL	27014	LM308AN
A16VR144	152-0168-00			SEMICOND DVC,DI:ZEN,SI,12V,5%,0.4W,DO-763B	14552	TD331689
A16VR380	152-0195-00			SEMICOND DVC,DI:ZEN,SI,5.1V,5%,0.4W,DO-7	04713	SZ11755RL
A16VR870	152-0168-00			SEMICOND DVC,DI:ZEN,SI,12V,5%,0.4W,DO-763B	14552	TD331689
A16VR929	152-0168-00			SEMICOND DVC,DI:ZEN,SI,12V,5%,0.4W,DO-763B	14552	TD331689
A16W280	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A16W310	196-2827-00			LEAD,ELECTRICAL:18 AWG,2.75 L,3-4	80009	196-2827-00
A16W315	196-2827-00			LEAD,ELECTRICAL:18 AWG,2.75 L,3-4	80009	196-2827-00
A16W360	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A16W368	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A16W460	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A16W462	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A16W467	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A16W566	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A16W627	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A16W662	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A16W664	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A16W762	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A16W862	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A16W865	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A16W868	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A17	670-8166-00	B010100	B010321	CIRCUIT BD ASSY:HV	80009	670-8166-00
A17	670-8166-01	B010322	B010699	CIRCUIT BD ASSY:HV	80009	670-8166-01
A17	670-8166-02	B010700	B013699	CIRCUIT BD ASSY:HV	80009	670-8166-02
A17	670-8166-04	B013700	B014160	CIRCUIT BD ASSY:HV	80009	670-8166-04
A17	670-9748-00	B014161		CIRCUIT BD ASSY:HV POWER SPLY (2430 ONLY)	80009	670-9748-00
A17	670-8166-02	B010100	B010130	CIRCUIT BD ASSY:HV	80009	670-8166-02
A17	670-8166-04	B010131	B014160	CIRCUIT BD ASSY:HV	80009	670-8166-04
A17	670-9748-00	B014161		CIRCUIT BD ASSY:HV POWER SPLY (2430M ONLY)	80009	670-9748-00
A17C109	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A17C133	281-0772-00			CAP,FXD,CER DI:4700PF,10%,100V	04222	MA201C472KAA
A17C139	283-0167-00			CAP,FXD,CER DI:0.1UF,10%,100V	04222	3430-100C-104K
A17C160	281-0865-00			CAP,FXD,CER DI:1000PF,5%,100V	04222	MA101A102JAA
A17C179	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A17C189	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A17C218	290-0766-00			CAP,FXD,ELCTLT:2.2UF,+50-10%,160VDC	54473	ECEA2CS2R2
A17C222	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A17C234	281-0762-00			CAP,FXD,CER DI:27PF,20%,100V	04222	MA101A270MAA
A17C239	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A17C260	283-0167-00			CAP,FXD,CER DI:0.1UF,10%,100V	04222	3430-100C-104K
A17C269	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A17C279	281-0766-00			CAP,FXD,CER DI:100PF,20%,200V	04222	MA106A101MAA
A17C288	283-0167-00			CAP,FXD,CER DI:0.1UF,10%,100V	04222	3430-100C-104K
A17C289	283-0187-00	B010100	B013699	CAP,FXD,CER DI:0.047UF,10%,400V	04222	SR308C473KAA
A17C289	283-0187-05	B013700		CAP,FXD,CER DI:0.047UF,10%,500V (2430 ONLY)	51642	W400500-X5R-473K
A17C289	283-0187-00	B010100	B010130	CAP,FXD,CER DI:0.047UF,10%,400V	04222	SR308C473KAA
A17C289	283-0187-05	B010131		CAP,FXD,CER DI:0.047UF,10%,500V (2430M ONLY)	51642	W400500-X5R-473K
A17C295	281-0798-00			CAP,FXD,CER DI:51PF,1%,100V	04222	MA101A510GAA
A17C317	290-0939-00			CAP,FXD,ELCTLT:10UF,+100-10%,100V	56289	672D106H100CG2C
A17C327	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A17C409	281-0814-00			CAP,FXD,CER DI:100 PF,10%,100V	04222	MA101A101KAA
A17C613	290-0973-00			CAP,FXD,ELCTLT:100UF,20%,25VDC	55680	ULB1E101MPA
A17C617	283-0339-00			CAP,FXD,CER DI:0.22UF,10%,50V	05397	C330C224K5R5CA
A17C618	283-0187-00	B010100	B013699	CAP,FXD,CER DI:0.047UF,10%,400V	04222	SR308C473KAA
A17C618	283-0187-05	B013700		CAP,FXD,CER DI:0.047UF,10%,500V (2430 ONLY)	51642	W400500-X5R-473K
A17C618	283-0187-00	B010100	B010130	CAP,FXD,CER DI:0.047UF,10%,400V	04222	SR308C473KAA
A17C618	283-0187-05	B010131		CAP,FXD,CER DI:0.047UF,10%,500V (2430M ONLY)	51642	W400500-X5R-473K
A17C628	281-0865-00			CAP,FXD,CER DI:1000PF,5%,100V	04222	MA101A102JAA
A17C629	283-0187-00	B010100	B013699	CAP,FXD,CER DI:0.047UF,10%,400V	04222	SR308C473KAA
A17C629	283-0187-05	B013700		CAP,FXD,CER DI:0.047UF,10%,500V (2430 ONLY)	51642	W400500-X5R-473K
A17C629	283-0187-00	B010100	B010130	CAP,FXD,CER DI:0.047UF,10%,400V	04222	SR308C473KAA
A17C629	283-0187-05	B010131		CAP,FXD,CER DI:0.047UF,10%,500V (2430M ONLY)	51642	W400500-X5R-473K
A17C638	283-0187-00	B010100	B013699	CAP,FXD,CER DI:0.047UF,10%,400V	04222	SR308C473KAA
A17C638	283-0187-05	B013700		CAP,FXD,CER DI:0.047UF,10%,500V (2430 ONLY)	51642	W400500-X5R-473K
A17C638	283-0187-00	B010100	B010130	CAP,FXD,CER DI:0.047UF,10%,400V	04222	SR308C473KAA
A17C638	283-0187-05	B010131		CAP,FXD,CER DI:0.047UF,10%,500V (2430M ONLY)	51642	W400500-X5R-473K
A17C640	281-0766-00			CAP,FXD,CER DI:100PF,20%,200V	04222	MA106A101MAA
A17C643	283-0187-00	B010100	B013699	CAP,FXD,CER DI:0.047UF,10%,400V	04222	SR308C473KAA
A17C643	283-0187-05	B013700		CAP,FXD,CER DI:0.047UF,10%,500V (2430 ONLY)	51642	W400500-X5R-473K
A17C643	283-0187-00	B010100	B010130	CAP,FXD,CER DI:0.047UF,10%,400V	04222	SR308C473KAA

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A17C643	283-0187-05	B010131		CAP,FXD,CER DI:0.047UF,10%,500V (2430M ONLY)	51642	W400500-X5R-473K
A17C688	283-0429-00			CAP,FXD,CER DI:270PF,20%,2000V	51406	DHR12-Z5U271M-2K
A17C689	283-0187-00	B010100	B013699	CAP,FXD,CER DI:0.047UF,10%,400V	04222	SR308C473KAA
A17C689	283-0187-05	B013700		CAP,FXD,CER DI:0.047UF,10%,500V (2430 ONLY)	51642	W400500-X5R-473K
A17C689	283-0187-00	B010100	B010130	CAP,FXD,CER DI:0.047UF,10%,400V	04222	SR308C473KAA
A17C689	283-0187-05	B010131		CAP,FXD,CER DI:0.047UF,10%,500V (2430M ONLY)	51642	W400500-X5R-473K
A17C690	283-0167-00			CAP,FXD,CER DI:0.1UF,10%,100V	04222	3430-100C-104K
A17C692	283-0187-00	B010100	B013699	CAP,FXD,CER DI:0.047UF,10%,400V	04222	SR308C473KAA
A17C692	283-0187-05	B013700		CAP,FXD,CER DI:0.047UF,10%,500V (2430 ONLY)	51642	W400500-X5R-473K
A17C692	283-0187-00	B010100	B010130	CAP,FXD,CER DI:0.047UF,10%,400V	04222	SR308C473KAA
A17C692	283-0187-05	B010131		CAP,FXD,CER DI:0.047UF,10%,500V (2430M ONLY)	51642	W400500-X5R-473K
A17C694	283-0167-00			CAP,FXD,CER DI:0.1UF,10%,100V	04222	3430-100C-104K
A17CR134	152-0574-00			SEMICOND DVC,DI:SW,SI,120V,0.15A,DO-35	12969	NDP566
A17CR315	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A17CR411	152-0400-00			SEMICOND DVC,DI:RECT,SI,400V,1A	04713	SR1977K
A17CR442	152-0061-00			SEMICOND DVC,DI:SW,SI,175V,0.1A,DO-35	07263	FDH2161
A17CR500	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A17CR541	152-0061-00			SEMICOND DVC,DI:SW,SI,175V,0.1A,DO-35	07263	FDH2161
A17CR565	152-0805-03			SEMICOND DVC,DI:HV MODULE,22KVDC OUTPUT	60211	VM341
A17CR610	152-0400-00			SEMICOND DVC,DI:RECT,SI,400V,1A	04713	SR1977K
A17CR611	152-0400-00			SEMICOND DVC,DI:RECT,SI,400V,1A	04713	SR1977K
A17CR643	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A17CR644	152-0061-00			SEMICOND DVC,DI:SW,SI,175V,0.1A,DO-35	07263	FDH2161
A17DS490	150-0030-00			LAMP,GLOW:60-90V MAX,0.7MA,A28-T,WIRE LEADS	58224	A2B-T
A17DS491	150-0030-00			LAMP,GLOW:60-90V MAX,0.7MA,A28-T,WIRE LEADS	58224	A2B-T
A17J162	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 2)	22526	48283-036
A17J172	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY OF 2)	22526	48283-029
A17J173	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY OF 2)	22526	48283-029
A17J174	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 9)	22526	48283-036
A17J176	131-0608-00	B010100	B010321	TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 10)	22526	48283-036
A17J176	131-0608-00	B010322		TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 9)	22526	48283-036
A17L605	108-0318-00			COIL,RF:FIXED,100UH	32159	81000M
A17Q145	151-0443-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS7950
A17Q152	151-0443-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS7950
A17Q215	151-0444-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS797
A17Q269	151-0443-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS7950
A17Q500	151-0443-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS7950
A17Q628	151-0816-00	B010322		TRANSISTOR:PNP,SI,TO-3P	TK1016	2SA1264R
A17Q640	151-0444-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS797
A17R100	311-2234-00			RES,VAR,NONWW:TRMR,5K OHM,20%,0.5W LINEAR	TK1450	GF06UT 5K
A17R119	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A17R122	321-0267-00			RES,FXD,FILM:5.90K OHM,1%,0.125W,TC=T0	19701	5033ED5K900F
A17R137	301-0752-00			RES,FXD,FILM:7.5K OHM,5%,0.5W	19701	5053CX7K500J
A17R145	321-0367-00	B010100	B010319	RES,FXD,FILM:64.9K OHM,1%,0.125W,TC=T0	07716	CEAD64901F
A17R145	321-0368-00	B010320		RES,FXD,FILM:66.5K OHM,1%,0.125W,TC=T0	07716	CEAD66501F
A17R146	321-1489-00	B010100	B010319	RES,FXD,FILM:1.23M,1%,0.125W,TC=T0	01121	CC1234FY
A17R160	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25W	57668	NTR25J-E 2K
A17R161	315-0224-00			RES,FXD,FILM:220K OHM,5%,0.25W	57668	NTR25J-E220K
A17R162	315-0272-00			RES,FXD,FILM:2.7K OHM,5%,0.25W	57668	NTR25J-E02K7

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A17R170	315-0272-00			RES,FXD,FILM:2.7K OHM,5%,0.25W	57668	NTR25J-E02K7
A17R178	315-0393-00			RES,FXD,FILM:39K OHM,5%,0.25W	57668	NTR25J-E39K0
A17R179	321-0693-00			RES,FXD,FILM:68.1K OHM,0.5%,0.125W,TC=T0	19701	5033RD6812DB2980
A17R200	311-2239-00			RES,VAR,NONWW:TRMR,100K OHM,20%,0.5W LINEAR	TK1450	GF06UT 100K
A17R209	321-0245-00			RES,FXD,FILM:3.48K OHM,1%,0.125W,TC=T0	19701	5033ED3K48F
A17R233	315-0560-00			RES,FXD,FILM:56 OHM,5%,0.25W	57668	NTR25J-E56E0
A17R245	321-0438-00			RES,FXD,FILM:357K OHM,1%,0.125W,TC=T0	07716	CEAD35702F
A17R246	321-0447-00			RES,FXD,FILM:442K OHM,1%,0.125W,TC=T0	24546	NA55D4423F
A17R247	321-0393-00			RES,FXD,FILM:121K OHM,1%,0.125W,TC=T0	19701	5043ED121K0F
A17R248	321-0407-00			RES,FXD,FILM:169K OHM,1%,0.125W,TC=T0	07716	CEAD16902F
A17R260	321-0393-00			RES,FXD,FILM:121K OHM,1%,0.125W,TC=T0	19701	5043ED121K0F
A17R261	321-0367-00			RES,FXD,FILM:64.9K OHM,1%,0.125W,TC=T0	07716	CEAD64901F
A17R262	321-0407-00	B010100	B010319	RES,FXD,FILM:169K OHM,1%,0.125W,TC=T0	07716	CEAD16902F
A17R262	321-0413-00	B010320		RES,FXD,FILM:196K OHM,1%,0.125W,TC=T0	07716	CEAD19602F
A17R263	321-0385-07	B010100	B010319	RES,FXD,FILM:100K OHM,0.1%,0.125W,TC=T9	19701	5033RE100K0B
A17R263	321-0963-07	B010320		RES,FXD,FILM:98.73K OHM,0.1%,0.125W,TC=T9	07716	CEA 98.73KOHM 1%
A17R277	321-0693-00			RES,FXD,FILM:68.1K OHM,0.5%,0.125W,TC=T0	19701	5033RD6812DB2980
A17R278	321-0481-07			RES,FXD,FILM:1M OHM,0.1%,0.125W,TC=T9	19701	5033RE1M000B
A17R279	321-0481-07			RES,FXD,FILM:1M OHM,0.1%,0.125W,TC=T9	19701	5033RE1M000B
A17R297	321-0245-00			RES,FXD,FILM:3.48K OHM,1%,0.125W,TC=T0	19701	5033ED3K48F
A17R300	311-2236-00			RES,VAR,NONWW:TRMR,20K OHM,20%,0.5W LINEAR	TK1450	GF06UT 20K
A17R305	311-2234-00			RES,VAR,NONWW:TRMR,5K OHM,20%,0.5W LINEAR	TK1450	GF06UT 5K
A17R315	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A17R393	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A17R395	321-0271-00			RES,FXD,FILM:6.49K OHM,1%,0.125W,TC=T0	07716	CEAD64900F
A17R400	311-2236-00			RES,VAR,NONWW:TRMR,20K OHM,20%,0.5W LINEAR	TK1450	GF06UT 20K
A17R442	315-0331-03			RES,FXD,CMPSN:330 OHM 5%,0.25W	01121	CB3315
A17R443	315-0162-00			RES,FXD,FILM:1.6K OHM,5%,0.25W	19701	5043CX1K600J
A17R500	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A17R543	315-0393-00			RES,FXD,FILM:39K OHM,5%,0.25W	57668	NTR25J-E39K0
A17R546	315-0201-00			RES,FXD,FILM:200 OHM,5%,0.25W	57668	NTR25J-E200E
A17R620	315-0220-00			RES,FXD,FILM:22 OHM,5%,0.25W	19701	5043CX22R00J
A17R642	321-0407-00			RES,FXD,FILM:169K OHM,1%,0.125W,TC=T0	07716	CEAD16902F
A17R643	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A17R644	315-0224-00			RES,FXD,FILM:220K OHM,5%,0.25W	57668	NTR25J-E220K
A17R645	321-0463-00			RES,FXD,FILM:649K OHM,1%,0.125W	19701	5033ED649K0F
A17R689	321-0438-00			RES,FXD,FILM:357K OHM,1%,0.125W,TC=T0	07716	CEAD35702F
A17R690	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A17R691	315-0100-00	B010100	B013135	RES,FXD,FILM:10 OHM,5%,0.25W	19701	5043CX10RR00J
A17R691	315-0102-00	B013136		RES,FXD,FILM:1K OHM,5%,0.25W (STANDARD ONLY)	57668	NTR25JE01K0
A17R691	315-0100-00	B010100	B010115	RES,FXD,FILM:10 OHM,5%,0.25W	19701	5043CX10RR00J
A17R691	315-0102-00	B010116		RES,FXD,FILM:1K OHM,5%,0.25W (2430M ONLY)	57668	NTR25JE01K0
A17R693	315-0100-00	B010100	B013135	RES,FXD,FILM:10 OHM,5%,0.25W	19701	5043CX10RR00J
A17R693	315-0102-00	B013136		RES,FXD,FILM:1K OHM,5%,0.25W (STANDARD ONLY)	57668	NTR25JE01K0
A17R693	315-0100-00	B010100	B010115	RES,FXD,FILM:10 OHM,5%,0.25W	19701	5043CX10RR00J
A17R693	315-0102-00	B010116		RES,FXD,FILM:1K OHM,5%,0.25W (2430M ONLY)	57668	NTR25JE01K0
A17T525	120-1548-00			TRANSFORMER,RF:HIGH VOLTAGE	80009	120-1548-00
A17U168	156-0158-07			MICROCKT,LINEAR:DUAL OPNL AMPL,SCREENED	01295	MC1458JG4
A17U227	155-0294-00			MICROCKT,LINEAR:Z-AXIS AMPL W/AUTO FOCUS	80009	155-0294-00
A17VR210	152-0285-00			SEMICOND DVC,DI:ZEN,SI,62V,5%,0.4W,DO-7	12954	1N980B
A17VR316	152-0243-00			SEMICOND DVC,DI:ZEN,SI,15V,5%,0.4W,DO-7	04713	SZ13203 (1N965B)
A17W175	175-9231-00	B010100	B010321	CA ASSY,SP,ELEC:5,22 AWG,6.0 L,RIBBON	80009	175-9231-00
A17W175	175-9231-01	B010322		CA ASSY,SP,ELEC:7,26 AWG,2.75 L,RIBBON	TK1544	ORDER BY DESCR
A17W176	175-9230-01			CA ASSY,SP,ELEC:10,26 AWG,11.0 L,RIBBON	80009	175-9230-01

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A18	670-8795-00	B010100	B010699	CIRCUIT BD ASSY:SCALE ILLUM	80009	670-8795-00
A18	670-8795-01	B010700	B014161	CIRCUIT BD ASSY:SCALE ILLUM	80009	670-8795-01
A18	670-7280-00	B014162		CIRCUIT BD ASSY:SCALE ILLUM (2430 ONLY)	80009	670-7280-00
A18	670-8795-01	B010100	B019999	CIRCUIT BD ASSY:SCALE ILLUM (2430M ONLY)	80009	670-8795-01
A18DS910	150-0057-01			LAMP,INCAND:5V,0.115A,WIRE LD,AGED & SEL	71744	7153 AS 15
A18DS911	150-0057-01			LAMP,INCAND:5V,0.115A,WIRE LD,AGED & SEL	71744	7153 AS 15
A18DS912	150-0057-01			LAMP,INCAND:5V,0.115A,WIRE LD,AGED & SEL	71744	7153 AS 15

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
B1000	119-1770-01			FAN,TUBEAXIAL:12V,1.72 W,42 CFM W/CONN	80009	119-1770-01
DS920	150-1064-00			LT EMITTING DIO:YELLOW,585NM,40 MA MAX	15513	SP840113
DS921	150-1064-00			LT EMITTING DIO:YELLOW,585NM,40 MA MAX	15513	SP840113
DS922	150-1064-00			LT EMITTING DIO:YELLOW,585NM,40 MA MAX	15513	SP840113
F1000	159-0014-00			FUSE,CARTRIDGE:3AG,5A,250V,0.8SEC	71400	MTH-CW-5
FL1000	119-1306-00			FILTER,RFI:6A,250V,50-400HZ	56289	6JX5431A
L1000	119-1478-01			COIL,TUBE DEFL:FXD,TRACE ROTATION	80009	119-1478-01
R1000	301-0474-00			RES,FXD,FILM:470K OHM,5%,0.5W	19701	5053CX470K0J
R1077	311-1845-00			RES,VAR,NONWW:PNL,5K OHM,0.5W	01121	W8355
R1088	311-1845-00			RES,VAR,NONWW:PNL,5K OHM,0.5W	01121	W8355
R1099	311-1845-00			RES,VAR,NONWW:PNL,5K OHM,0.5W	01121	W8355
R1121	311-2248-00			RES,VAR,NONWW:PNL,(2)10K OHM,20%,0.5W	12697	CM43462
S1000	260-1967-00			SWITCH,SLIDE:DPDT 5A/250V 10A/125V MKD	TK0935	4021.0512
S1350	260-2202-00			SWITCH,PUSH:DPDT,5A,250VAC	31918	N30 51870
S1666	260-2173-00			SW,PUSH BUTTON:MOMENTARY,5 BUTTON	61545	CP85-41313
U624	156-1414-02			MICROCKT,DGTL:OCTAL GPIB BUS XCVR,SCRN	27014	DS75160A N
U630	156-1444-01			MICROCKT,DGTL:NMOS,GPIB INTFC CONTROLLER	01295	TMS9914A (NL
U692	160-2554-00			MICROCKT,DGTL:16384 X 8 EPROM,PRGM	80009	160-2554-00
U720	156-2013-00			MICROCKT,DGTL:STTL,IEEE-488 XCVR	27014	DS75162AN
V1000	154-0850-01			CRT ASSEMBLY:FINISHED 2445	80009	154-0850-01

DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

Symbols

Graphic symbols and class designation letters are based on ANSI Standard Y32.2-1975.

Logic symbology is based on ANSI Y32.14-1973 in terms of positive logic. Logic symbols depict the logic function performed and may differ from the manufacturer's data.

The overline on a signal name indicates that the signal performs its intended function when it is in the low state.

Abbreviations are based on ANSI Y1.1-1972.

Other ANSI standards that are used in the preparation of diagrams by Tektronix, Inc. are:

Y14.15, 1966 Drafting Practices.
Y14.2, 1973 Line Conventions and Lettering.
Y10.5, 1968 Letter Symbols for Quantities Used in Electrical Science and Electrical Engineering.

American National Standard Institute
1430 Broadway
New York, New York 10018

Component Values

Electrical components shown on the diagrams are in the following units unless noted otherwise:

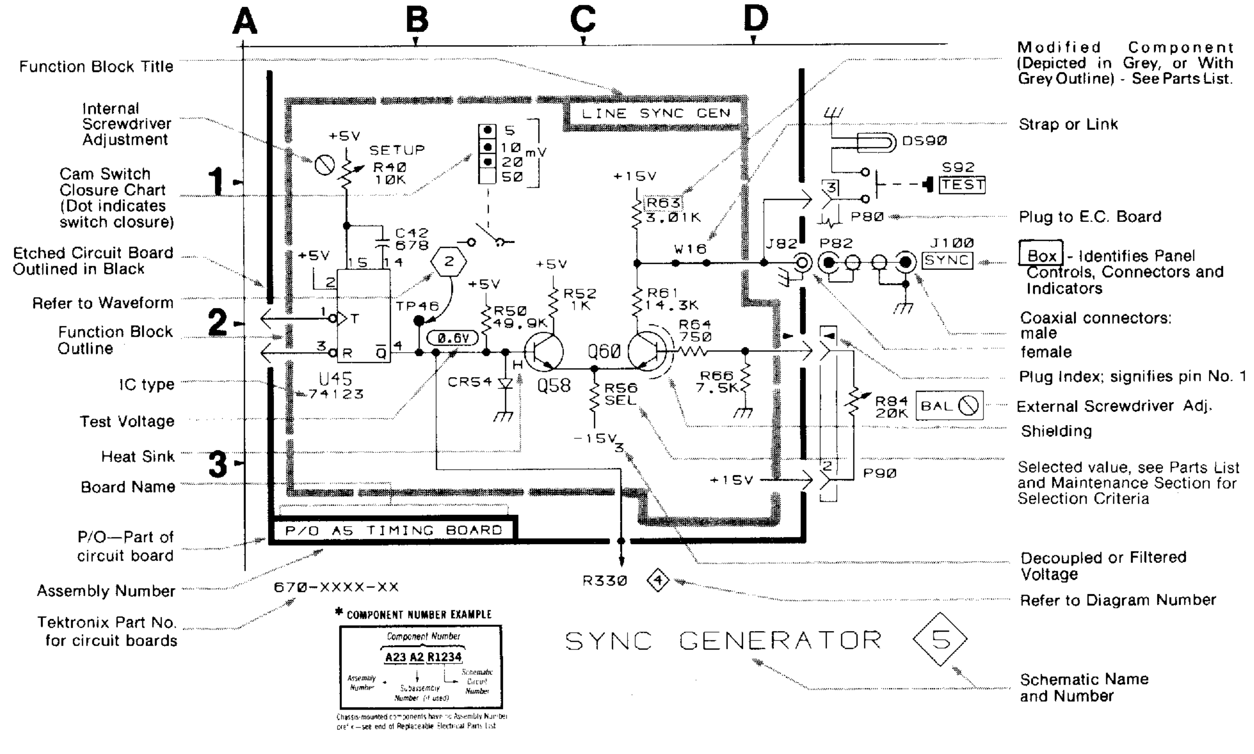
Capacitors = Values one or greater are in picofarads (pF). Values less than one are in microfarads (μF).
Resistors = Ohms (Ω).

The information and special symbols below may appear in this manual.

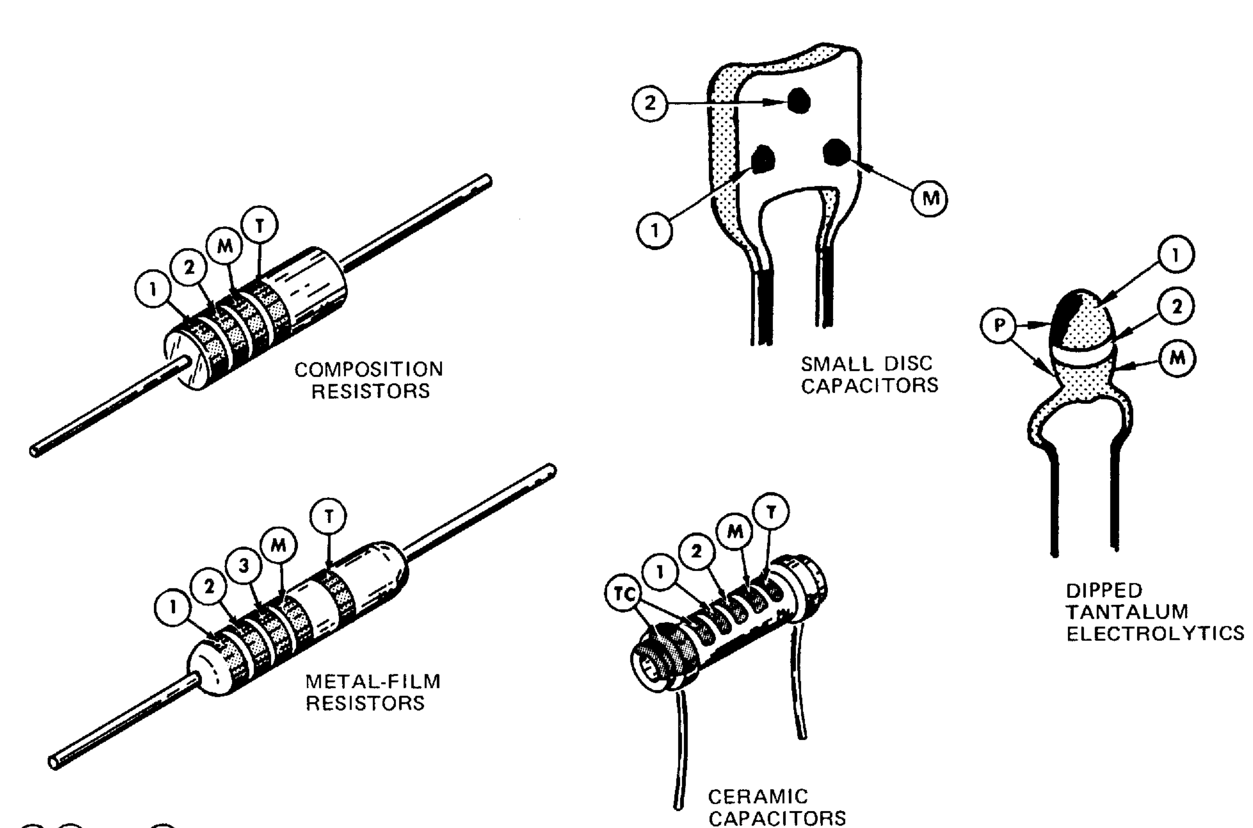
Assembly Numbers and Grid Coordinates

Each assembly in the instrument is assigned an assembly number (e.g., A20). The assembly number appears on the circuit board outline on the diagram, in the title for the circuit board component location illustration, and in the lookup table for the schematic diagram and corresponding component locator illustration. The Replaceable Electrical Parts list is arranged by assemblies in numerical sequence; the components are listed by component number *(see following illustration for constructing a component number).

The schematic diagram and circuit board component location illustration have grids. A lookup table with the grid coordinates is provided for ease of locating the component. Only the components illustrated on the facing diagram are listed in the lookup table. When more than one schematic diagram is used to illustrate the circuitry on a circuit board, the circuit board illustration may only appear opposite the first diagram on which it was illustrated; the lookup table will list the diagram number of other diagrams that the circuitry of the circuit board appears on.



COLOR CODE



(1)(2) and (3) — 1st, 2nd, and 3rd significant figures
(M) —multiplier
(T) —tolerance
(TC) —temperature coefficient
(P) —polarity and voltage rating
(T) and/or (TC) color code may not be present on some capacitors

COLOR	SIGNIFICANT FIGURES	RESISTORS		CAPACITORS			DIPPED TANTALUM VOLTAGE RATING
		MULTIPLIER	TOLERANCE	MULTIPLIER	TOLERANCE		
					over 10 pF	under 10 pF	
BLACK	0	1	---	1	±20%	±2 pF	4 VDC
BROWN	1	10	±1%	10	±1%	±0.1 pF	6 VDC
RED	2	10^2 or 100	±2%	10^2 or 100	±2%	---	10 VDC
ORANGE	3	10^3 or 1 K	±3%	10^3 or 1000	±3%	---	15 VDC
YELLOW	4	10^4 or 10 K	±4%	10^4 or 10,000	+100% −9%	---	20 VDC
GREEN	5	10^5 or 100 K	±½%	10^5 or 100,000	±5%	±0.5 pF	25 VDC
BLUE	6	10^6 or 1 M	±¼%	10^6 or 1,000,000	---	---	35 VDC
VIOLET	7	---	±1/10%	---	---	---	50 VDC
GRAY	8	---	---	10^{-2} or 0.01	+80% −20%	±0.25 pF	---
WHITE	9	---	---	10^{-1} or 0.1	±10%	±1 pF	3 VDC
GOLD	–	10^{-1} or 0.1	±5%	---	---	---	---
SILVER	–	10^{-2} or 0.01	±10%	---	---	---	---
NONE	–	---	±20%	---	±10%	±1 pF	---

(1861-20A) 2662-48

Figure 9-1. Color codes for resistors and capacitors.

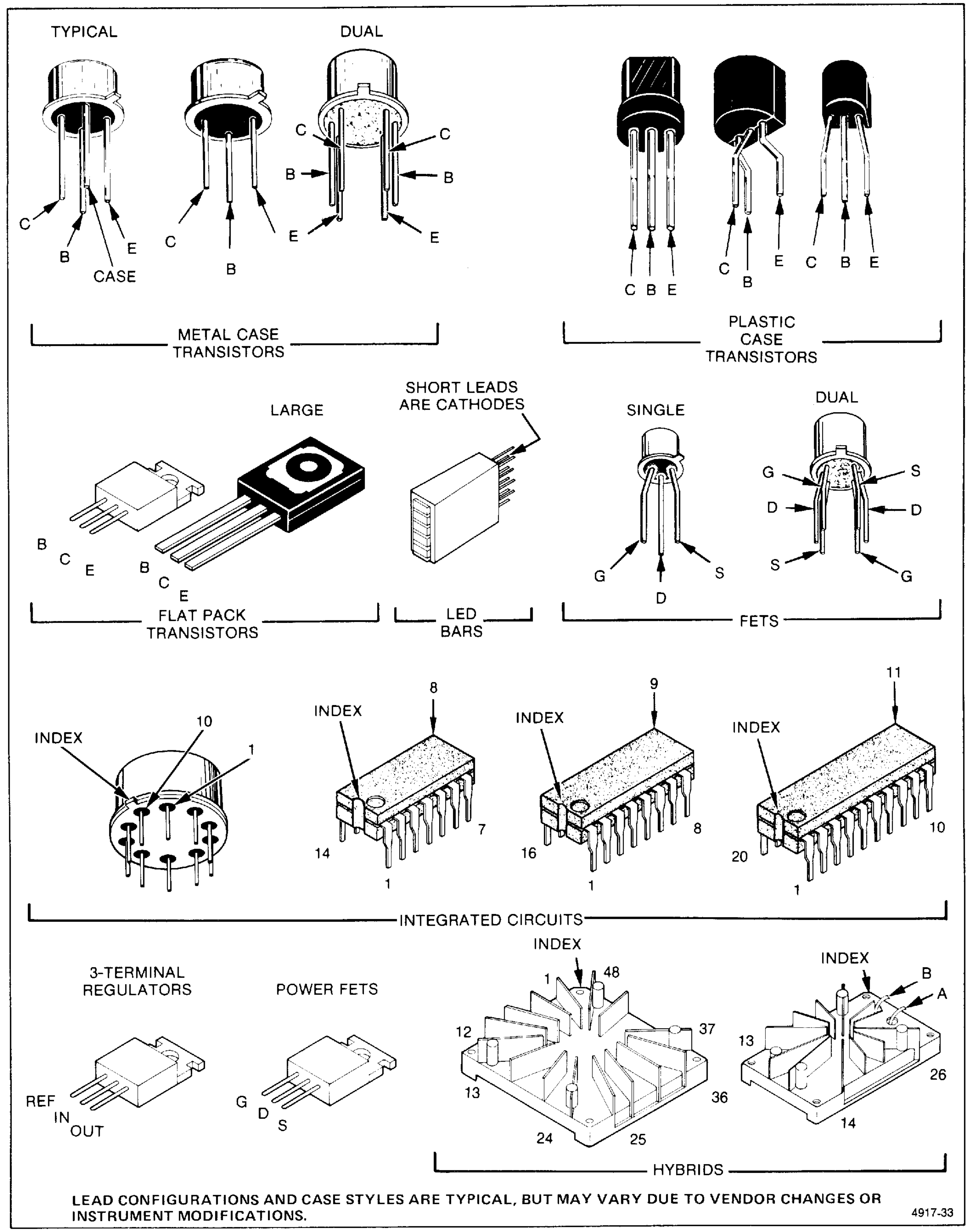


Figure 9-2. Semiconductor lead configurations.

To identify any component mounted on a circuit board and to locate that component in the appropriate schematic diagram

1. Locate the Circuit Board Illustration

a. Identify the particular circuit board that the component is located on by using the Circuit Board Location illustration (Figure 9-5) to determine the Assembly Number.

b. In the manual locate and pull out tabbed page whose title corresponds with the Assembly Number of the circuit board. Circuit board assembly numbers and board nomenclature are printed on the back side of the tabs (facing the rear of the manual).

2. Determine the Circuit Number

a. Compare the circuit board with its illustration and locate the desired component by area and shape on the illustration.

b. Scan the table adjacent to the Circuit Board Illustration and find the Circuit Number of the desired component.

c. Determine the Schematic Diagram Number in which the component is located.

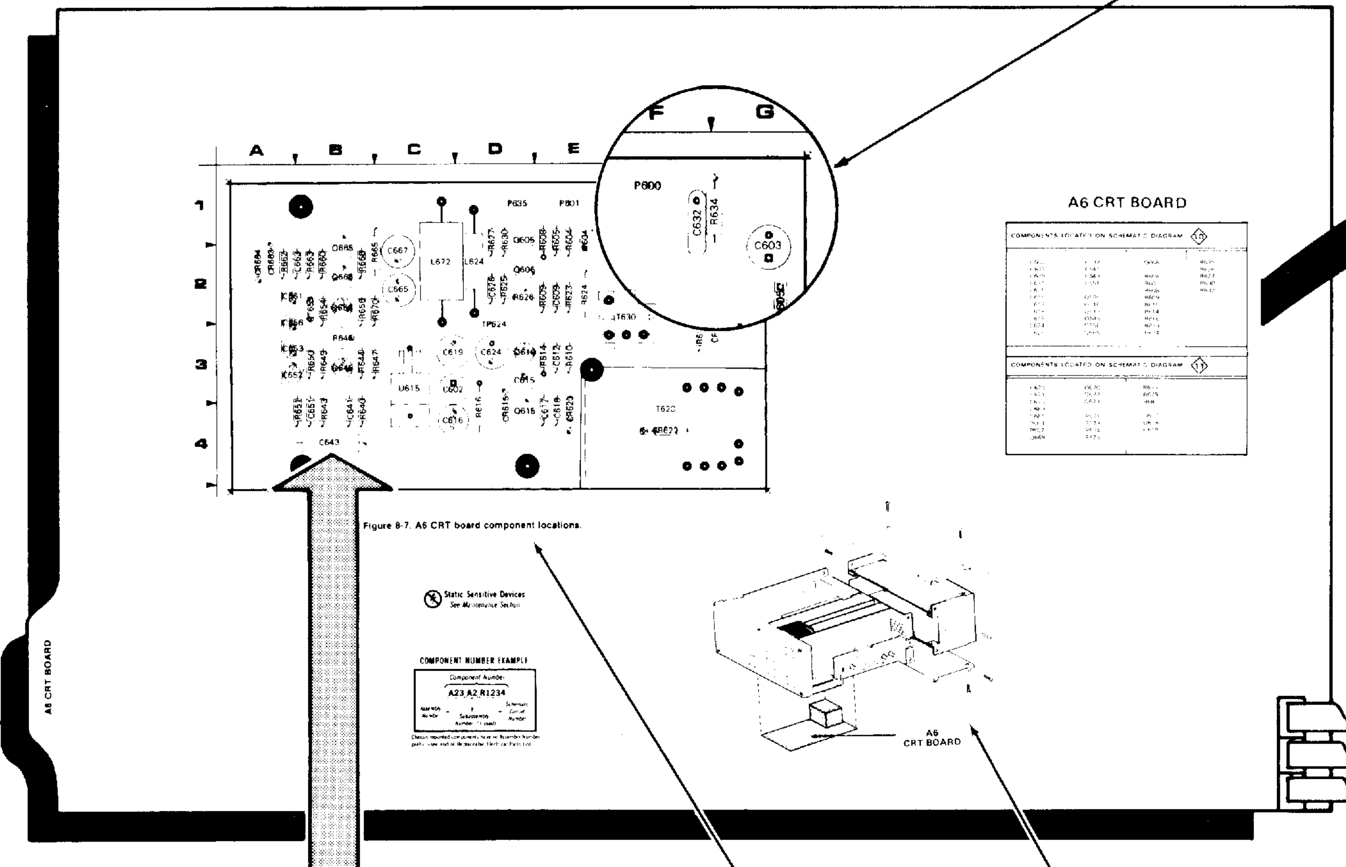
3. Locate the Component on the Schematic Diagram

a. Locate and pull out tabbed page whose number and title correspond with the Schematic Diagram Number just determined in the table. Schematic diagram nomenclature and numbers are printed on the front side of the tabs (facing the front of the manual).

b. Scan the Component Location Table adjacent to the schematic diagram and find the Circuit Number of the desired component.

c. Under the SCHEM LOCATION column, read the grid coordinates for the desired component.

d. Using the Circuit Number and grid coordinates, locate the component on the schematic diagram.



A6 CRT BOARD

PULL OUT PAGE TABS FOR CIRCUIT BOARD ILLUSTRATION

ASSEMBLY NUMBER AND CIRCUIT BOARD NAME

ILLUSTRATION FOR INSTRUMENT CIRCUIT BOARD LOCATION

MANUAL BINDER

A6 CRT BOARD

COMPONENTS LOCATED ON SCHEMATIC DIAGRAM 10			
C602	C632	Q668	R625
C603	C641		R626
C609	C643	R604	R627
C671	C651	R605	R630
C615		R608	R632
C616	Q606	R609	
C617	Q610	R610	
C618	Q615	R614	
C619	Q645	R616	
C624	Q656	R623	
C626	Q665	R624	

COMPONENTS LOCATED ON SCHEMATIC DIAGRAM 11			
C670	Q670	R677	
C671	Q672	R679	
C673	Q673	R680	
C680			
C681	R671	U617	
P603	R673	U618	
P607	R674	U619	
Q669	R675		

COMPONENT LOCATION TABLE

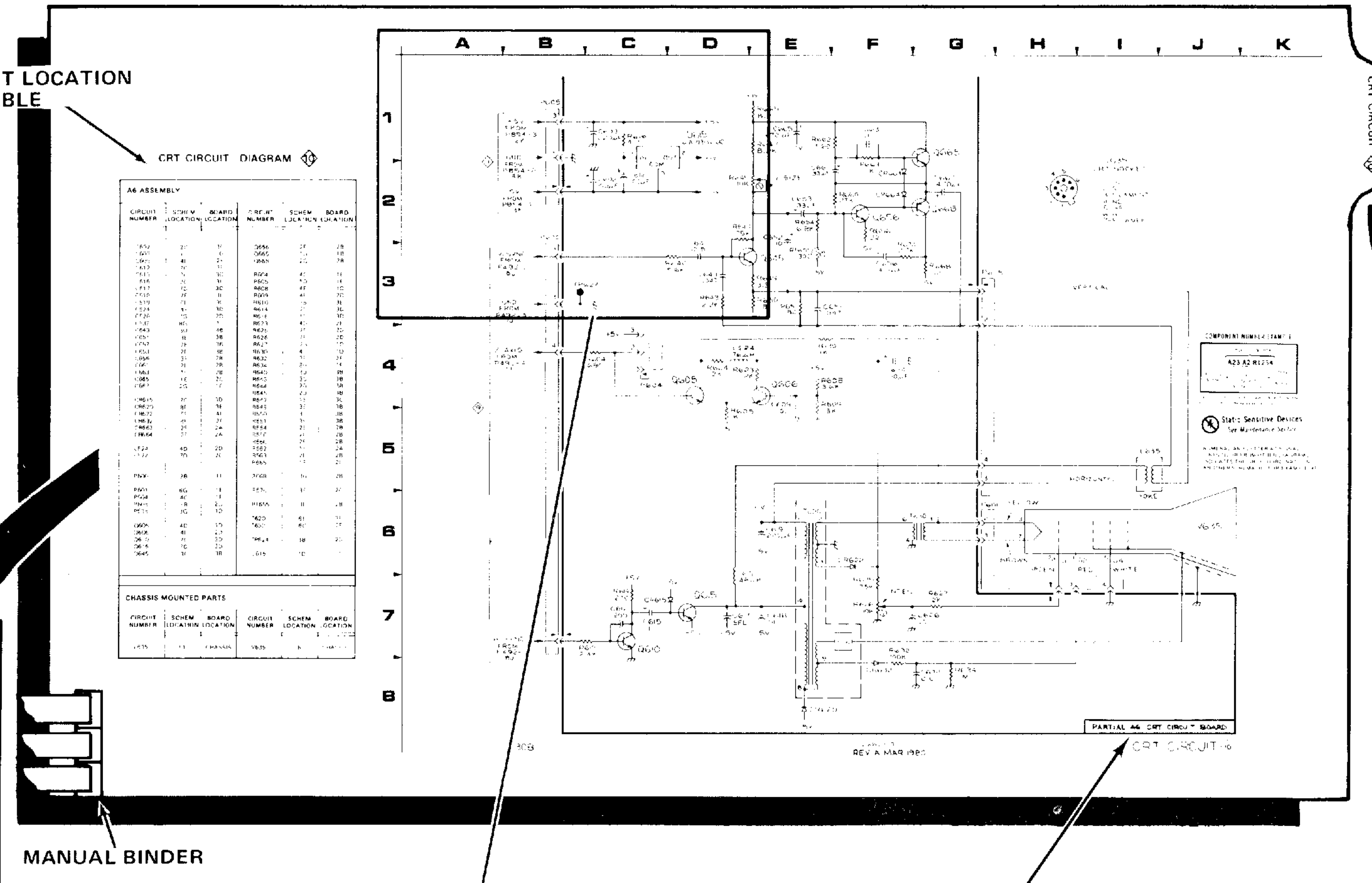
CRT CIRCUIT DIAGRAM 10

A6 ASSEMBLY

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C602	2C	3C	Q656	2F	2B
C603	1C	1G	Q665	1G	1B
C609	4E	[illegible]	Q668	2G	2B
C612	7C	3E			
C615	7C	3D	R604	4C	1E
C616	2C	3C	R605	5D	1E
C617	7D	3D	R608	4E	1D
C618	7E	3E	R609	4E	2D
C619	6E	3C	R610	7B	3E
C624	4F	3D	R614	7C	3D
C626	7G	2D	R616	1C	3D
C632	8G	1F	R623	4D	2E
C643	3D	4B	R625	7F	2D
C651	3E	3B	R626	7F	2D
		3B	R627	7G	1D
			R630	4F	[illegible]
Q605					
Q606	4E	2D			
Q610	7C	3D	TP624	3B	2D
Q615	7D	3D			
Q645	3E	3B	U615	1D	3C

CHASSIS MOUNTED PARTS

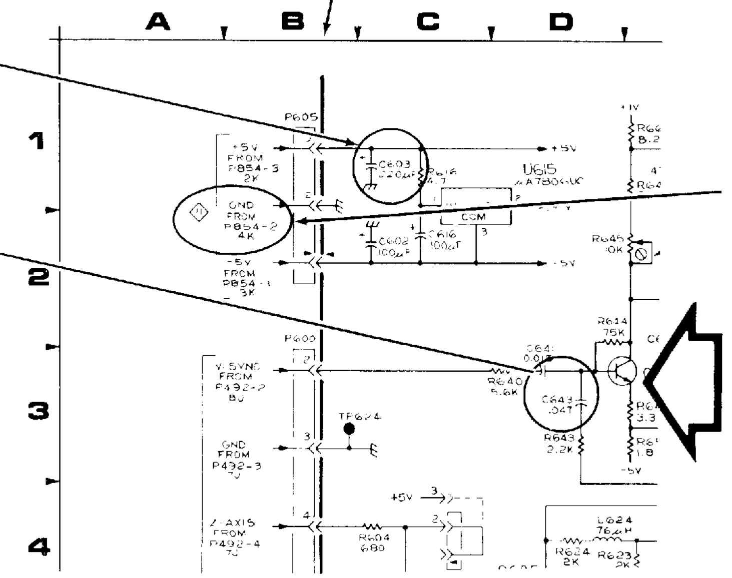
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
L635	51	CHASSIS	V635	6J	CHASSIS



PULL OUT PAGE TABS FOR SCHEMATIC DIAGRAMS

CRT CIRCUIT 10

MANUAL BINDER



PARTIAL A6 CRT CIRCUIT BOARD

CRT CIRCUIT 10

SCHEMATIC DIAGRAM NAME AND NUMBER

Numeral and letter at signal lines to or from other diagrams indicates the grid coordinates on another schematic (for example: 4K)

To identify any component in a schematic diagram and to locate that component on its respective circuit board.

5. Locate the Component on the Circuit Board

a. In the manual, locate and pull out the tabbed page whose title and Assembly Number correspond with the desired circuit board. This information is on the back side of the tabs.

b. Using the Circuit Number and grid coordinates, locate the component on the Circuit Board Illustration.

c. In the circuit board location illustration, determine the location of the circuit board in the instrument.

d. Find the circuit board in the instrument and compare it with its illustration in the manual to locate the desired component on the board.

4. Determine the Circuit Board Illustration and Component Location

a. From the schematic diagram, determine the Assembly Number of the circuit board on which the component is mounted. This information is boxed and located in a corner of the heavy line that distinguishes the board outline.

b. Scan the Component Location Table for the Assembly Number just determined and find the Circuit Number of the desired component.

c. Under the BOARD LOCATION column, read the grid coordinates for the desired component.

Figure 9-3. Locating components on schematic diagrams and circuit board illustrations.

4204-58 A

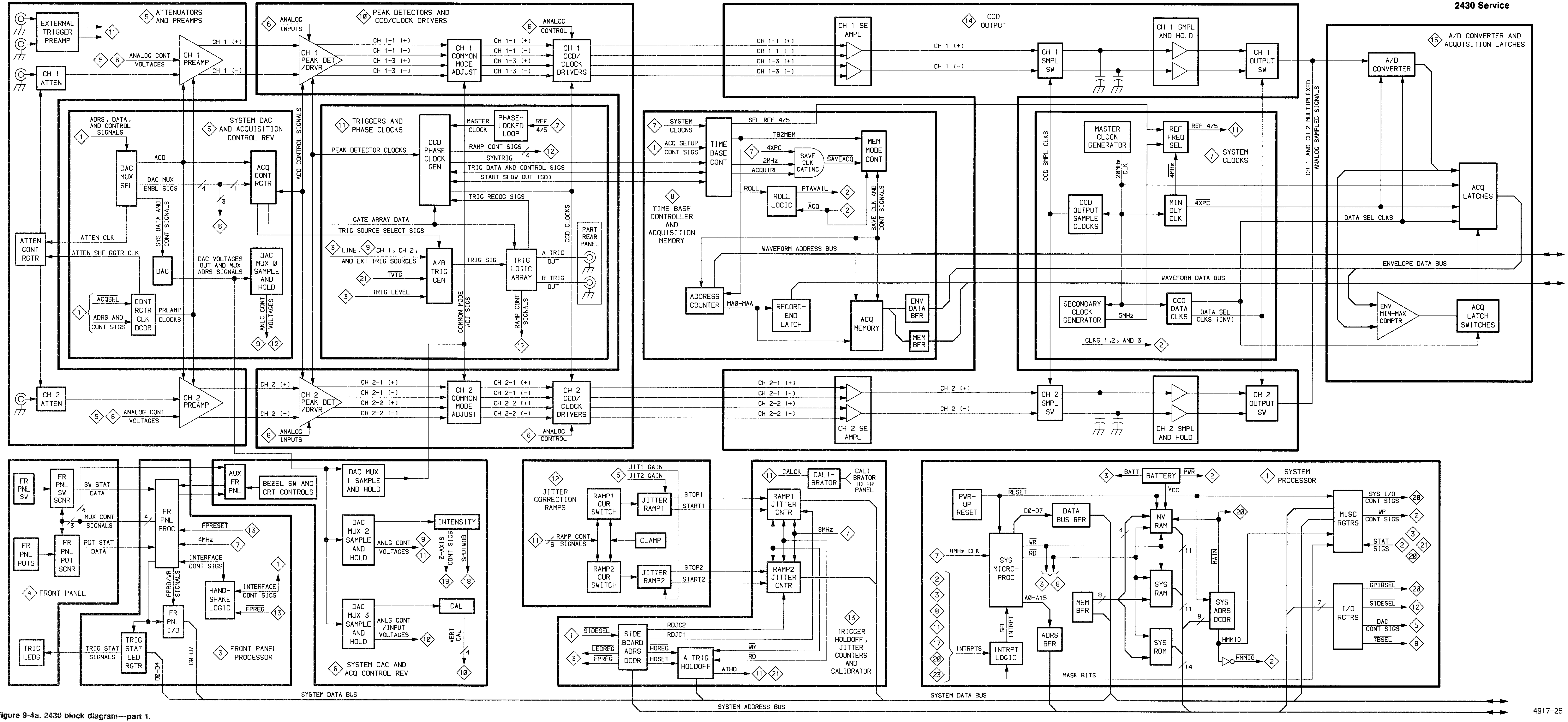


Figure 9-4a. 2430 block diagram—part 1.

2430 BLOCK DIAGRAM—PART 1

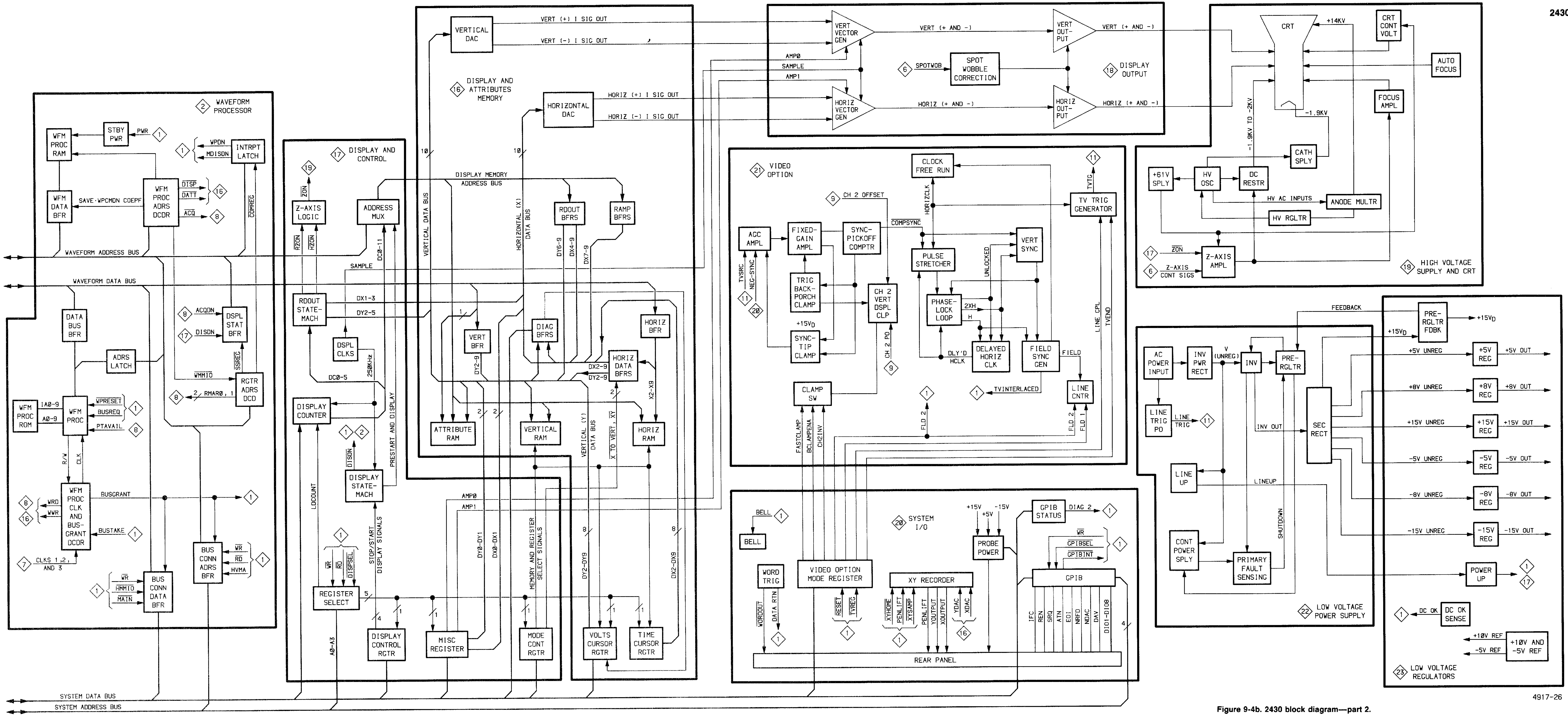
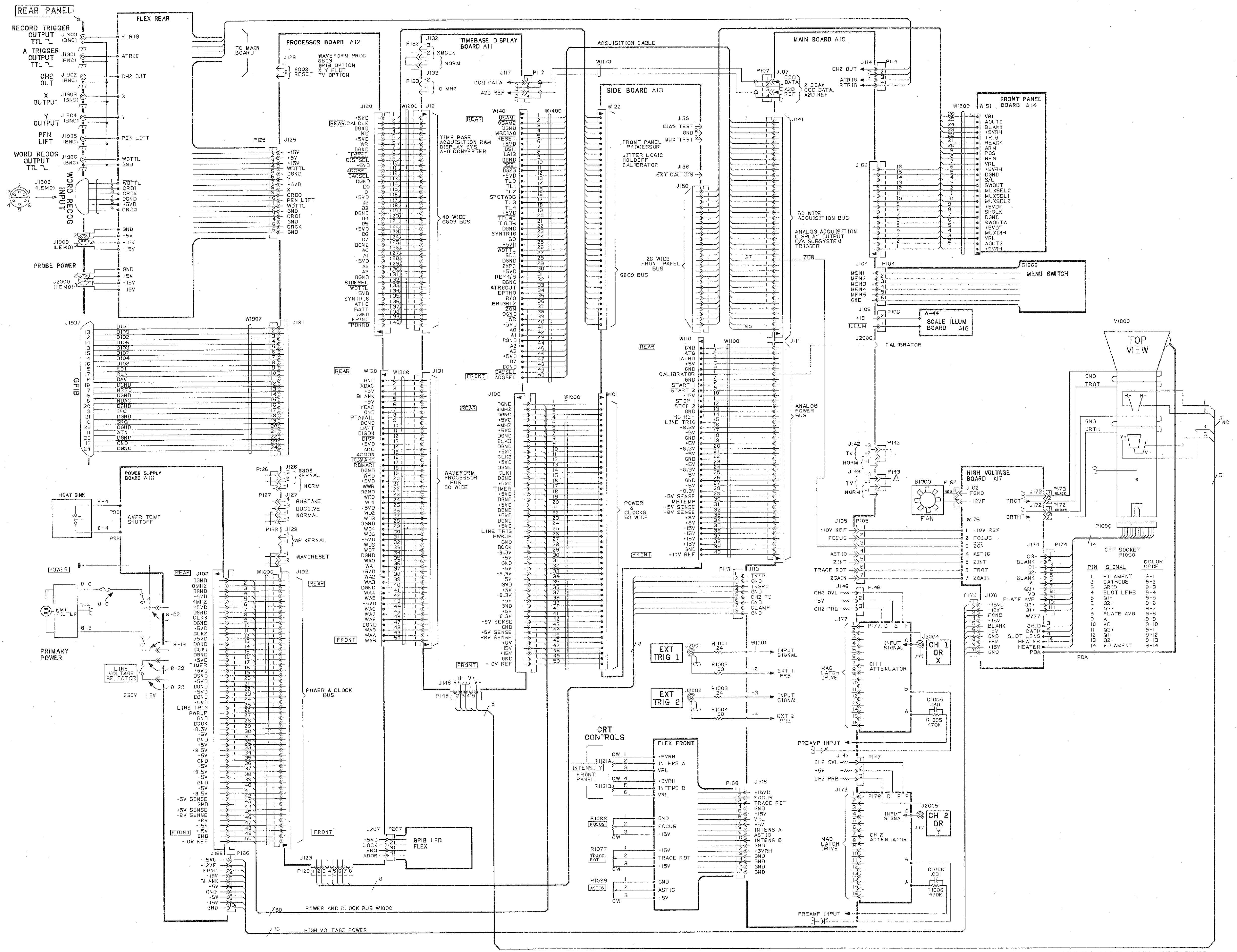


Figure 9-4b. 2430 block diagram—part 2.

2430 BLOCK DIAGRAM—PART 2



4917-64

CIRCUIT BOARD INTERCONNECTIONS

TEST WAVEFORMS

Test waveforms for schematic diagrams (if applicable) precede the schematic. They are intended to aid in troubleshooting the instrument. Special conditions required of the test oscilloscope are given above the waveform; special conditions for the 2430 under test are given beneath the waveform. Unless otherwise stated, the test conditions for the first waveform listed pertain to all the waveforms for a given schematic diagram. Normal control settings for the test oscilloscope are given in the readouts shown in each waveform illustration.

RECOMMENDED TEST EQUIPMENT

Item	Specification	Example
Test oscilloscope with 10X probe and 1X probe (1X probe is optional accessory.)	Digital Storage; frequency response: dc to 40 MHz single event bandwidth to 150 MHz equivalent-time sampling.	TEKTRONIX 2430 Digial Oscilloscope with two 10X probes.
Calibration Generator	Standard-amplitude signal levels: 5 mV to 50 V. Accuracy ±3%.	TEKTRONIX PG 506 Calibration Generator.[a]
Digital Voltmeter (DMM)	Range 0 to 140 V. Dc voltage accuracy: ±0.15%. 4 1/2 digit display.	TEKTRONIX DM 501A Digital Multimeter.[a]
High Voltage Probe for DMM	Maximum voltage 20 kV.	Fluke Model 80K-40 High Voltage Probe.
Precision Coaxial Cable	Impedance: 50 ohm. Length: 36 in. Connectors: BNC.	Tektronix Part Number 012-0482-00.
Dual-Input Coupler	Connectors: BNC female-to-dual-BNC male.	Tektronix Part Number 103-0090-00.
Sync and Linearity Test Generator	Conforms to TV System requirements.	TEKTRONIX R147A NTSC Test Signal Generator. TEKTRONIX R148 Insertion Test Signal Generator.
Coaxial Cable (2 required)	Impedance: 75 ohm. Length: 42 in. Connectors: BNC.	Tektronix Part Number 012-0074-00.

[a]TM 500-Series Power-Module Mainframe required.

DC VOLTAGE MEASUREMENTS

Dc voltages indicated on the schematic diagrams are typical of a normally operating instrument. Voltages are with respect to chassis ground except in the isolated portion of the Low Voltage Power Supply, where they are with respect to the REF NODE indicated by the darker line in the Control Power Supply circuitry.

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM NUMBER	SCHEM LOCATION	CIRCUIT NUMBER	SCHEM NUMBER	SCHEM LOCATION	CIRCUIT NUMBER	SCHEM NUMBER	SCHEM LOCATION	CIRCUIT NUMBER	SCHEM NUMBER	SCHEM LOCATION
B1000	19	7A	P103	1	5A	P123	21	3A	P150	3	6A
			P103	1	9A	P123	21	6G	P150	3	6N
C1005	9	1F	P103	20	2A	P123	21	7N	P150	3	7A
C1006	9	6F	P103	2	1A	P125	20	1L	P152	6	1J
			P103	2	2A	P125	20	4H	P152	6	2J
FL1000	22	1A	P104	6	1J	P126	1	5E	P152	6	2M
			P105	19	1C	P127	2	2A	P162	19	7A
			P105	19	8C	P128	2	6A	P166	23	1M
J30	22	1A	P105	6	5M	P131	16	1A	P166	23	3M
J60	22	1A	P106	6	3G	P131	16	7A	P166	23	4M
J70	22	4A	P107	14	4N	P131	17	1J	P166	23	5M
J80	22	4A	P108	19	1B	P131	17	4K	P166	23	8M
J1900	11	7K	P111	10	7E	P131	18	3M	P172	19	2M
J1901	11	6K	P111	10	8D	P131	18	5A	P173	19	2G
J1902	9	6N	P111	11	6A	P131	18	8M	P174	19	1G
J1903	20	2M	P111	11	7J	P131	8	1E	P174	19	2G
J1904	20	2M	P111	12	2M	P131	8	1M	P174	19	2M
J1905	20	1M	P111	13	7E	P131	8	6M	P174	19	4M
J1906	20	3M	P111	14	4A	P131	8	7F	P176	19	6A
J1907	20	2G	P111	6	8M	P131	8	7L	P181	20	2F
J1908	20	4G	P111	9	5F	P141	10	2F	P207	20	6L
J1908	20	5M	P113	11	7E	P141	11	1A			
J1909	20	4M	P113	11	8A	P141	11	5K	R1000	22	2A
J2000	20	4M	P113	9	3H	P141	11	6E	R1001	9	7B
J2001	9	7A	P113	9	4N	P141	11	6J	R1002	9	7B
J2002	9	7A	P114	11	6J	P141	11	6N	R1003	9	7B
J2004	9	1C	P114	9	6N	P141	11	7A	R1004	9	8B
J2005	9	6C	P117	15	3A	P141	14	2G	R1005	9	1F
			P120	1	1K	P141	14	3G	R1006	9	6F
L1000	19	1K	P120	1	2M	P141	14	6G	R1015	9	1G
			P120	1	4E	P141	14	8G	R1016	9	6G
P100	17	4A	P120	1	6K	P141	19	8B	R1077	19	1A
P100	18	3A	P120	1	8A	P141	5	1A	R1088	19	3A
P100	7	2N	P120	1	8M	P141	5	3M	R1099	19	2A
P100	7	7E	P120	20	4J	P141	6	5A	R1121A	6	4J
P100	8	6F	P120	20	5A	P141	6	6G	R1121B	6	2J
P102	22	1D	P120	21	8H	P146	9	1F			
P102	23	1M	P121	17	1A	P147	9	6F	S1000	22	4A
P102	23	3M	P121	18	2A	P148	18	2M	S1020	22	3C
P102	23	4E	P121	8	1C	P148	18	4M	S1350	22	1A
P102	23	4M	P121	8	3A	P148	18	6M	S1666	6	2H
P102	23	5M	P121	8	6F	P150	3	1C			
P103	1	4A	P121	8	8A	P150	3	2N			

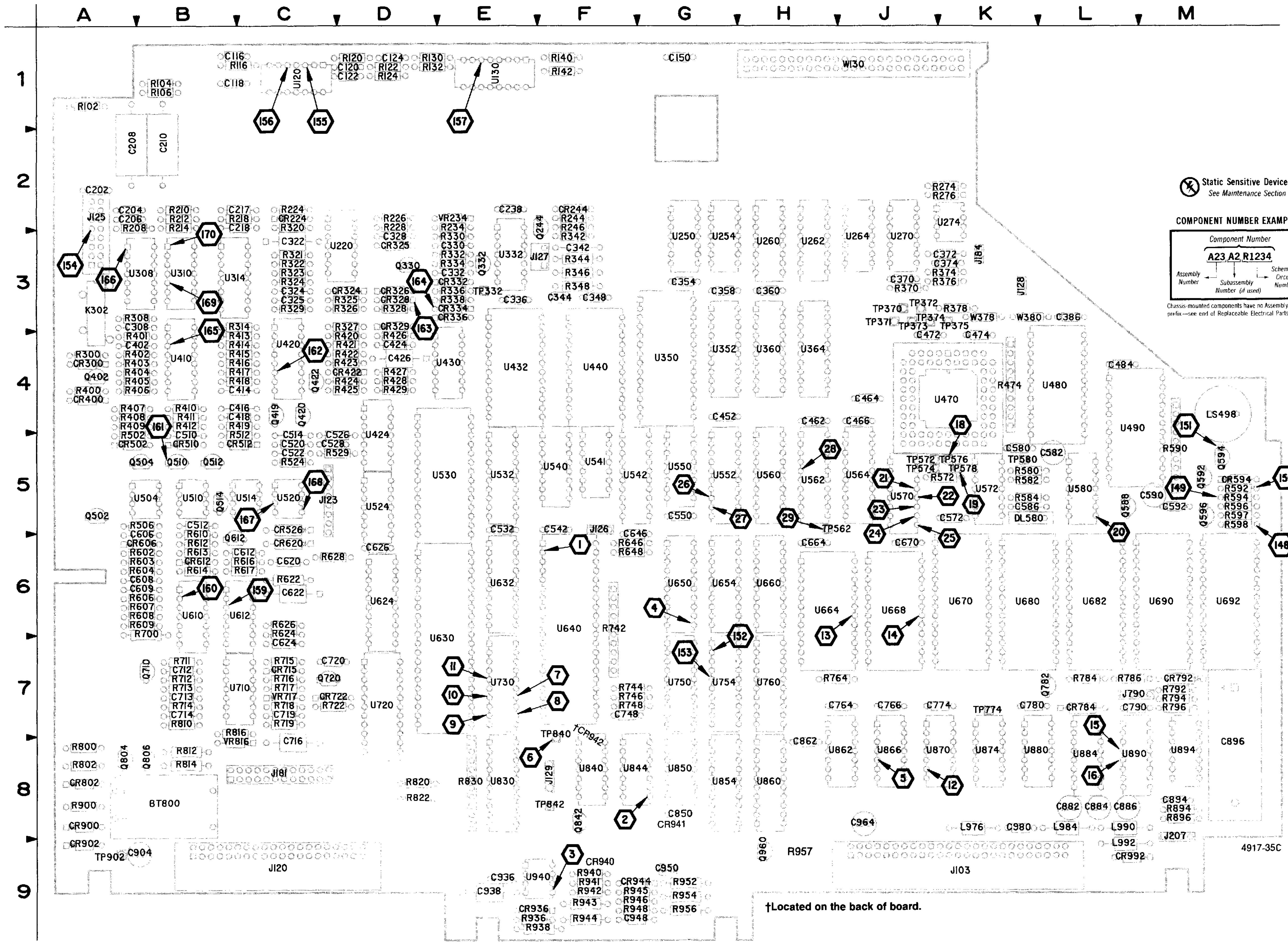
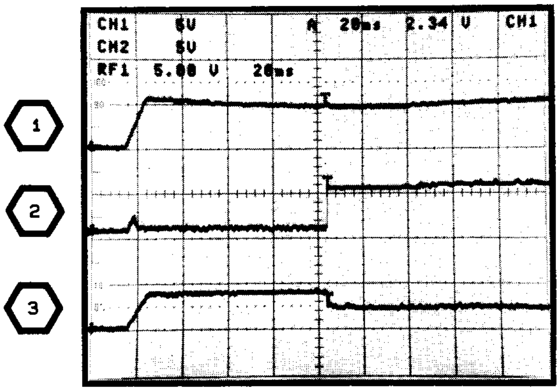


Figure 9-5. A12—Processor board.

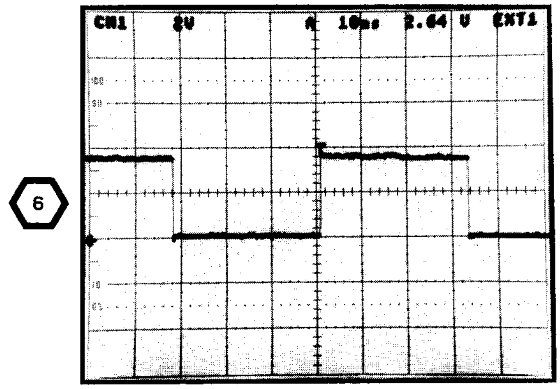
A12—PROCESSOR BOARD

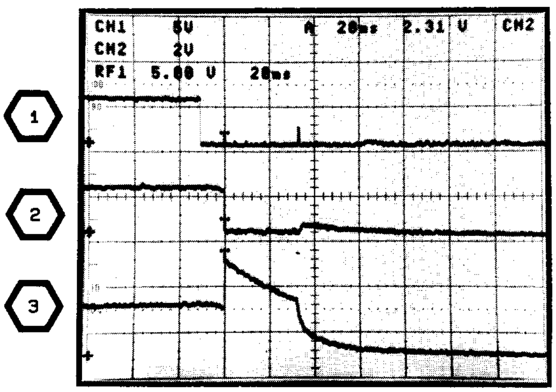
CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
BT800	1	C720	20	L984	20	R376	2	R744	1	U424	21
		C748	20	L990	20	R378	2	R746	1	U430	21
C116	20	C764	20	L992	20	R400	20	R748	1	U432	2
C118	20	C766	20			R401	21	R764	1	U440	2
C120	20	C774	20	LS498	20	R402	21	R784	2	U470	2
C122	20	C780	20			R403	21	R786	2	U480	2
C124	20	C790	20	Q244	2	R404	21	R792	20	U490	2
C150	20	C850	20	Q330	21	R405	21	R794	20	U504	21
C202	20	C862	20	Q332	2	R406	21	R796	20	U510	21
C204	20	C882	20	Q402	20	R407	21	R800	1	U514	21
C206	20	C884	20	Q419	21	R408	21	R802	1	U520	21
C208	20	C886	20	Q420	21	R409	21	R810	21	U524	21
C210	20	C894	20	Q422	21	R410	21	R812	1	U530	21
C217	21	C896	2	Q502	21	R411	21	R814	1	U532	20
C218	21	C904	1	Q504	21	R412	21	R816	21	U540	2
C238	20	C936	20	Q510	21	R413	21	R820	1	U541	21
C308	21	C938	1	Q512	21	R414	21	R822	1	U542	2
C322	21	C948	1	Q514	21	R415	21	R830	1	U550	2
C324	21	C950	1	Q588	20	R416	21	R894	1	U552	2
C325	21	C964	20	Q592	20	R417	21	R896	1	U560	2
C328	21	C980	20	Q594	20	R418	21	R900	1	U562	2
C330	21			Q596	20	R419	21	R936	1	U564	2
C332	21	CR224	21	Q612	21	R420	21	R938	1	U570	2
C336	20	CR244	2	Q710	21	R421	21	R940	1	U572	1
C342	2	CR300	20	Q720	20	R422	21	R941	1	U572	2
C344	2	CR324	21	Q782	2	R423	21	R942	1	U580	1
C348	20	CR325	21	Q804	1	R424	21	R943	1	U580	2
C354	2	CR326	21	Q806	1	R425	21	R944	1	U610	21
C358	20	CR328	21	Q842	1	R426	21	R945	1	U612	21
C360	20	CR329	21	Q960	1	R427	21	R946	1	U624	20
C370	20	CR332	21			R428	21	R948	1	U630	20
C372	20	CR334	21	R102	21	R429	21	R952	1	U632	1
C374	20	CR336	21	R104	20	R474	2	R954	1	U640	1
C386	20	CR400	20	R106	20	R502	21	R956	1	U650	1
C402	21	CR422	21	R116	20	R506	21	R957	2	U654	1
C414	21	CR502	21	R120	20	R512	21			U660	1
C416	21	CR510	21	R122	20	R524	21	TP332	20	U664	1
C418	21	CR512	21	R124	20	R529	21	TP370	2	U668	1
C424	21	CR526	21	R130	20	R572	2	TP371	2	U670	1
C426	21	CR594	20	R132	20	R580	2	TP372	20	U680	1
C452	20	CR606	21	R140	20	R582	2	TP373	2	U682	1
C462	20	CR612	21	R142	20	R584	2	TP374	2	U690	1
C464	20	CR620	21	R208	21	R590	2	TP375	2	U692	1
C466	20	CR715	21	R210	21	R592	20	TP562	2	U710	21
C472	20	CR722	20	R212	21	R594	20	TP572	20	U720	20
C474	20	CR784	2	R214	21	R596	20	TP574	20	U730	1
C484	20	CR792	2	R218	21	R597	20	TP576	2	U750	20
C510	21	CR802	1	R224	21	R598	20	TP578	2	U754	20
C512	21	CR900	1	R226	21	R602	21	TP580	2	U760	1
C514	21	CR902	1	R228	21	R603	21	TP774	20	U830	1
C520	21	CR936	1	R234	21	R604	21	TP840	1	U840	1
C522	21	CR940	1	R244	2	R606	21	TP842	2	U840	2
C526	21	CR941	1	R246	2	R607	21	TP902	20	U844	1
C528	21	CR942	1	R274	20	R608	21			U844	20
C532	20	CR944	1	R276	20	R609	21	U120	20	U850	1
C542	20	CR992	20	R300	20	R610	21	U130	20	U850	2
C550	20			R308	21	R612	21	U220	21	U854	1
C572	20	DL580	2	R314	21	R613	21	U250	2	U860	1
C580	20			R320	21	R614	21	U254	1	U862	1
C582	2	J103	1	R321	21	R616	21	U254	2	U866	1
C586	2	J103	2	R322	21	R617	21	U260	2	U866	2
C590	20	J103	20	R323	21	R622	21	U262	2	U870	1
C592	20	J120	1	R324	21	R624	21	U264	2	U870	2
C606	21	J120	20	R325	21	R626	21	U264	20	U874	2
C608	21	J120	21	R326	21	R628	20	U270	2	U880	1
C609	21	J123	21	R327	21	R646	1	U270	20	U884	1
C612	21	J125	20	R328	21	R648	1	U274	20	U890	1
C620	21	J126	1	R329	21	R700	21	U308	21	U894	1
C622	21	J127	2	R330	21	R711	21	U310	21	U940	1
C624	21	J128	2	R332	20	R712	21	U314	21		
C626	20	J129	1	R334	21	R713	21	U332	1	VR234	21
C646	20	J181	20	R336	21	R714	21	U332	2	VR717	20
C664	1	J184	2	R338	21	R715	21	U332	20	VR816	21
C670	20	J207	20	R342	2	R716	20	U350	2		
C712	21	J790	1	R344	2	R717	20	U352	2	W130	2
C713	21			R346	2	R718	20	U360	2	W130	20
C714	21	K302	20	R348	2	R719	21	U364	2	W378	2
C716	21			R370	2	R722	20	U410	21	W380	2
C719	21	L976	20	R374	2	R742	1	U420	21		

WAVEFORMS FOR DIAGRAM 1



AT POWER ON





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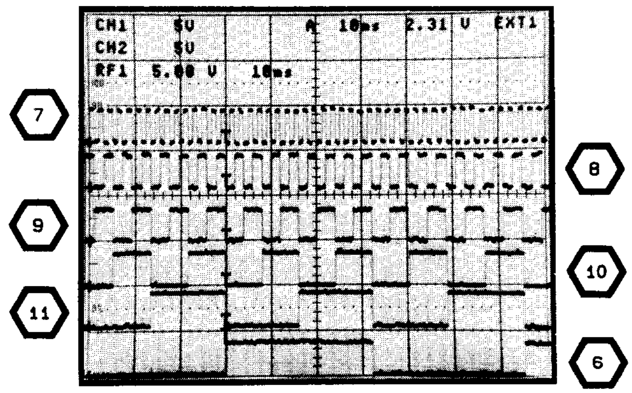
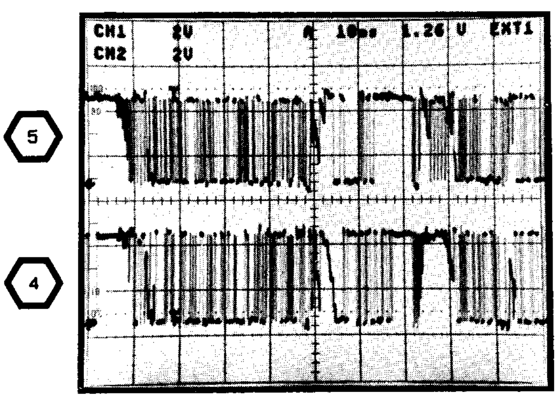
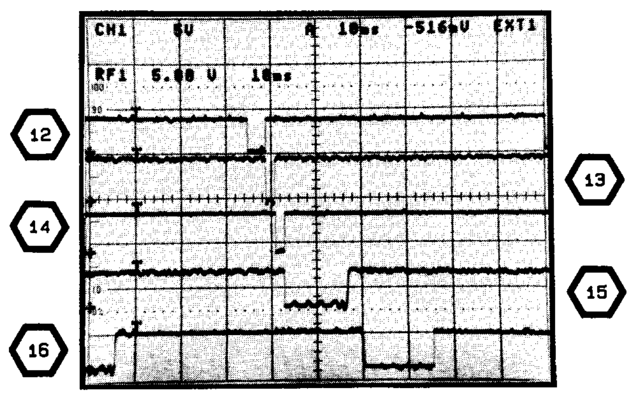
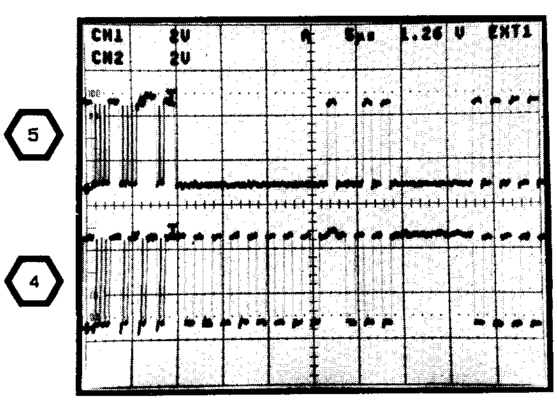








4917-72

SYSTEM PROCESSOR DIAGRAM 1

ASSEMBLY A12

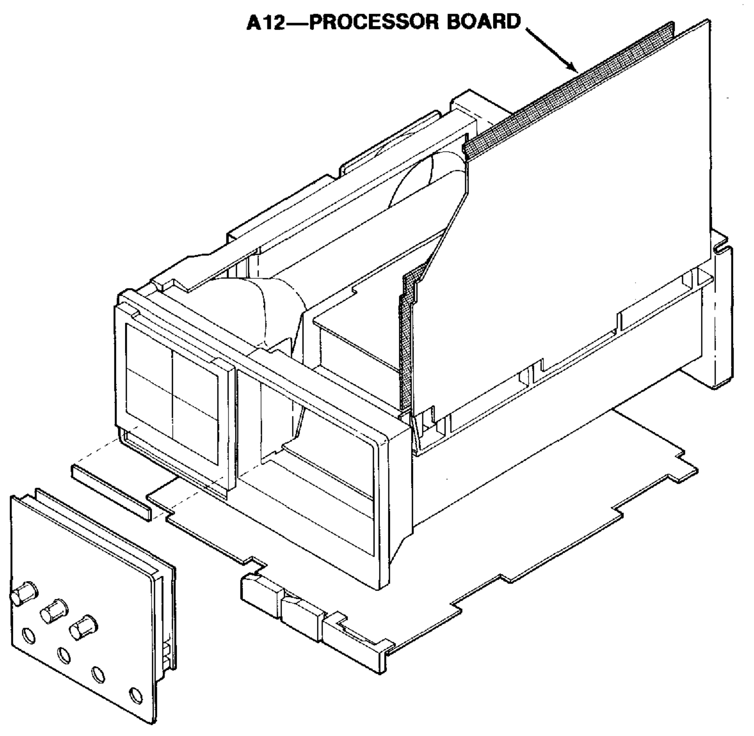
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
BT00800	1J	8A	Q804	1H	8A	R942	5B	9F	U730	8H	7E
			Q806	1G	8B	R943	5A	9F	U760	7L	7H
C664	1H	6H	Q842	2G	8F	R944	5A	9F	U830	8K	8E
C904	1J	9B	Q960	2H	9H	R945	2G	9F	U840A	3G	8F
C938	5A	9E				R946	2G	9F	U840B	2G	8F
C948	2G	9F	R646	6E	6F	R948	2G	9F	U840D	4D	8F
C950	2H	9G	R648	8G	6F	R952	2H	9G	U844A	4E	8F
			R742A	5C	6F	R954	2H	9G	U844B	4D	8F
CR802	1H	8A	R742B	5B	6F	R956	2H	9G	U844C	5C	8F
CR900	1H	8A	R742C	4C	6F				U850B	7C	8G
CR902	1J	9A	R742	6D	6F	TP840	9H	8F	U854	7K	8G
CR936	5B	9E	R744	7D	7F				U860	7F	8H
									U862	4L	8J
CR940*	5B	8G	R746	7D	7F	U254A	8B	3G	U866A	4L	8J
CR941*	5B	8F	R748	7J	7F	U254C	3F	3G	U866B	4M	8J
CR942*	5C	4F	R764	2H	7H	U332A	3L	3E	U866C	4J	8J
CR944	2H	9F	R800	1H	8A	U572C	5D	5K	U866D	4D	8J
			R802	1J	8A	U580A	4L	5L	U870A	4J	8K
J103	4A	9K	R812	1G	8B	U580B	7B	5L	U870B	4L	8K
J103	5A	9K	R814	1G	8B	U632	8G	6E	U870D	5D	8K
J103	9A	9K	R820	9L	8D	U640	4C	6F	U880A	8B	8K
J120	1K	9C	R822	8L	8D	U650	7E	6G	U880B	7B	8K
J120	2M	9C	R830A	8B	8E	U654	8C	6G	U880C	8B	8K
J120	4E	9C	R830	8L	8E	U660	2M	6H	U880D	4D	8K
J120	6K	9C	R894	6B	8M	U664	2J	6H	U884	5J	8L
J120	8A	9C	R896	6B	8M	U668	2L	6J	U890A	5E	8L
J120	8M	9C	R900	1J	8A	U670	1A	6K	U890B	5F	8L
J126	5E	5F	R936	5B	9E	U680	1B	6K	U894A	6B	8M
J129	5A	8F	R938	5B	9E	U682	1C	6L	U940A	1J	9F
J790*	6H	7L	R940	5B	9F	U690	1D	6M	U940B	5B	9F
			R941	5B	9F	U692	1E	6M			

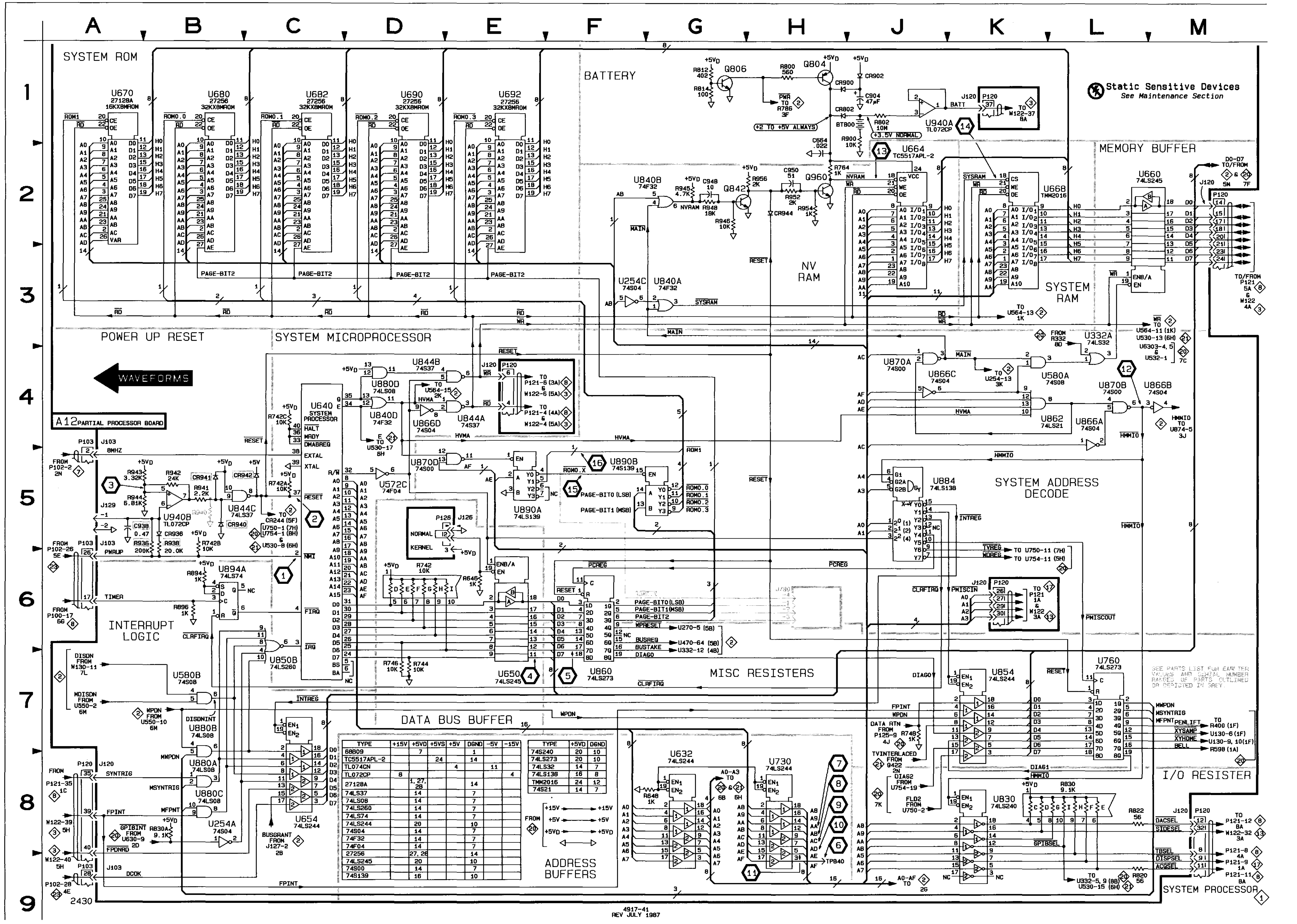
Partial A12 also shown on diagrams 2, 20 and 21.

CHASSIS MOUNTED PARTS

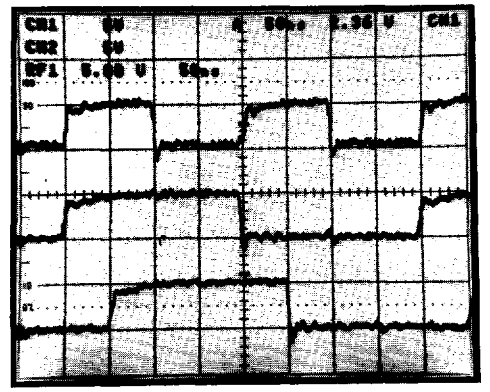
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P103	4A	CHASSIS	P120	1K	CHASSIS	P120	6K	CHASSIS	P126	5E	CHASSIS
P103	5A	CHASSIS	P120	2M	CHASSIS	P120	8A	CHASSIS			
P103	9A	CHASSIS	P120	4E	CHASSIS	P120	8M	CHASSIS			

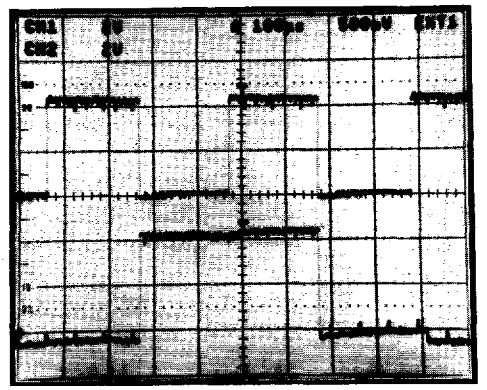
***See Parts List for serial number ranges.**

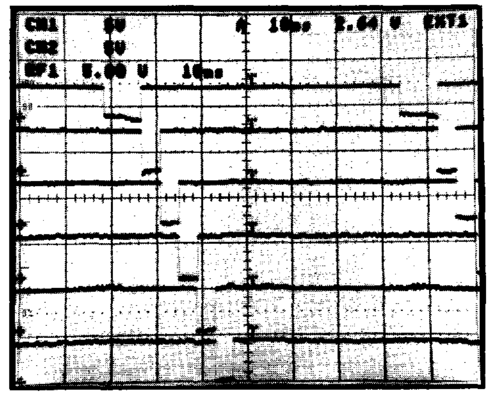


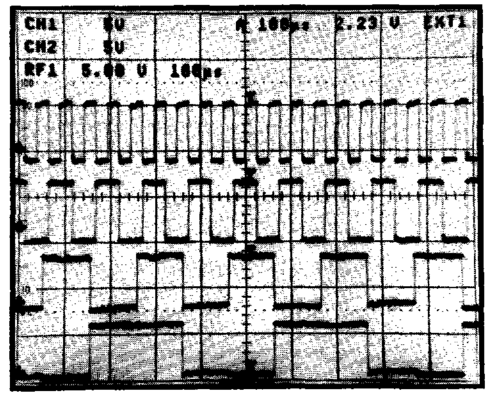


WAVEFORMS FOR DIAGRAM 2

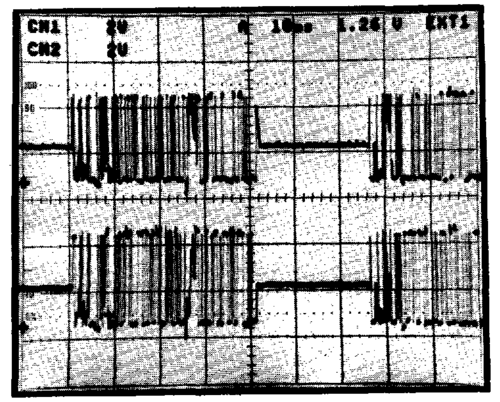




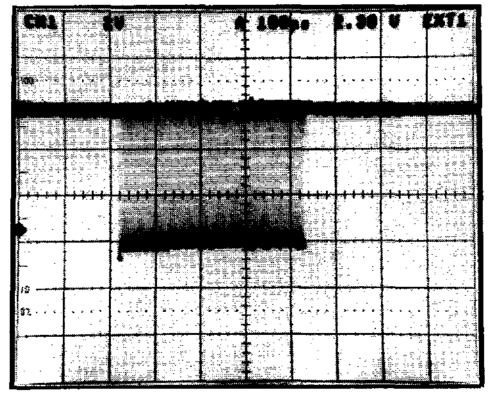


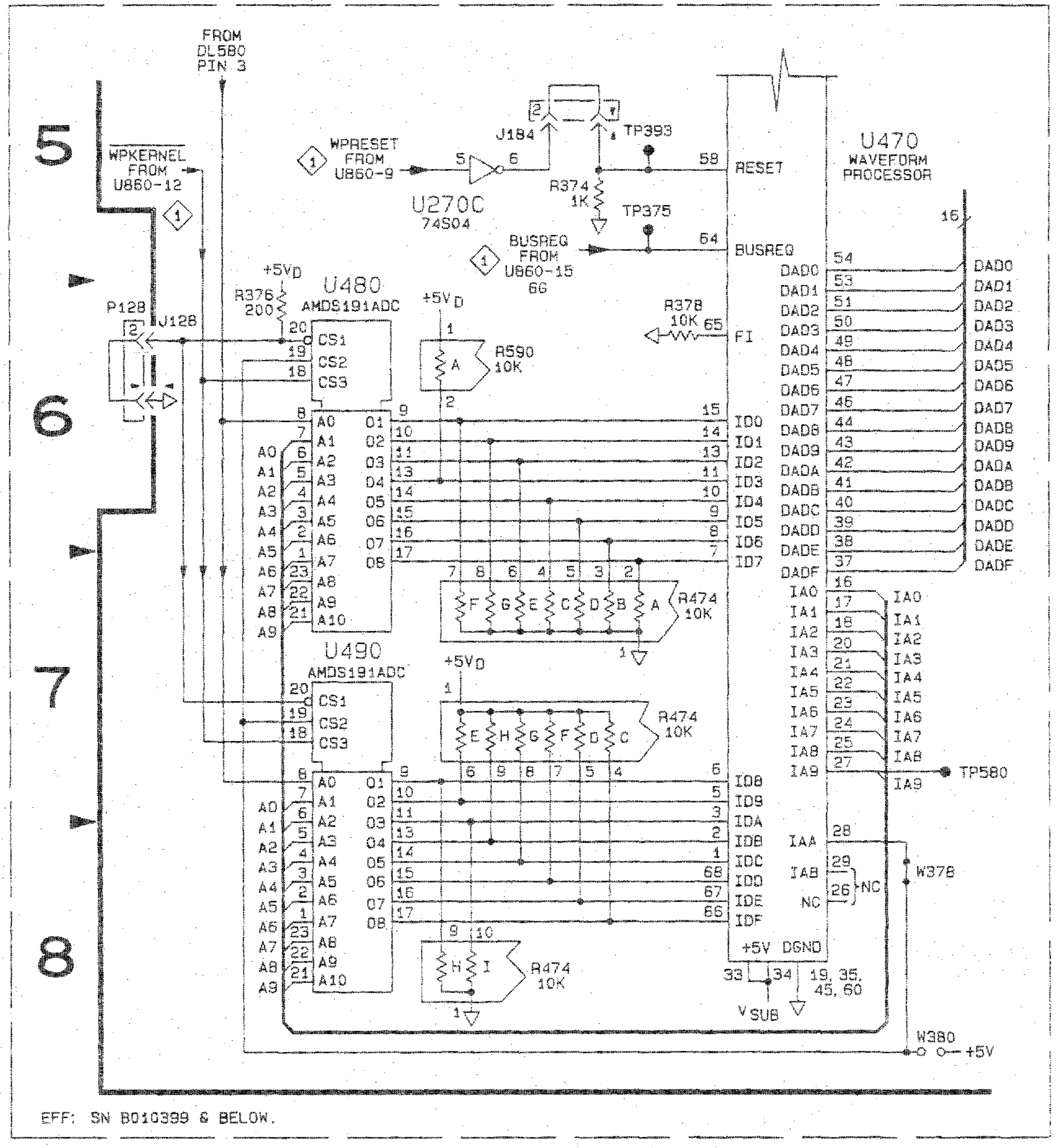


TEST SCOPE IN ENVELOPE



BUS ISOLATED





WAVEFORM PROCESSOR DIAGRAM 2

ASSEMBLY A12

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C342	5E	3F
C344	5F	3F
C354	4F	3G
C582	8F	5L
C586	3A	5K
C896	4G	8M
CR244	5F	2F
CR784	4G	7L
CR792	3G	7M
DL580	2A	5K
J103	1A	9K
J103	2A	9K
J127	1A	3F
J128	6A	3K
J184	5B	3K
Q244	5F	3E
Q332	5G	3E
Q782	3F	7L
R244	5E	2F
R246	5F	3F
R342	5E	3F
R344	5F	3F
R346	5F	3F
R348	5F	3F

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
R370	4D	3J
R374	5B	3K
R376	6A	3K
R378	5C	3K
R474	7C	4K
R474	8B	4K
R572	1E	5K
R580	4B	5K
R582	5B	5K
R584	3A	5K
R590	1E	5M
R590	6B	5M
R590	7C	5M
R784	4G	7L
R786	3F	7L
R957*	6K	9K
TP370	5C	3J
TP371	5D	3J
TP373	4D	3J
TP374	5C	3J
TP375	5C	3K
TP562	2G	5H
TP576	4C	5K
TP578	4C	5K
TP580	7D	5K
TP842	1B	8F
U250A	2D	3G

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
U250B	2D	3G
U250C	6G	3G
U250D	7G	3G
U254B	1G	3G
U254D	3L	3G
U254E	7G	3G
U254F	3K	3G
U260	1J	3H
U262	1H	3H
U264A	3C	3J
U264B	1C	3J
U264C	2C	3J
U270A	3B	3J
U270B	1E	3J
U270C	5B	3J
U270D	6J	3J
U270E	2C	3J
U332D	3B	3E
U350	5H	4G
U352	4K	4G
U360	3D	4H
U364	1G	4H
U432	8H	4E
U440	7J	4F
U470	5C	4K
U480	6A	4L
U490	7A	4L
U540	6J	5F
U542A	6L	5F

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
U542B	1D	5F
U550	6M	5G
U552	3M	5G
U560	2E	5H
U562	3G	5H
U564	1L	5J
U570	4D	5J
U572A	4B	5K
U572B	3C	5K
U572D	2B	5K
U572E	2D	5K
U572F	2D	5K
U580C	5E	5L
U580D	4G	5L
U840C	1B	8F
U850A	3K	8G
U866E	1B	8J
U866F	2C	8J
U870C	2C	8K
U874A	3J	8K
U874B	3J	8K
U874D	3H	8K
W130	2N	1J
W130	5A	1J
W130	6E	1J
W130	8K	1J
W378	8D	3K
W380	8D	3K

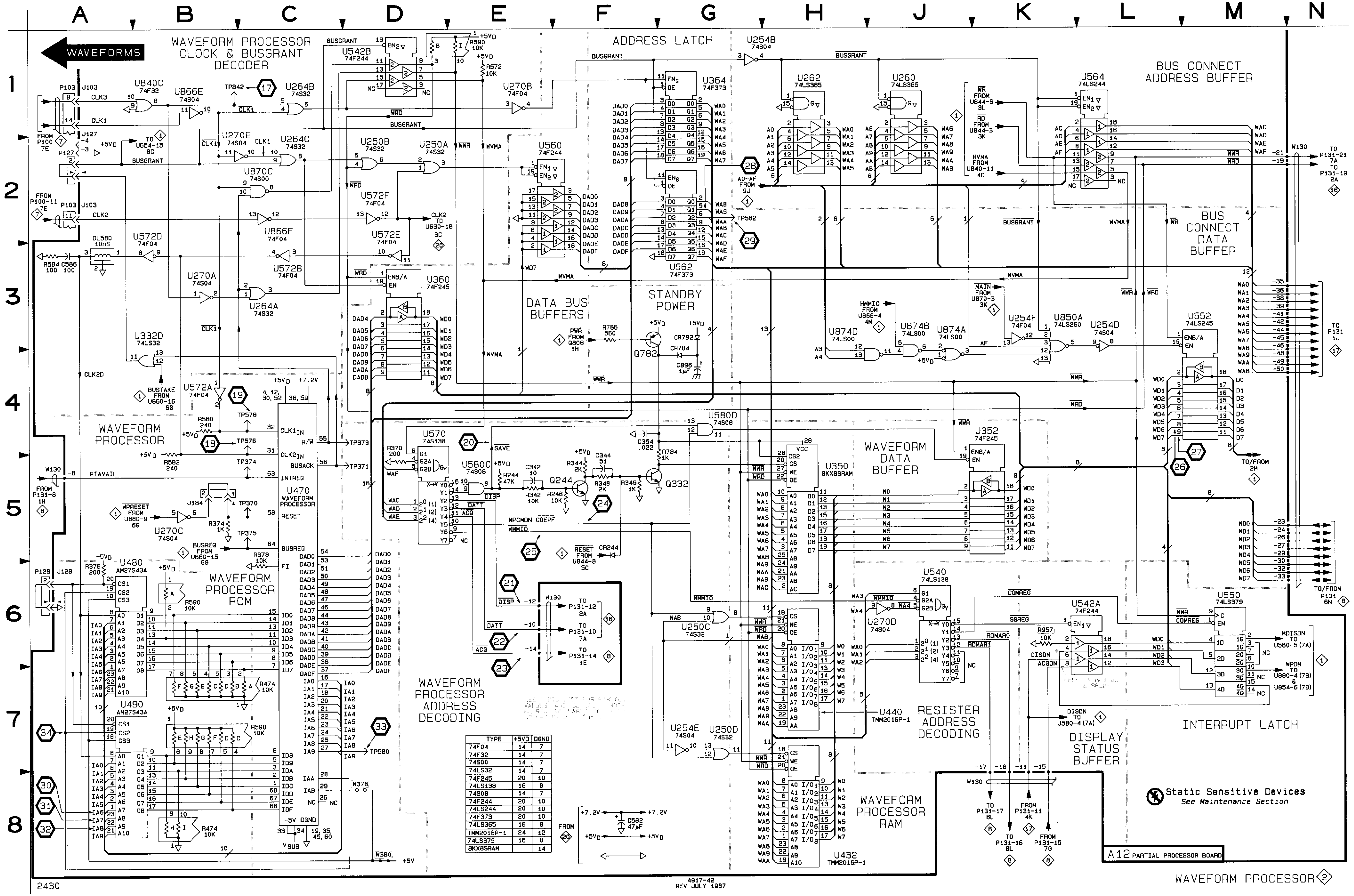
Partial A12 also shown on diagrams 1, 20 and 21.

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P103	1A	CHASSIS	P103	2A	CHASSIS	P127	2A	CHASSIS	P128	6A	CHASSIS

***See Parts List for serial number ranges.**

HISTORY



WAVEFORM PROCESSOR

2

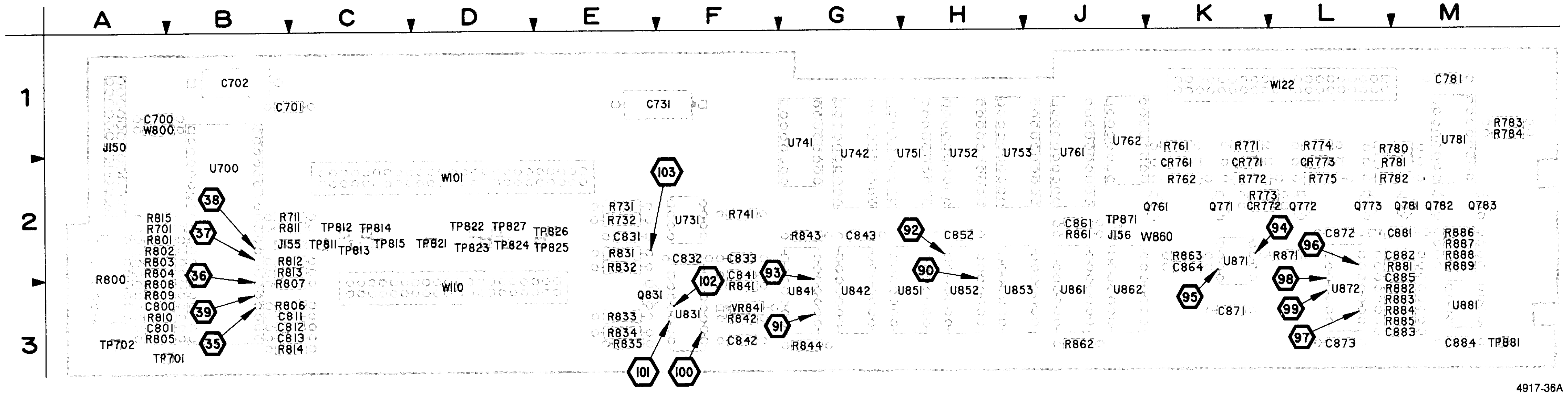


Figure 9-6. A13—Side board.

A13—SIDE BOARD

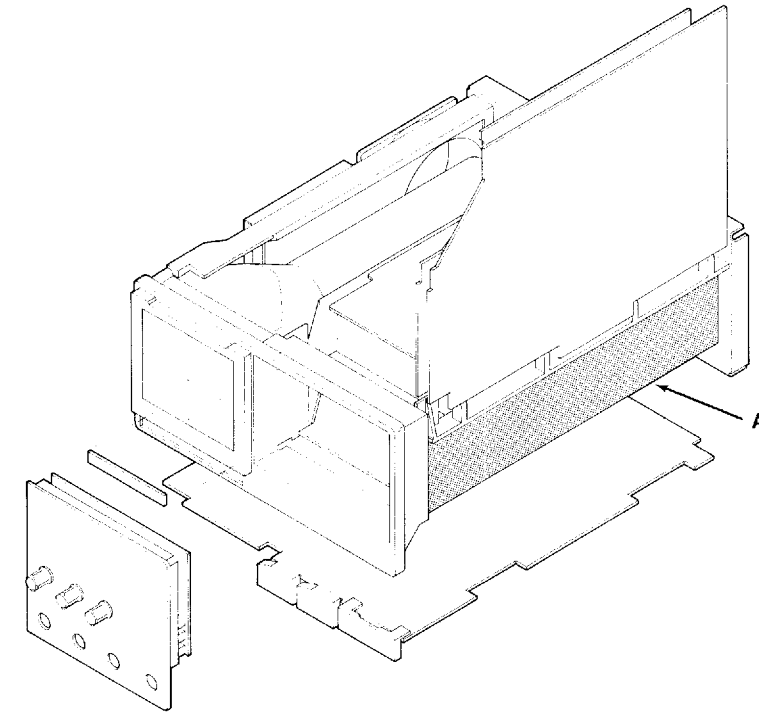
CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C700	13	CR773	13	R801	3	R883	13	U752	13
C701	3	J150	3	R802	3	R884	13	U753	13
C702	3	J155	3	R803	3	R885	13	U761	13
C731	13	J156	13	R804	3	R886	13	U762	13
C781	13	Q761	13	R805	3	R887	13	U781	13
C800	3	Q771	13	R806	3	R888	13	U831	13
C801	3	Q772	13	R807	3	R889	13	U841	13
C811	3	Q773	13	R808	3	TP701	3	U842	13
C812	3	Q781	13	R809	3	TP702	3	U851	13
C813	3	Q782	13	R810	3	TP811	3	U852	13
C831	13	Q783	13	R811	3	TP812	3	U853	13
C832	13	Q831	13	R812	3	TP813	3	U861	3
C833	13	R701	3	R813	3	TP814	3	U862	3
C841	13	R711	3	R814	3	TP815	3	U871	13
C842	13	R731	13	R815	3	TP821	3	U872	13
C843	13	R732	13	R831	13	TP821	3	U881	13
C852	13	R741	13	R832	13	TP822	3	VR841	13
C861	13	R761	13	R833	13	TP823	3	W101	3
C864	13	R762	13	R834	13	TP824	3	W101	3
C871	13	R771	13	R835	13	TP825	3	W101	13
C872	13	R772	13	R841	13	TP826	3	W110	3
C873	13	R773	13	R842	13	TP826	13	W110	13
C881	13	R774	13	R843	13	TP827	3	W122	3
C882	13	R775	13	R844	13	TP871	13	W122	13
C883	13	R780	13	R861	13	TP881	3	W800	3
C884	13	R781	13	R862	3	U700	3	**W860**	13
C885	13	R782	13	R863	13	U731	13		
CR761	13	R783	13	R871	13	U741	3		
CR771	13	R784	13	R881	13	U742	3		
CR772	13	R800	3	R882	13	U751	3		

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

Component Number
A23 A2 R1234
Assembly Number — *Subassembly Number (if used)* — *Schematic Circuit Number*

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



A13—SIDE BOARD

FRONT PANEL PROCESSOR DIAGRAM 3

ASSEMBLY A13

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C701	4K	1C	R800F	6L	3A	TP701	2B	3B	U742	3F	2G
C702	2B	1B	R800G	8H	3A	TP702	2B	3A	U751	1H	2H
C800	6L	3A	R800H	7H	3A	TP811	1B	2C	U861A	4G	3J
C801	8J	3A	R801	5K	2A	TP812	1B	2C	U861B	5G	3J
C811	7J	3C	R802	7L	2A	TP813	3B	2C	U862A	5F	3J
C812	7J	3C	R803	7L	2A	TP814	1B	2C	U862B	5E	3J
C813	8J	3C	R804	7L	2A	TP815	3B	2C	U862C	5E	3J
			R805	7L	3A	TP821	1B	2D	U862D	5F	3J
J150	2M	2A	R806	6K	3C	TP821	2B	2D			
J150	7A	2A	R807	6L	3C	TP822	2B	2D	W101	1A	2E
J155	4L	2B	R808	7H	3A	TP823	3B	2D	W101	6A	2E
			R809	7H	3A	TP824	2B	2D	W110	1C	3E
R701	5L	2A	R810	4L	3B	TP825	1B	2E	W110	7A	3E
R711	8L	2C	R811	8L	2C	TP826	2B	2E	W122	4A	1L
R800A	6H	3A	R812	6J	2C	TP827	6B	2D	W122	5H	1L
R800B	6L	3A	R813	4L	2C	TP881	2C	3M	W122	8A	1L
R800C	6L	3A	R814	8H	3C				W800	5L	1A
R800D	6L	3A	R815	6J	2A	U700	5K	1B			
R800E	6L	3A	R862	4G	3J	U741	1K	1G			

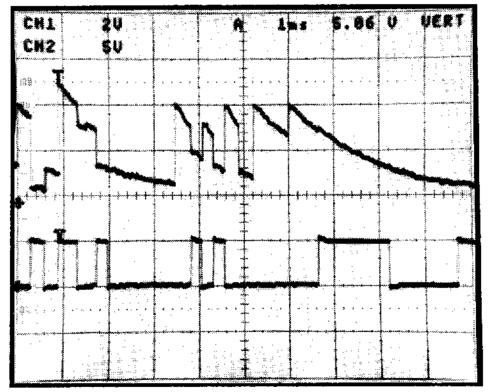
Partial A13 also shown on diagram 13.

CHASSIS MOUNTED PARTS

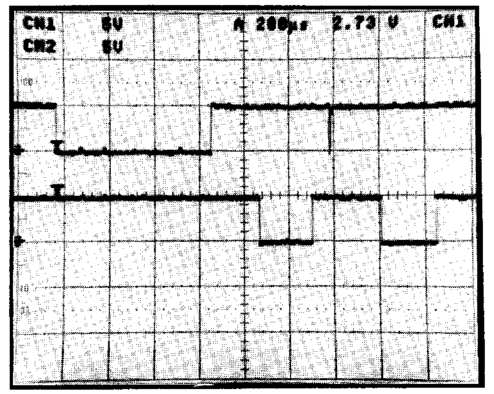
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P150	1C	CHASSIS	P150	6A	CHASSIS	P150	7A	CHASSIS			
P150	2M	CHASSIS	P150	6N	CHASSIS						

WAVEFORMS FOR DIAGRAM 3

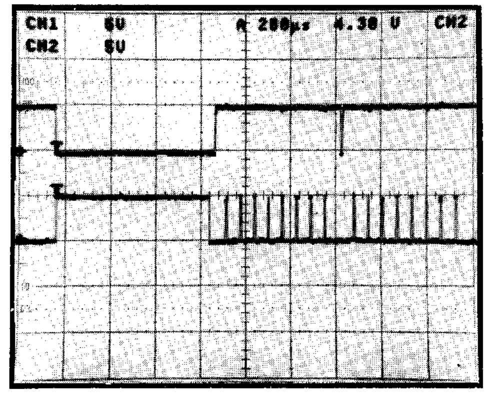
35
36



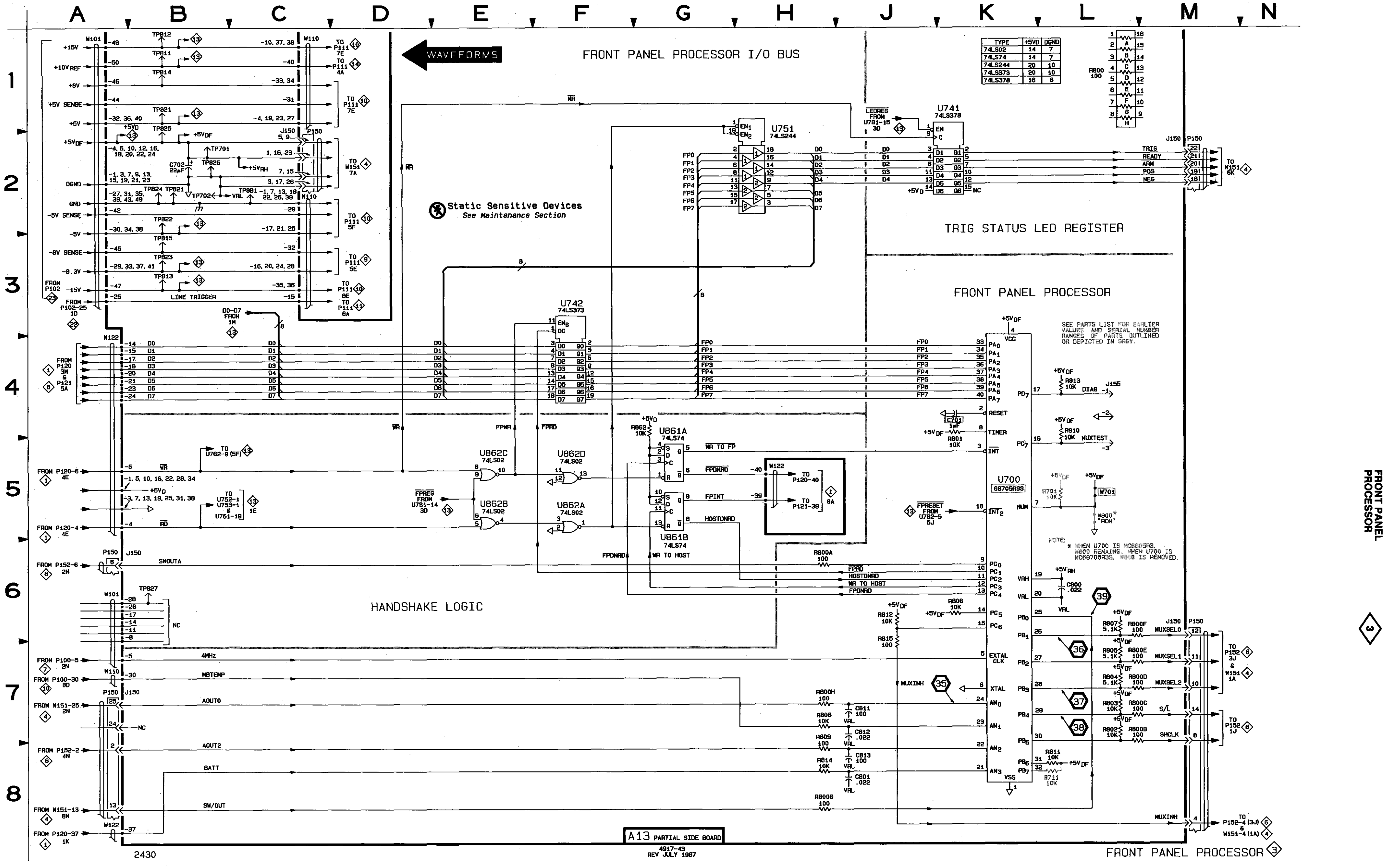
37
39



37
38



4917-74



FRONT PANEL PROCESSOR

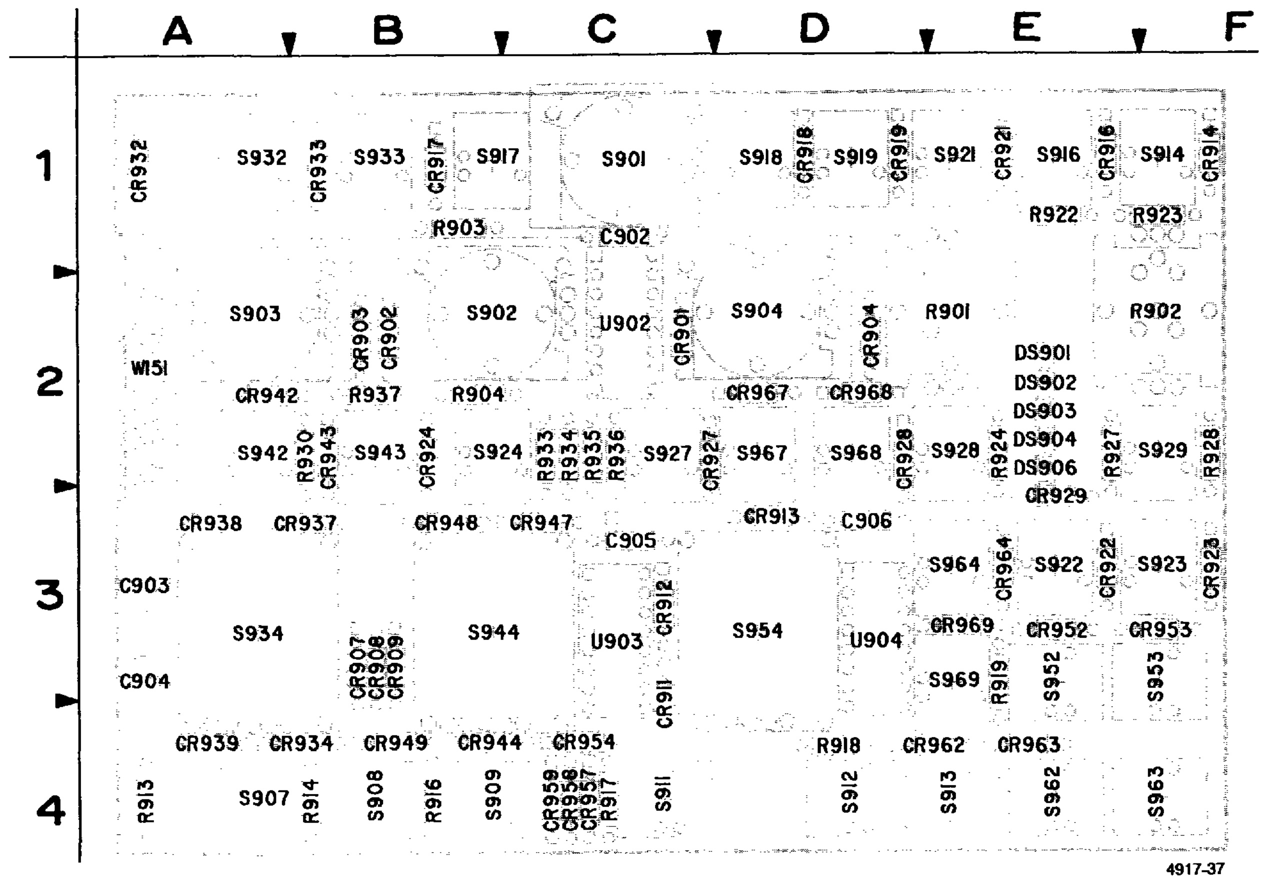
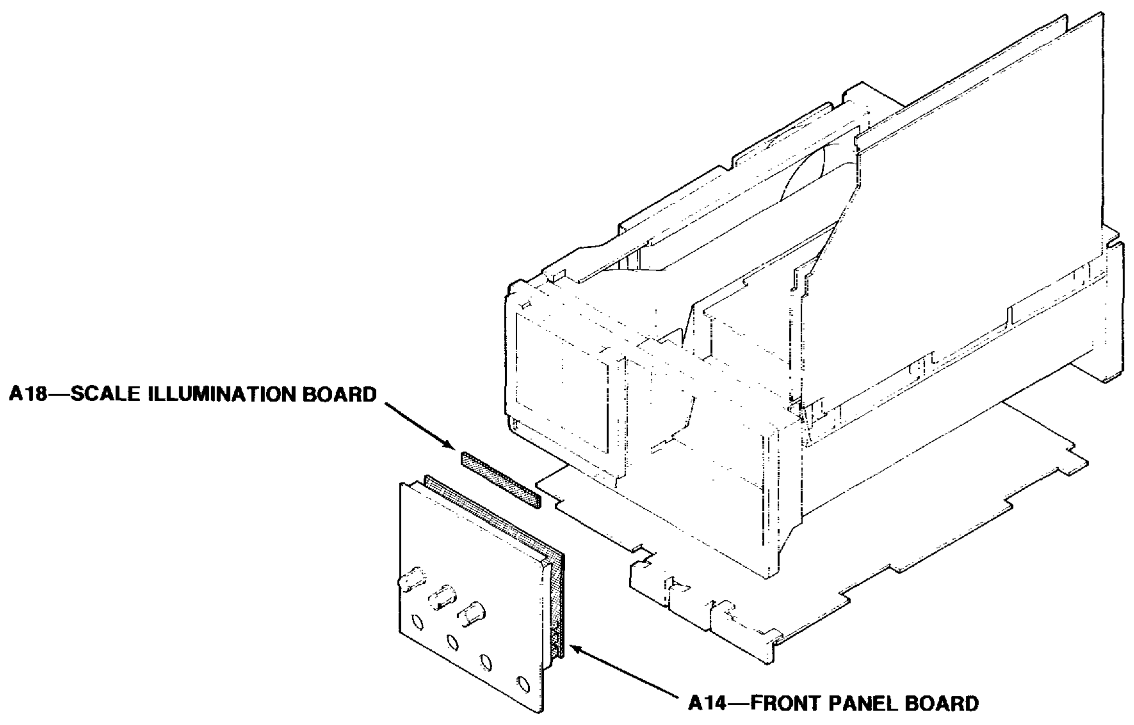


Figure 9-7. A14—Front Panel board.

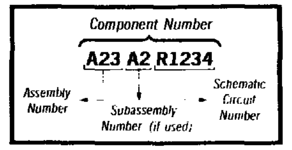


A14—FRONT PANEL BOARD

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C902	4	CR924	4	CR964	4	R924	4	S919	4	U903	4
C903	4	CR927	4	CR967	4	R927	4	S921	4	U904	4
C904	4	CR928	4	CR968	4	R928	4	S922	4	W151	4
C905	4	CR929	4	CR969	4	R930	4	S923	4	W151	4
C906	4	CR932	4	DS901	4	R933	4	S924	4	W151	4
CR901	4	CR933	4	DS902	4	R934	4	S927	4		
CR902	4	CR934	4	DS903	4	R935	4	S928	4		
CR903	4	CR937	4	DS904	4	R936	4	S929	4		
CR904	4	CR938	4	DS906	4	R937	4	S932	4		
CR904	4	CR939	4	R901	4	S901	4	S933	4		
CR907	4	CR942	4	R901	4	S902	4	S934	4		
CR908	4	CR943	4	R902	4	S903	4	S942	4		
CR909	4	CR944	4	R902	4	S903	4	S943	4		
CR911	4	CR947	4	R903	4	S904	4	S944	4		
CR912	4	CR948	4	R904	4	S907	4	S952	4		
CR913	4	CR949	4	R913	4	S908	4	S953	4		
CR914	4	CR952	4	R914	4	S909	4	S954	4		
CR916	4	CR953	4	R916	4	S911	4	S962	4		
CR917	4	CR954	4	R917	4	S912	4	S963	4		
CR918	4	CR957	4	R918	4	S913	4	S964	4		
CR919	4	CR958	4	R919	4	S914	4	S967	4		
CR921	4	CR959	4	R919	4	S916	4	S968	4		
CR922	4	CR962	4	R922	4	S917	4	S969	4		
CR923	4	CR963	4	R923	4	S918	4	U902	4		

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

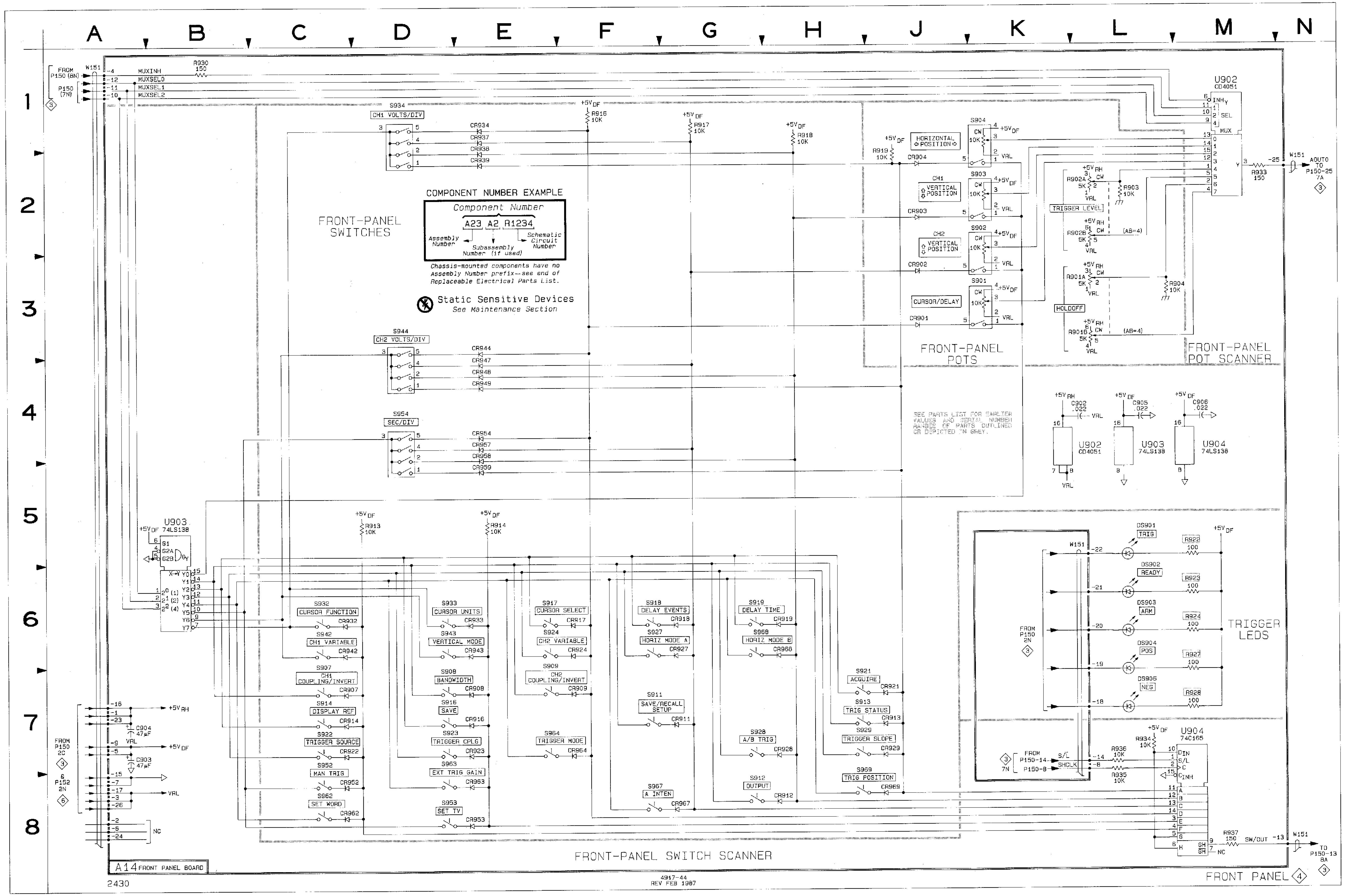


Chassis mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List

FRONT PANEL DIAGRAM 4

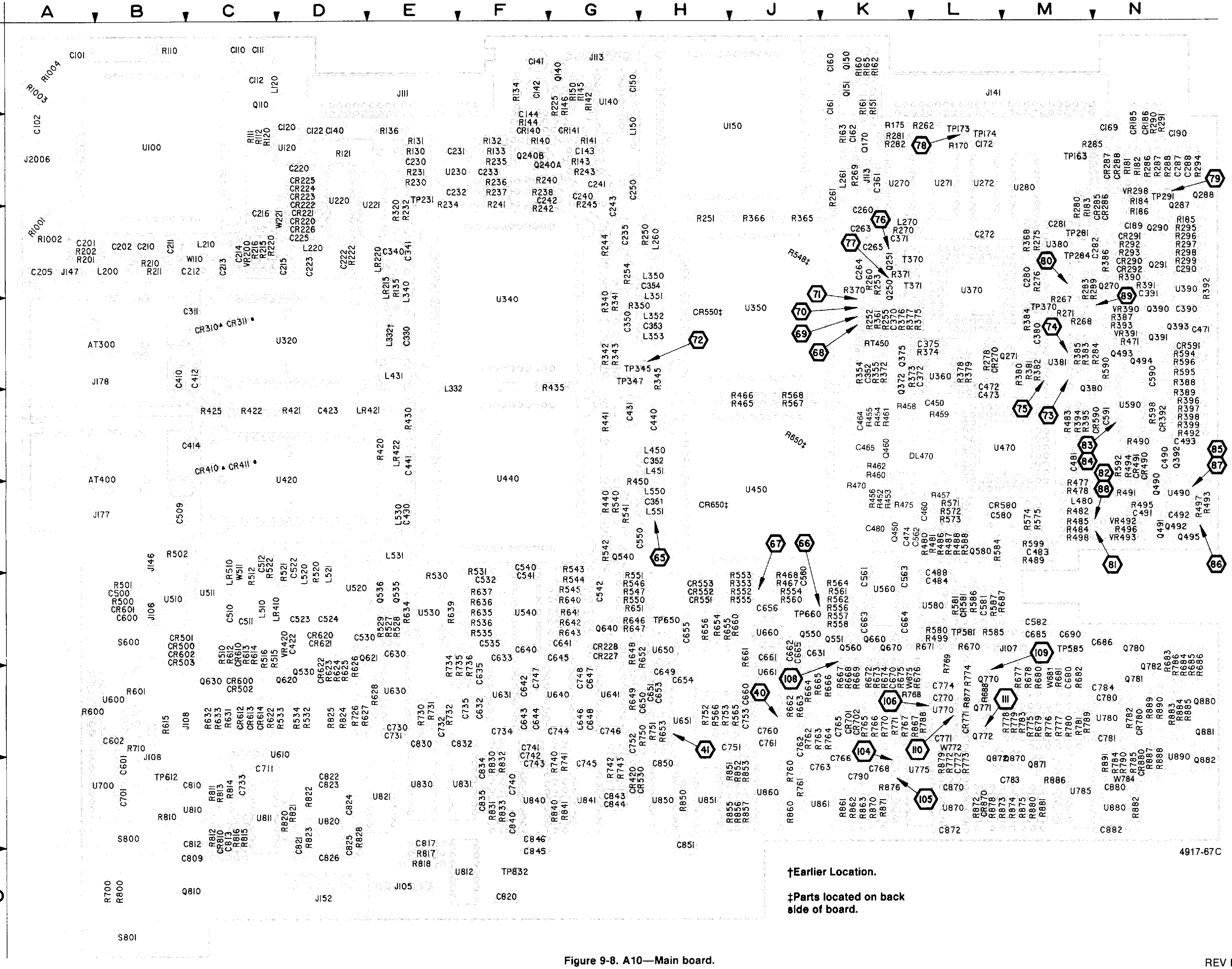
ASSEMBLY A14

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C902	4L	1C	CR938	1E	3A	R913	5D	4A	S918	6F	1D
C903	7A	3A	CR939	2E	4A	R914	5E	4B	S919	6G	1D
C904	7A	3A	CR942	6C	2A	R916	1F	4B	S921	7H	1D
C905	4L	3C	CR943	6E	2B	R917	1G	4C	S922	7C	3E
C906	4M	3D	CR944	3E	4B	R918	1H	4D	S923	7D	3E
			CR947	4E	3C	R919	2J	3E	S924	6E	2B
CR901	3J	2C	CR948	4E	3B	R919	2K	3E	S927	6F	2C
CR902	3J	2B	CR949	4E	4B	R922	5M	1E	S928	7G	2D
CR903	2J	2B	CR952	8C	3E	R923	6M	1F	S929	7H	2E
CR904	2J	2D	CR953	8E	3F	R924	6M	2E	S932	6C	1A
CR904	2K	2D	CR954	4E	4C	R927	6M	2E	S933	6D	1B
CR907	7C	3B	CR957	4E	4C	R928	7M	2F	S934	1D	3A
CR908	7D	3B	CR958	4E	4C	R930	1B	2B	S942	6C	2A
CR909	7F	3B	CR959	5E	4C	R933	2M	2C	S943	6D	2B
CR911	7G	4C	CR962	8C	4E	R934	7L	2C	S944	3D	3B
CR912	8H	3C	CR963	8E	4E	R935	8L	2C	S952	7C	4E
CR913	7J	3D	CR964	7F	3E	R936	7L	2C	S953	8D	4F
CR914	7C	1F	CR967	8G	2D	R937	8M	2B	S954	4D	3D
CR916	7E	1E	CR968	6H	2D				S962	8C	4E
CR917	6F	1B	CR969	8J	3E	S901	3K	1C	S963	7D	4F
CR918	6G	1D				S902	2K	2B	S964	7E	3D
CR919	6H	1D	DS901	5L	2E	S903	2K	2A	S967	8F	2D
CR921	7J	1E	DS902	6L	2E	S903	2K	2A	S968	6G	2D
CR922	7C	3E	DS903	6L	2E	S904	1K	2C	S969	7H	3D
CR923	7E	3F	DS904	6L	2E	S907	6C	4A			
CR924	6F	2B	DS906	7L	2E	S908	7D	4B	U902	1M	2C
CR927	6G	2D				S909	6E	4B	U903	5B	3C
CR928	7H	2D	R901A	3L	2E	S911	7F	4C	U904	7M	3D
CR929	7J	3E	R901B	3L	2E	S912	8G	4D			
CR932	6C	1A	R902A	2L	2F	S913	7H	4E	W151	1A	3A
CR933	6E	1B	R902B	2L	2F	S914	7C	1E	W151	2N	3A
CR934	1E	4B	R903	2L	1B	S916	7D	1E	W151	5L	3A
CR937	1E	3B	R904	3L	2B	S917	6E	1B	W151	8N	3A



FRONT PANEL

4

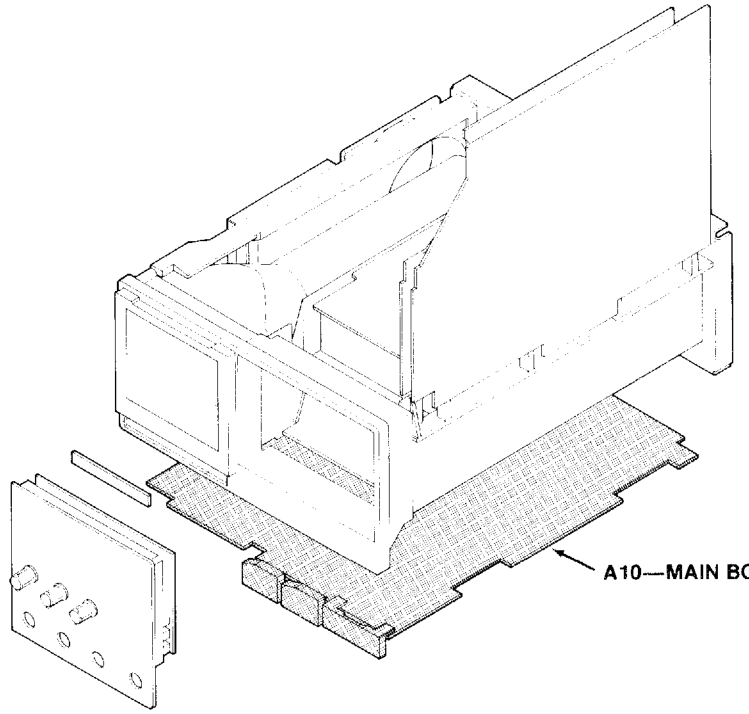


†Earlier Location.

‡Parts located on back side of board.

Figure 9-8. A10—Main board.

REV FEB 1987



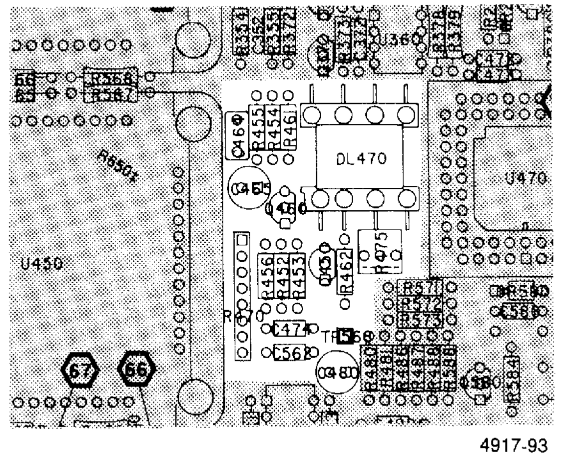
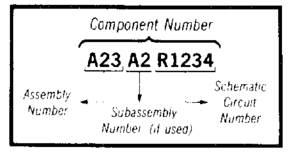


Figure 9-8A. A10-Partial Main board (SN B012726 & below).

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

A10—MAIN BOARD

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
AT300	9	C423	9	C690	6	CR286	11	L150	11	Q782	14
AT400	9	C430	10	C701	6	CR287	5	L200	9	Q810	6
		C431	10	C711	6	CR288	5	L210	9	Q870	14
C101	9	C440	10	C730	6	CR290	12	L220	9	Q871	14
C102	13	C441	10	C731	6	CR291	12	L260	11	Q872	14
C110	10	C450	11	C732	6	CR292	12	L261	10	Q880	14
C111	10	C460	11	C733	6	CR310	9	L270	11	Q881	14
C112	9	C464	10	C734	6	CR311	9	L332	10	Q882	14
C120	9	C465	10	C735	6	CR392	12	L340	10		
C122	9	C471	12	C740	6	CR410	9	L350	10	R110	9
C140	10	C472	11	C741	6	CR411	9	L351	10	R111	9
C141	10	C473	11	C742	6	CR420	5	L352	10	R112	9
C142	10	C474	10	C743	6	CR490	12	L353	10	R120	9
C143	9	C480	10	C744	6	CR491	12	L431	10	R121	9
C144	9	C481	12	C745	6	CR500	9	L450	10	R130	9
C150	11	C483	12	C746	6	CR501	9	L451	10	R131	9
C160	11	C484	11	C747	6	CR502	9	L480	12	R132	9
C161	11	C488	11	C748	6	CR503	9	L510	9	R133	9
C162	11	C490	12	C751	5	CR530	5	L520	9	R134	11
C169	11	C491	12	C752	5	CR550	10	L521	9	R135	9
C172	5	C492	12	C753	5	CR551	10	L530	10	R136	9
C189	11	C493	10	C760	5	CR552	10	L531	10	R140	9
C190	10	C500	9	C761	6	CR553	10	L550	10	R141	9
C201	9	C509	9	C762	14	CR580	11	L551	10	R142	5
C202	9	C510	9	C763	14	CR581	11			R143	9
C205	9	C511	9	C765	14	CR590	12	LR215	9	R144	9
C210	9	C512	9	C766	14	CR591	12	LR220	9	R145	11
C211	9	C522	9	C768	14	CR600	9	LR410	9	R146	11
C212	9	C523	9	C770	14	CR601	9	LR421	9	R150	11
C213	9	C524	9	C771	14	CR602	9	LR422	9	R151	11
C214	9	C530	9	C772	14	CR610	9	LR510	9	R160	11
C215	9	C532	10	C774	14	CR612	6			R161	11
C216	9	C535	10	C780	14	CR613	6	Q110	9	R162	11
C220	9	C540	10	C781	14	CR614	6	Q140	11	R163	11
C222	9	C541	10	C783	14	CR620	9	Q150	11	R165	11
C223	9	C542	10	C784	14	CR621	9	Q151	11	R170	10
C225	9	C550	10	C790	14	CR622	9	Q170	10	R175	10
C230	9	C560	10	C809	6	CR650	10	Q240	9	R181	5
C231	9	C561	14	C810	6	CR701	5	Q250	11	R182	5
C232	9	C562	10	C812	6	CR702	5	Q251	11	R183	11
C233	9	C563	14	C813	6	CR771	14	Q270	11	R184	11
C235	10	C580	11	C817	6	CR780	14	Q271	11	R185	11
C240	9	C581	10	C820	14	CR810	6	Q287	11	R186	11
C241	11	C582	14	C821	6	CR870	14	Q288	11	R201	9
C242	10	C590	12	C822	6	CR880	14	Q290	12	R202	9
C243	10	C591	12	C823	6			Q291	12	R210	9
C250	11	C600	9	C824	6	DL470	11	Q372	10	R211	9
C260	11	C601	6	C825	6			Q375	10	R215	9
C263	10	C602	6	C826	6	J104	6	Q380	12	R216	9
C264	10	C630	6	C830	6	J105	6	Q390	12	R220	9
C265	10	C631	6	C832	6	J105	19	Q391	12	R222	9
C272	11	C632	6	C834	6	J106	6	Q392	12	R225	11
C280	11	C633	6	C835	6	J107	14	Q393	12	R230	9
C281	11	C635	6	C840	6	J108	6	Q450	10	R231	9
C282	12	C640	10	C843	6	J108	19	Q460	10	R232	10
C287	11	C641	10	C844	6	J111	6	Q490	12	R234	9
C288	11	C642	6	C845	6	J111	9	Q491	12	R235	9
C290	12	C643	6	C846	6	J111	10	Q492	12	R236	9
C311	9	C644	6	C850	6	J111	11	Q493	12	R237	9
C330	10	C645	6	C851	14	J111	12	Q494	12	R238	10
C340	10	C646	6	C870	14	J111	13	Q495	12	R240	9
C341	10	C647	5	C872	14	J111	14	Q530	10	R241	9
C350	10	C648	5	C880	14	J113	9	Q535	5	R242	10
C351	10	C649	6	C882	14	J113	11	Q536	5	R243	9
C352	10	C650	5			J114	9	Q540	10	R244	10
C353	10	C651	5	CR140	9	J114	11	Q550	10	R245	10
C354	10	C653	5	CR141	9	J141	5	Q551	10	R250	11
C361	11	C654	5	CR185	5	J141	6	Q560	10	R251	10
C370	10	C655	5	CR186	5	J141	10	Q580	10	R252	11
C370	11	C656	5	CR220	9	J141	11	Q620	9	R253	11
C371	11	C660	5	CR221	9	J141	14	Q621	9	R254	10
C372	10	C661	5	CR222	9	J141	19	Q630	10	R255	11
C375	10	C662	5	CR223	9	J146	9	Q640	10	R260	11
C380	11	C663	14	CR224	9	J147	9	Q660	14	R261	11
C390	12	C664	14	CR225	9	J152	6	Q670	14	R262	11
C391	12	C665	6	CR226	9	J177	9	Q770	14	R267	11
C410	9	C670	14	CR227	5	J178	9	Q771	14	R268	11
C412	9	C680	14	CR228	5	J2006	13	Q772	14	R269	5
C414	9	C685	14	CR270	11			Q780	14	R270	11
C422	9	C686	14	CR285	11	L120	9	Q781	14	R271	11

MORE

MORE

A10—MAIN BOARD (cont)

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
R275	11	R453	10	R561	10	R676	14	R831	6	U270	5
R276	11	R454	10	R562	10	R677	14	R832	6	U271	5
R278	11	R455	10	R564	14	R678	14	R833	6	U272	5
R280	5	R456	10	R565	6	R679	14	R840	6	U280	5
R281	11	R457	11	R566	6	R680	14	R841	6	U320	9
R282	11	R458	11	R567	10	R681	14	R850	5	U340	10
R283	12	R459	11	R568	10	R682	14	R851	5	U350	10
R284	12	R460	11	R571	11	R683	14	R852	5	U360	10
R285	5	R461	10	R572	11	R684	14	R853	5	U370	11
R286	11	R462	11	R573	11	R685	14	R855	5	U380	5
R287	11	R465	10	R574	11	R686	14	R856	5	U380	11
R288	11	R466	10	R575	11	R687	14	R857	5	U381	11
R289	12	R467	10	R580	11	R688	14	R860	5	U390	12
R290	5	R468	10	R581	11	R700	6	R861	14	U420	9
R291	5	R470	10	R584	11	R710	6	R862	14	U440	10
R292	12	R471	12	R585	10	R726	6	R863	14	U450	10
R293	12	R475	11	R586	10	R730	6	R867	14	U470	11
R294	5	R477	12	R587	10	R731	6	R870	14	U490	12
R295	12	R478	12	R588	10	R732	6	R871	14	U510	9
R296	12	R480	11	R590	12	R734	6	R872	14	U511	9
R297	12	R481	11	R592	12	R735	6	R873	14	U520	6
R298	12	R482	12	R594	12	R736	6	R874	14	U520	9
R299	12	R483	12	R595	12	R740	6	R875	14	U530	5
R320	9	R484	12	R596	12	R741	6	R876	14	U540	10
R340	10	R485	12	R598	12	R742	10	R877	14	U560	14
R341	10	R486	10	R599	12	R743	10	R878	14	U580	10
R342	10	R487	10	R600	6	R750	5	R879	14	U580	11
R343	10	R488	10	R601	6	R751	5	R880	14	U590	12
R345	10	R489	12	R612	9	R752	5	R881	14	U600	6
R350	10	R490	12	R613	9	R753	5	R882	14	U610	6
R352	10	R491	12	R614	9	R760	5	R883	14	U630	6
R353	10	R492	12	R615	6	R761	5	R884	14	U631	6
R354	10	R493	12	R622	9	R762	14	R885	14	U640	6
R355	10	R494	12	R623	9	R763	14	R886	14	U641	5
R361	11	R495	12	R624	9	R764	14	R887	14	U650	5
R365	10	R496	12	R625	9	R765	14	R888	14	U651	5
R366	10	R497	12	R626	6	R766	14	R889	14	U660	5
R368	11	R498	12	R627	6	R767	14	R890	14	U661	5
R370	10	R499	11	R628	6	R768	14	R891	14	U661	6
R371	11	R500	9	R631	10	R769	14	R1001	9	U700	6
R372	10	R501	9	R632	10	R770	14	R1002	9	U770	14
R373	10	R502	9	R633	10	R771	14	R1003	9	U775	14
R374	10	R510	9	R634	6	R772	14	R1004	9	U780	14
R375	10	R512	9	R635	10	R773	14			U785	14
R376	10	R515	9	R636	10	R774	14	RT450	10	U810	6
R377	10	R516	9	R637	10	R775	14			U811	6
R378	10	R520	9	R639	6	R776	14	S600	6	U812	6
R379	10	R521	9	R640	10	R777	14	S800	6	U820	6
R380	11	R522	5	R641	10	R778	14	S801	6	U821	6
R381	11	R527	5	R642	10	R779	14			U830	6
R382	11	R528	5	R643	10	R780	14	T370	11	U831	6
R383	11	R529	5	R646	10	R781	14	T371	11	U840	6
R384	11	R530	9	R647	10	R782	14			U841	6
R385	11	R531	5	R648	5	R783	14	TP163	11	U850	5
R386	12	R532	10	R649	5	R784	14	TP173	11	U851	5
R387	12	R533	10	R650	10	R785	14	TP174	11	U860	5
R388	12	R534	10	R651	10	R786	14	TP231	11	U861	14
R389	12	R535	10	R652	5	R788	14	TP281	10	U870	14
R390	12	R536	10	R653	5	R789	14	TP284	11	U880	14
R391	12	R540	10	R654	5	R790	14	TP291	11	U890	14
R392	12	R541	10	R655	5	R800	6	TP345	10		
R393	12	R542	10	R656	5	R810	6	TP347	10	VR200	9
R394	12	R543	10	R660	5	R811	6	TP370	11	VR298	11
R395	12	R544	10	R661	5	R812	6	TP568	11	VR390	12
R396	12	R545	10	R662	5	R813	6	TP581	11	VR391	12
R397	12	R546	10	R663	5	R814	6	TP585	11	VR420	9
R398	12	R547	10	R664	5	R815	6	TP612	11	VR492	12
R399	12	R548	10	R665	5	R816	6	TP650	5	VR493	12
R420	9	R550	14	R666	5	R817	6	TP660	5		
R421	9	R551	10	R667	14	R818	6	TP832	11	W110	9
R422	5	R552	10	R668	14	R820	6			W221	9
R425	9	R553	10	R669	14	R821	6	U100	9	W511	9
R430	10	R554	10	R670	14	R822	6	U120	9	W675	14
R435	10	R555	5	R671	14	R823	6	U140	5	W681	14
R440	10	R556	10	R672	14	R824	6	U150	11	W772	14
R441	10	R557	10	R673	14	R825	6	U220	9	W784	14
R450	10	R558	10	R674	14	R828	6	U221	9		
R452	10	R560	10	R675	14	R830	6	U230	9		

SYSTEM DAC & ACQUISITION CONTROL REGISTERS DIAGRAM 5

ASSEMBLY A10

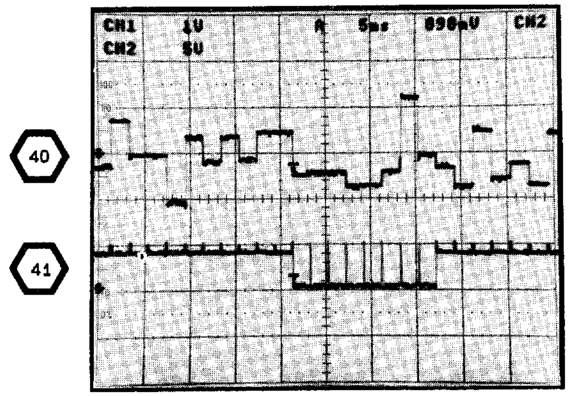
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C172	7D	2L	R181	3L	2N	R850	5E	9H
C647	6L	8G	R182	3M	2N	R851	8H	9H
C648	5M	8G	R269	1G	2K	R852	8H	9J
C650	7L	8G	R280	4G	3M	R853	8H	9J
C651	7L	8H	R285	3F	2N	R855	8G	9H
C653	6L	8H	R290	4G	2N	R856	8G	9J
C654	7D	8H	R291	3G	2N	R857	8G	9J
C655	7K	7H	R294	4G	2N	R860	5F	9J
C656	5J	7J	R422	2J	5C			
C660	4M	8J	R522	3J	6C	TP650	7K	7H
C661	8D	7J	R527	2J	7E	TP660	5J	7J
C662	5J	7J	R528	2J	7E			
C751	6F	8J	R529	3J	7E	U140	2L	1G
C752	6L	8G	R531	2F	7F	U270	1G	2K
C753	8L	8J	R555	7K	7J	U271	1D	2L
C760	7D	8J	R648	7M	7G	U272	3D	2L
			R649	7M	8G	U280A	2C	2M
CR185	3L	2N	R652	7M	7G	U280B	5E	2M
CR186	3L	2N	R653	6M	8H	U280C	2C	2M
CR227	7M	7G	R654	7K	7H	U280D	4C	2M
CR228	7M	7G	R655	5J	7H	U380A	3M	3M
CR287	3L	2N	R656	5J	7H	U530	2G	7E
CR288	3L	2N	R660	5J	7J	U641A	6M	8G
CR420	6M	9G	R661	4M	7J	U641B	5M	8G
CR530	7M	9G	R662	8M	8J	U641C	6M	8G
CR701	6K	8K	R663	6J	8J	U641D	7M	8G
CR702	6K	8K	R664	6H	8J	U650	7K	7H
			R665	7J	8J	U651	4K	8H
J141	1A	2L	R666	7J	8K	U660	5J	7J
J141	3M	2L	R750	6M	8G	U661A	4M	8J
			R751	6M	8H	U661B	8M	8J
Q535	2J	7E	R752	8M	8H	U661C	6J	8J
Q536	2J	7E	R753	4M	8H	U850	5E	9H
			R760	5G	9J	U851	7E	9H
R142	1K	1G	R761	6F	9J	U860	5G	9J

Partial A10 also shown on diagrams 6, 9, 10, 11, 12, 13, 14 and 19.

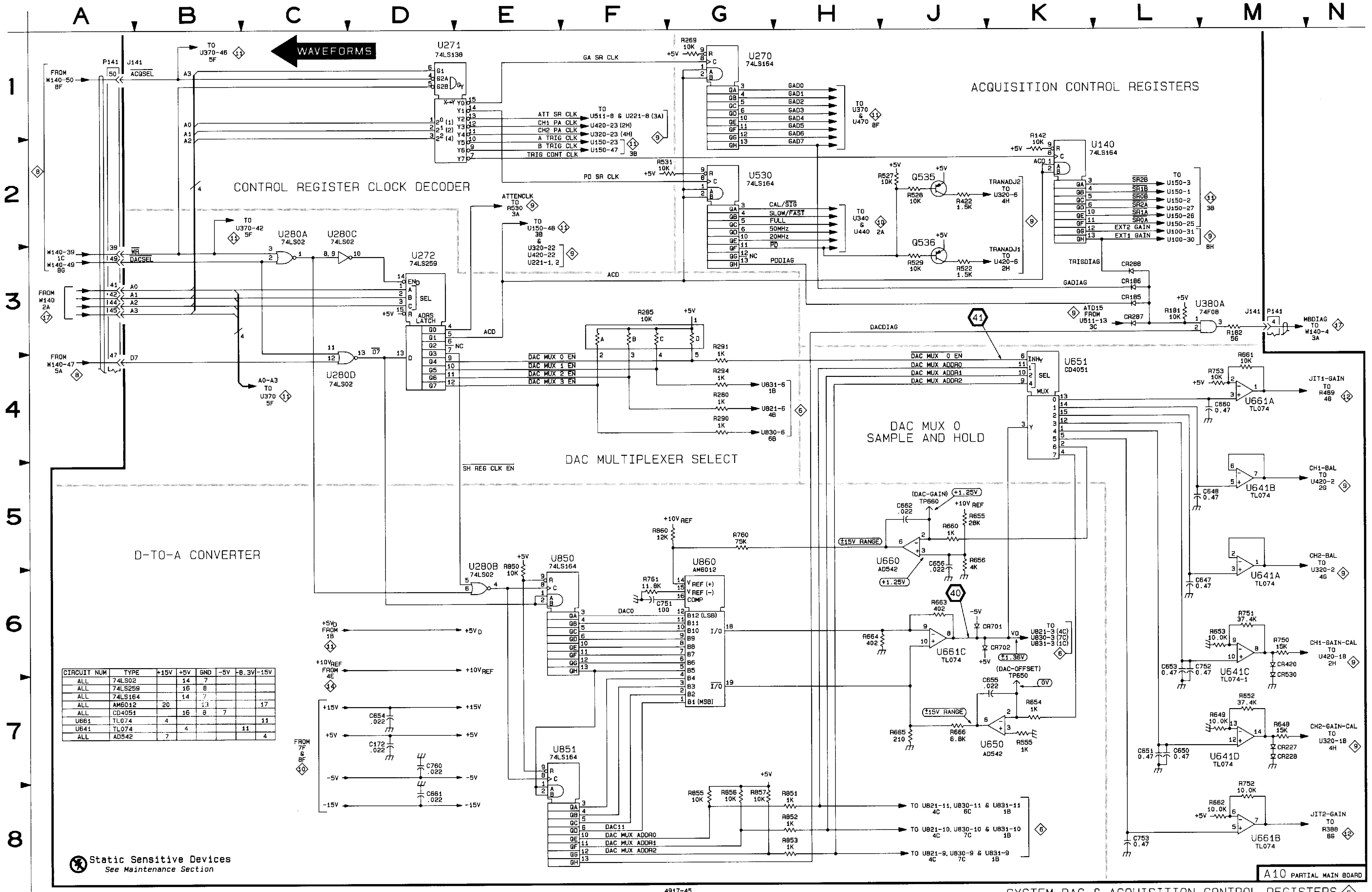
CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P141	1A	CHASSIS	P141	3M	CHASSIS			

WAVEFORMS FOR DIAGRAM 5



4917-75



SYSTEM DAC (CONT) & AUXILIARY FRONT PANEL DIAGRAM 6

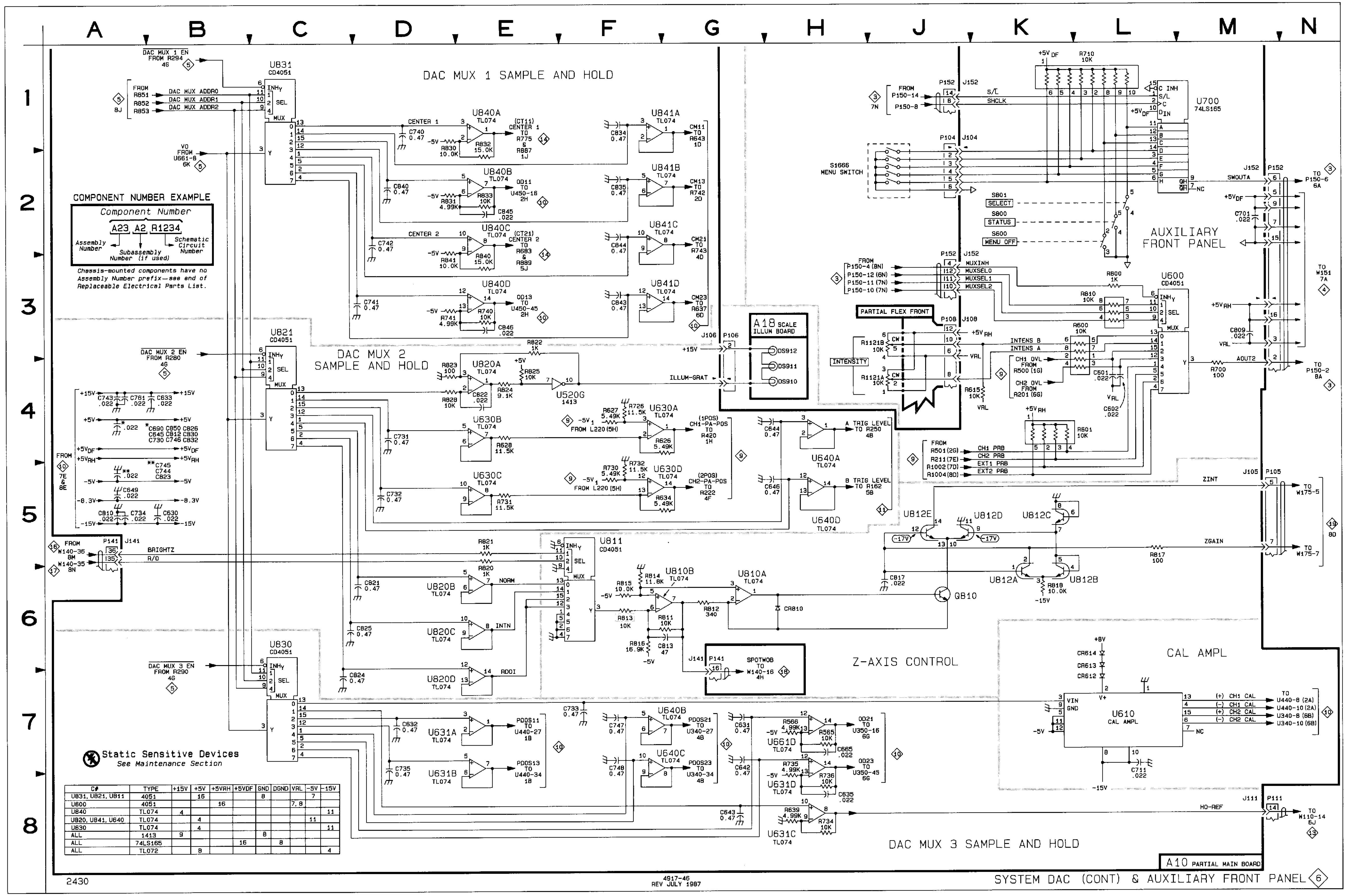
ASSEMBLY A10

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C601	4L	9B	C824	7C	9D	R639	8H	7E	U600	3L	8B
C602	4L	8B	C825	6D	9D	R700	4M	10B	U610	7L	8C
C630	5B	7E	C826	4B	10D	R710	1L	8B	U630A	4G	8E
C631	7G	7J	C830	4B	8E	R726	4F	8D	U630B	4E	8E
C632	7D	8F	C832	4B	8F	R730	5F	8E	U630C	5E	8E
C633	4B	7F	C834	1F	9F	R731	5E	8E	U630D	5G	8E
C635	8H	8F	C835	2F	9F	R732	5F	8E	U631A	7D	8F
C642	7G	8F	C840	2D	9F	R734	8H	8E	U631B	7D	8F
C643	8G	8F	C843	3F	9G	R735	7H	8E	U631C	8H	8F
C644	4H	8F	C844	2F	9G	R736	8H	8F	U631D	8H	8F
C645	4B	7G	C845	2E	10F	R740	3E	9G	U640A	4H	8G
C646	5H	8G	C846	3E	9F	R741	3D	9G	U640B	7G	8G
C649	5A	8H	C850	4B	9H	R800	3L	10B	U640C	7G	8G
C665	7H	7J				R810	3L	9B	U640D	5H	8G
C690	4B	7M	CR612	7L	8C	R811	6G	9C	U661D	7H	8J
C701	2M	9B	CR613	6L	8C	R812	6G	9C	U700	1M	9B
C711	7L	9C	CR614	6L	8C	R813	6F	9C	U810A	6G	9C
C730	4B	8E	CR810	6H	9C	R814	6F	9C	U810B	6G	9C
C731	4D	8E				R815	6F	9C	U811	5F	9C
C732	5D	8E	J104	1J	8B	R816	6F	9C	U812A	6K	10F
C733	7F	9C	J105	5M	10E	R817	5L	10E	U812B	6L	10F
C734	5A	8F	J106	3G	7B	R818	6K	10E	U812C	5K	10F
C735	7D	8F	J108	3J	8B	R820	6E	9D	U812D	5K	10F
C740	1D	9F	J111	8M	1E	R821	5E	9D	U812E	5J	10F
C741	3D	8F	J141	5A	2L	R822	3E	9D	U820A	4E	9D
C742	2D	9F	J141	6G	2L	R823	4D	9D	U820B	6D	9D
C743	4A	9F	J152	1J	10D	R824	4E	8D	U820C	6D	9D
C744	5B	8G	J152	2M	10D	R825	4E	8D	U820D	7D	9D
C745	5B	9G	J152	3J	10D	R828	4D	9D	U821	3C	9E
C746	4B	8G				R830	1D	9F	U830	6C	9E
C747	7F	8F	Q810	6J	10C	R831	2D	9F	U831	1C	9F
C748	7F	8G				R832	1E	9F	U840A	1E	9F
C761	4A	8J	R565	7H	8J	R833	2E	9F	U840B	2E	9F
C809	3M	10C	R566	7H	8H	R840	3E	9G	U840C	2E	9F
C810	5A	9C	R600	3L	8A	R841	3D	9G	U840D	3E	9F
C812	4B	9C	R601	4L	8B				U841A	1G	9G
C813	6G	9C	R615	4K	8B	S600	2K	7B	U841B	2G	9G
C817	6J	9E	R626	4G	8D	S800	2K	9B	U841C	2G	9G
C821	6D	9D	R627	4F	8D	S801	2K	10B	U841D	3G	9G
C822	4E	9D	R628	4E	8E						
C823	5B	9D	R634	5G	7E	U520G	4F	7D			

Partial A10 also shown on diagrams 5, 9, 10, 11, 12, 13, 14 and 19.

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P104	1J	CHASSIS	P141	5A	CHASSIS	P152	2M	CHASSIS	S1666	2H	CHASSIS
P105	5M	CHASSIS	P141	6G	CHASSIS						
P106	3G	CHASSIS	P152	1J	CHASSIS	R1121A	4J	CHASSIS			
P111	8M	CHASSIS	P152	2J	CHASSIS	R1121B	2J	CHASSIS			



SYSTEM DAC (cont) & AUX. FRONT PANEL

6

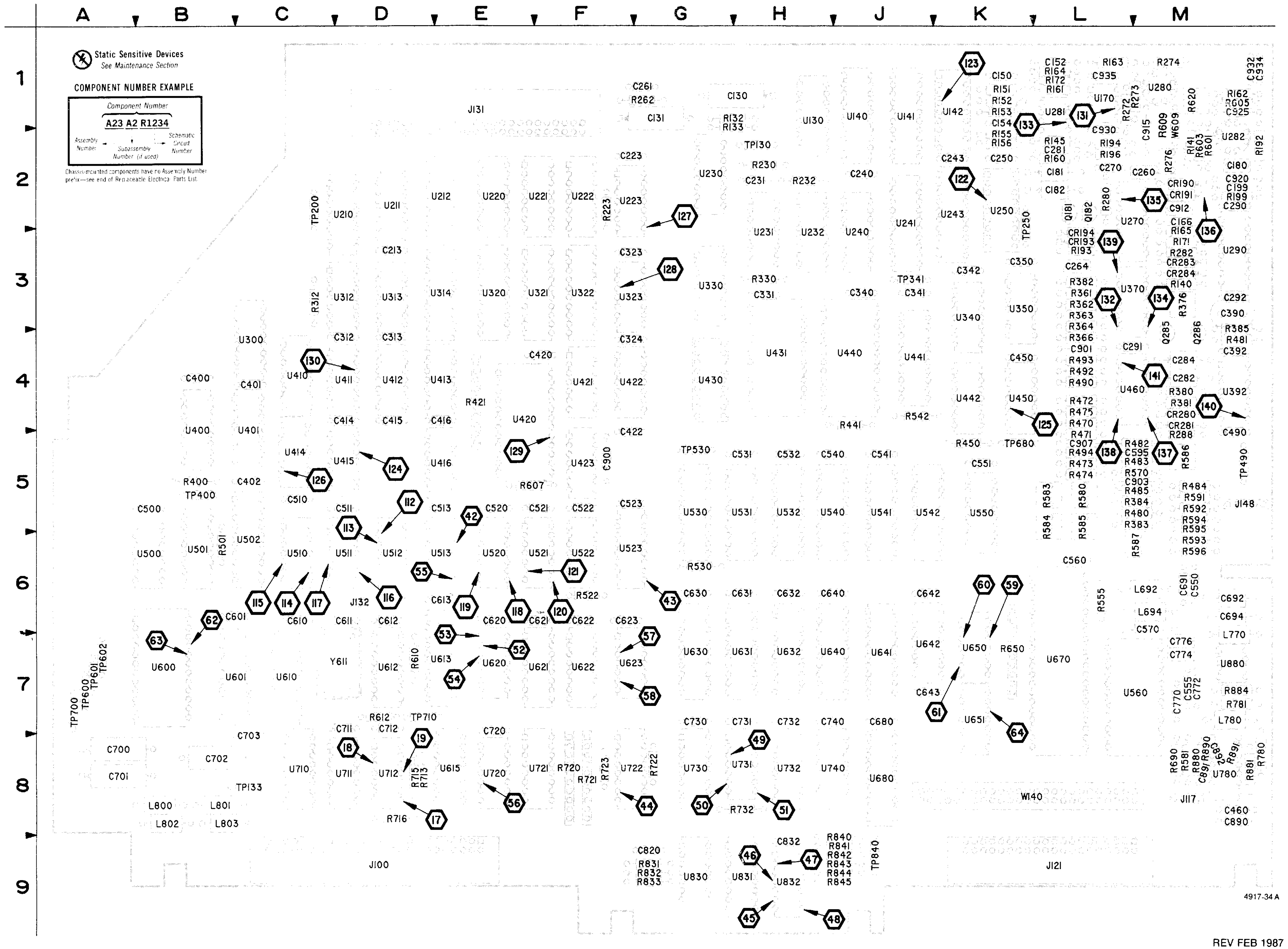


Figure 9-9. A11-Timebase/Display board.

A11—TIME BASE/DISPLAY BOARD

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C130	18	C620	15	L694	15	R474	18	TP250	18	U450	17
C131	18	C621	15	L770	15	R475	18	TP341	18	U460	18
C150	16	C622	15	L780	15	R480	18	TP400	15	U500	8
C152	18	C623	15	L800	18	R481	18	TP490	18	U501	8
C154	18	C630	15	L801	18	R482	18	TP530	15	U502	8
C166	18	C631	15	L802	18	R483	18	TP600	18	U510	15
C180	18	C632	15	L803	18	R484	18	TP601	15	U511	15
C181	18	C640	15			R485	18	TP602	18	U512	8
C182	18	C642	15	Q181	18	R490	18	TP680	18	U512	15
C199	18	C643	15	Q182	18	R492	18	TP700	18	U513	7
C213	15	C680	15	Q285	18	R493	18	TP710	18	U520	15
C223	15	C691	15	Q286	18	R494	18	TP840	18	U521	15
C231	15	C692	15			R501	8			U522	7
C240	15	C694	15	R132	17	R522	8	U130	16	U522	8
C243	15	C695	15	R133	17	R530	7	U140	16	U523	7
C250	16	C700	18	R140	18	R542	18	U141	16	U530	17
C260	18	C701	18	R141	18	R555	15	U142	16	U531	17
C261	15	C702	18	R145	18	R570	18	U170	18	U532	17
C264	18	C703	15	R151	16	R580	18	U210	17	U540	17
C270	15	C711	15	R152	16	R581	15	U211	17	U541	17
C281	18	C712	15	R153	18	R583	18	U212	17	U542	17
C282	18	C720	15	R155	16	R584	18	U220	17	U550	17
C284	18	C730	15	R156	16	R585	18	U221	17	U560	15
C290	15	C731	15	R160	18	R586	18	U222	17	U600	8
C291	15	C732	15	R161	18	R587	18	U223	17	U601	8
C292	15	C740	15	R162	18	R591	18	U230	17	U610	8
C312	15	C770	15	R163	18	R592	18	U231	17	U612	7
C313	15	C772	15	R164	18	R593	18	U232	17	U613	8
C323	15	C774	15	R165	18	R594	18	U240	16	U615	7
C324	15	C776	15	R171	18	R595	18	U241	16	U620	7
C331	15	C820	15	R172	18	R596	18	U243	16	U620	8
C340	15	C832	15	R192	18	R601	18	U250	16	U621	7
C341	15	C890	15	R193	18	R603	18	U270	18	U622	7
C342	15	C891	15	R194	18	R605	18	U280	18	U623	7
C350	15	C892	15	R196	18	R607	18	U281	18	U630	15
C390	18	C900	18	R199	18	R609	18	U282	18	U631	15
C392	15	C901	18	R223	17	R610	7	U290	18	U632	15
C400	15	C903	18	R230	17	R612	7	U300	8	U640	15
C401	15	C907	18	R232	17	R620	18	U312	17	U641	8
C402	15	C912	18	R262	18	R650	7	U313	17	U642	7
C414	15	C915	18	R272	18	R650	8	U314	16	U650	8
C415	15	C920	18	R273	18	R650	15	U320	16	U650	15
C416	15	C925	18	R274	18	R690	15	U321	16	U651	8
C420	15	C930	18	R276	18	R713	7	U322	16	U670	8
C422	15	C932	18	R280	18	R715	7	U323	16	U680	8
C450	15	C934	18	R282	18	R716	7	U323	17	U710	7
C460	15	C935	18	R288	18	R720	7	U330	17	U711	7
C490	15			R312	17	R720	8	U340	17	U712	7
C500	15	CR190	18	R330	17	R720	15	U350	16	U720	7
C510	15	CR191	18	R361	18	R721	7	U350	17	U721	7
C511	15	CR193	18	R362	18	R722	8	U370	18	U722	7
C513	15	CR194	18	R363	18	R723	7	U392	18	U722	8
C520	15	CR280	18	R364	18	R732	17	U400	8	U730	7
C521	15	CR281	18	R366	18	R780	15	U401	8	U731	7
C522	15	CR283	18	R376	18	R781	15	U410	17	U731	8
C523	15	CR284	18	R380	18	R831	7	U411	17	U732	15
C531	15			R381	18	R832	7	U412	17	U740	15
C532	15	J100	7	R382	18	R833	7	U413	16	U780	15
C540	15	J100	8	R383	18	R840	7	U413	17	U830	7
C541	15	J100	17	R384	18	R841	7	U414	17	U831	7
C550	15	J100	18	R385	18	R842	7	U415	17	U832	7
C551	15	J117	15	R400	8	R843	7	U416	17	U880	15
C555	15	J121	8	R421	7	R844	7	U420	17		
C560	15	J121	17	R421	8	R845	7	U421	16	W140	7
C570	15	J121	18	R421	15	R880	15	U422	16	W140	8
C571	15	J131	8	R421	17	R881	15	U423	16	W140	16
C572	15	J131	16	R421	18	R884	15	U423	17	W140	17
C595	18	J131	17	R441	18	R890	15	U430	16	W140	18
C601	15	J131	18	R450	16	R891	15	U431	16	W609	18
C610	15	J132	7	R470	18			U440	16		
C611	15	J148	18	R471	18	TP130	18	U441	16	Y611	7
C612	15			R472	18	TP133	7	U442	17		
C613	15	L692	15	R473	18	TP200	18	U450	16		

A11—TIME BASE/ DISPLAY BOARD

FIG. 9-9

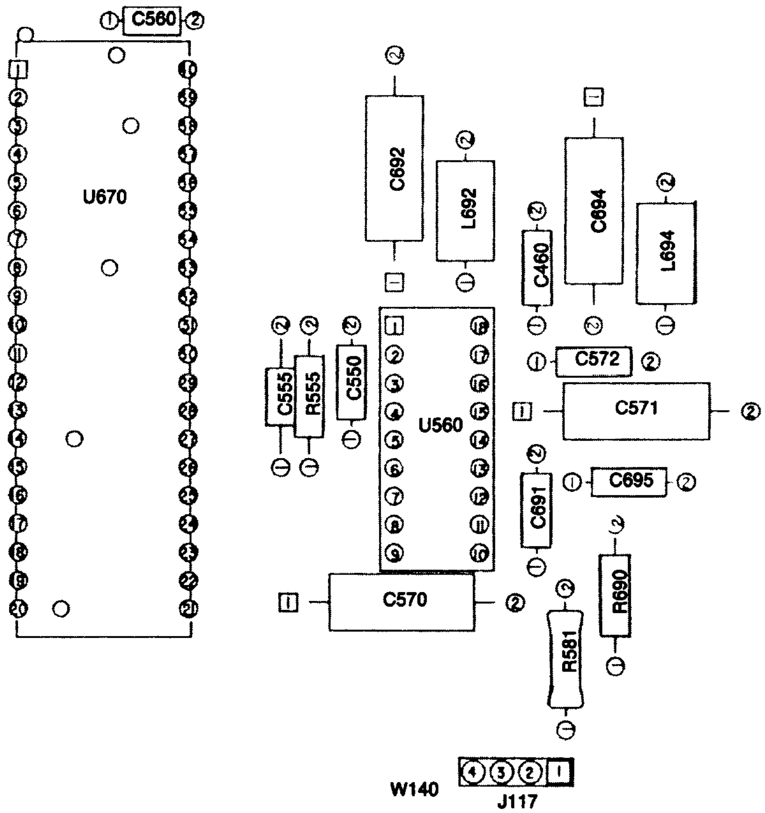
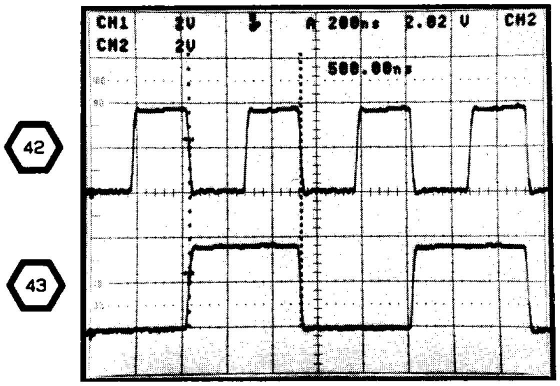
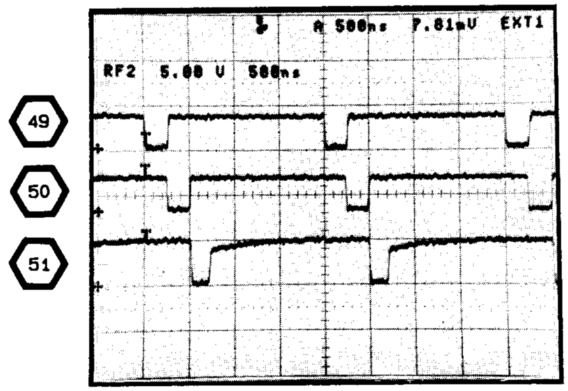
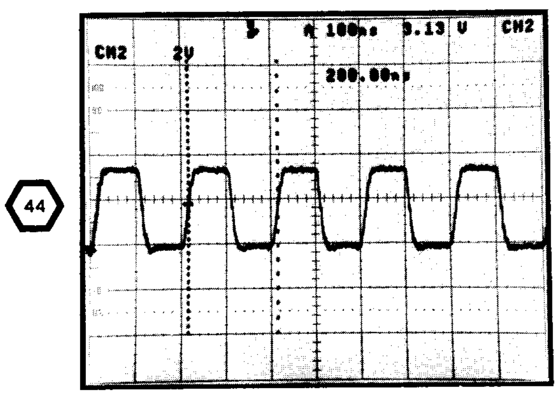


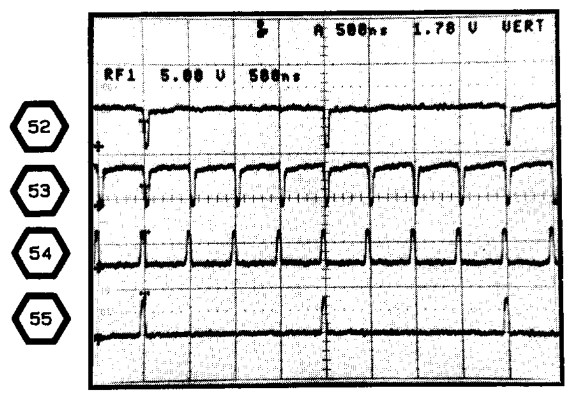
Figure 9-9A. A11-Partial Timebase/Display board (SN B011145 & Below).

WAVEFORMS FOR DIAGRAM 7

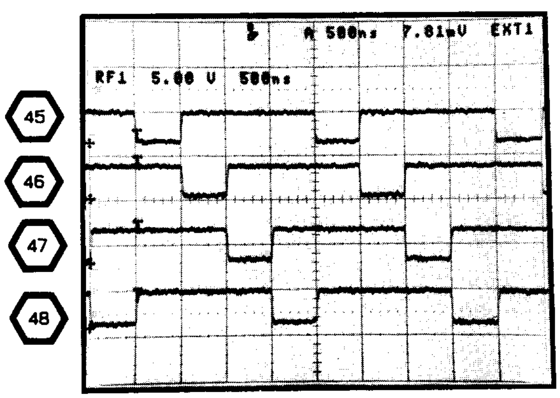




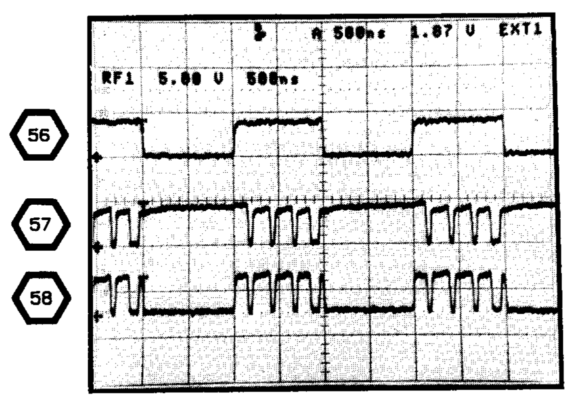




TEST SCOPE TRIGGERED ON
U832 PIN 6 (EITHER CH2 OR EXT)



TEST SCOPE TRIGGERED
ON U623 PIN 5



4917-76

SYSTEM CLOCKS DIAGRAM 7

ASSEMBLY A11

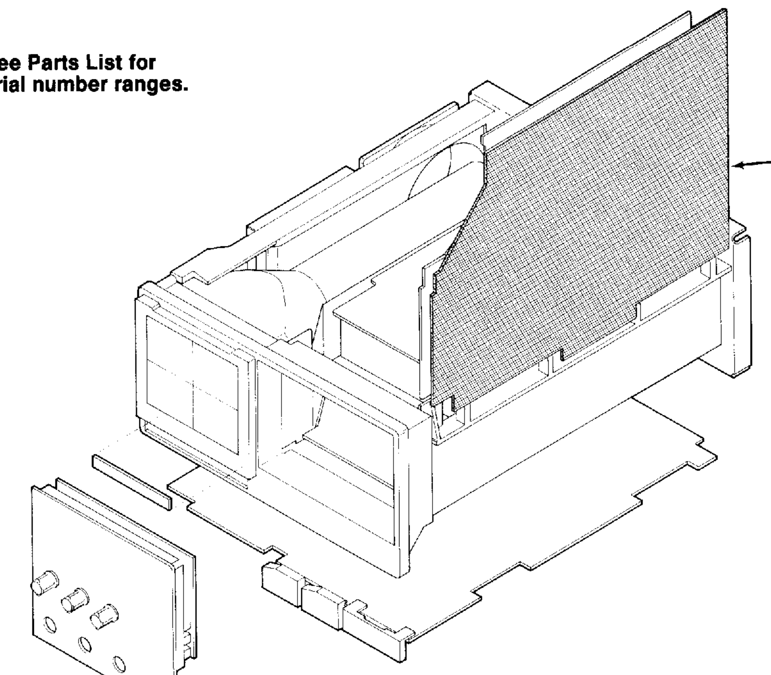
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J100	2M	9D	R833	3L	9G	U710	6B	8C
J100	7E	9D	R840	5M	9J	U711A	8B	8D
J132	2A	6D	R841	7L	9J	U711B	8B	8D
			R842	7L	9J	U711C	7B	8D
R421B	5F	4E	R843	8L	9J	U711D	5K	8D
R421D	1G	4E	R844	5M	9J	U712A	7D	8D
R530	1L	6G	R845	4M	9J	U712B	8C	8D
R610	2B	7D				U712C	7D	8D
R612*	2C	7D	TP133	7C	8C	U712D	8D	8D
R650E	4J	7K				U720A	5F	8E
R713	8E	8D	U513A	2A	6E	U720B	5L	8E
R715	7E	8D	U513B	4B	6E	U721	3H	8F
R716	7E	8D	U513C*	2C	6E	U722A	1K	8F
R720A	1D	8F	U513D	4K	6E	U730	7J	8G
R720B	5G	8F	U513E	6H	6E	U731A	7L	8H
R720D	7D	8F	U513F	2F	6E	U731B	7L	8H
R720E	8D	8F	U522A	4H	6F	U731C	8L	8H
R720F	5E	8F	U522B	1F	6F	U830	6J	9G
R720G	7D	8F	U523A	2G	6F	U831	4L	9H
R720H	5K	8F	U523B	1G	6F	U832A	5M	9H
R720I	6B	8F	U612A	2B	7D	U832B	5M	9H
R721A	7J	8F	U612B	3B	7D	U832C	4M	9H
R721B	2G	8F	U615A	3C	8E	U832D	4M	9H
R721C	6E	8F	U615B	3D	8E	U832E	3L	9H
R721D	2B	8F	U620A	4K	7E	U832F	2L	9H
R721E	3G	8F	U620B	6F	7E			
R721F	4H	8F	U620C	2D	7E	W140	1N	8K
R721G	4L	8F	U621	5H	7F	W140	4N	8K
R721H	7K	8F	U622	1E	7F	W140	5A	8K
R721I	7J	8F	U623A	4G	7F			
R723	2L	8F	U623B	5G	7F	Y611	2A	7C
R831	5M	9G	U623C	1F	7F			
R832	2L	9G	U642	4J	7J			

Partial A11 also shown on diagrams 8, 15, 16, 17 and 18.

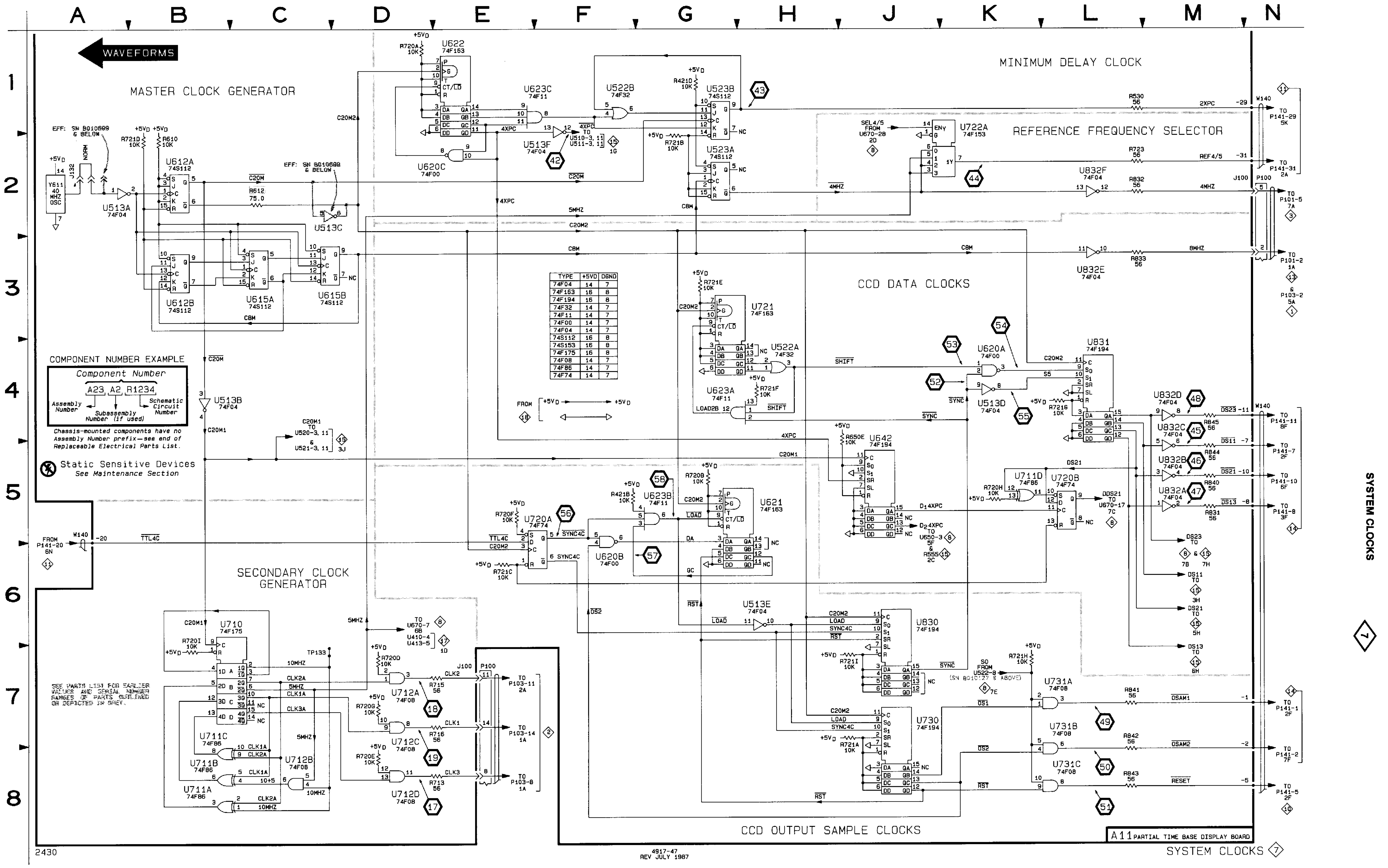
CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P100	2N	CHASSIS	P100	7E	CHASSIS			

***See Parts List for serial number ranges.**

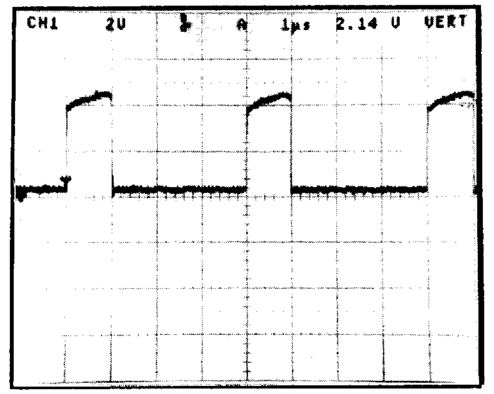


A11—TIME BASE/DISPLAY BOARD

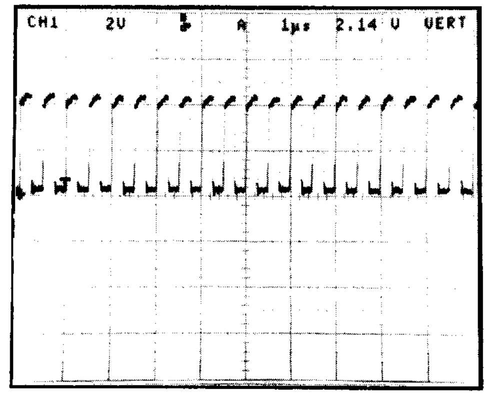


WAVEFORMS FOR DIAGRAM 8

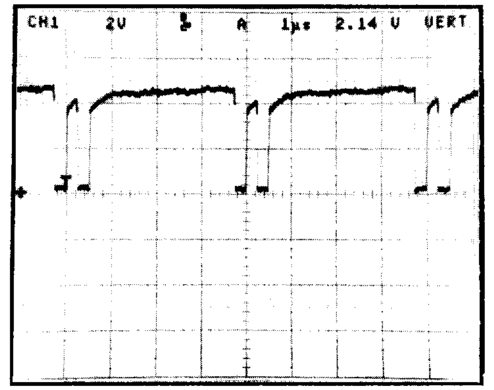
59



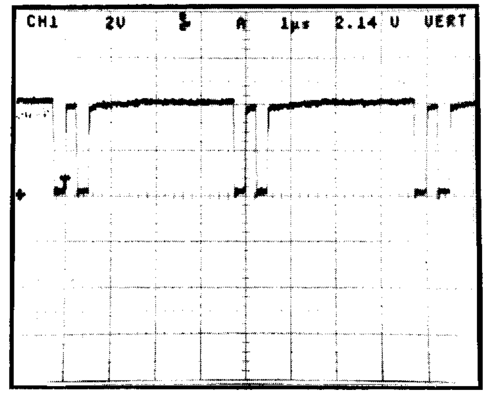
60



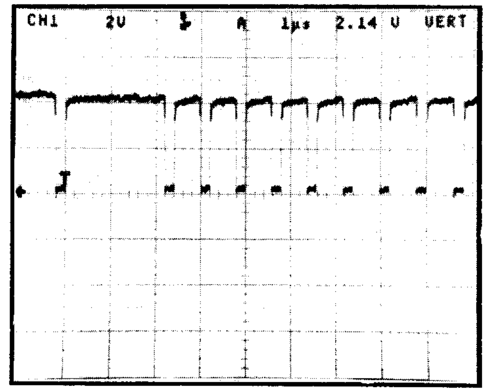
61



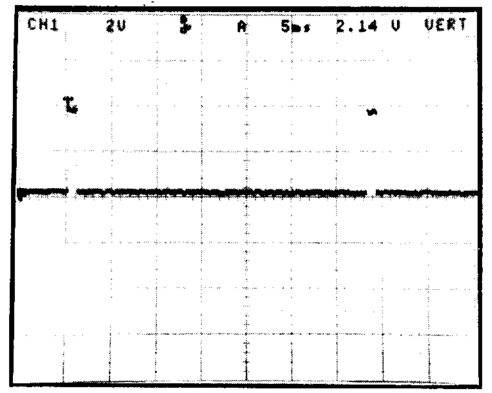
62



63



64



4917-77

TIME BASE CONTROLLER & ACQUISITION MEMORY DIAGRAM 8

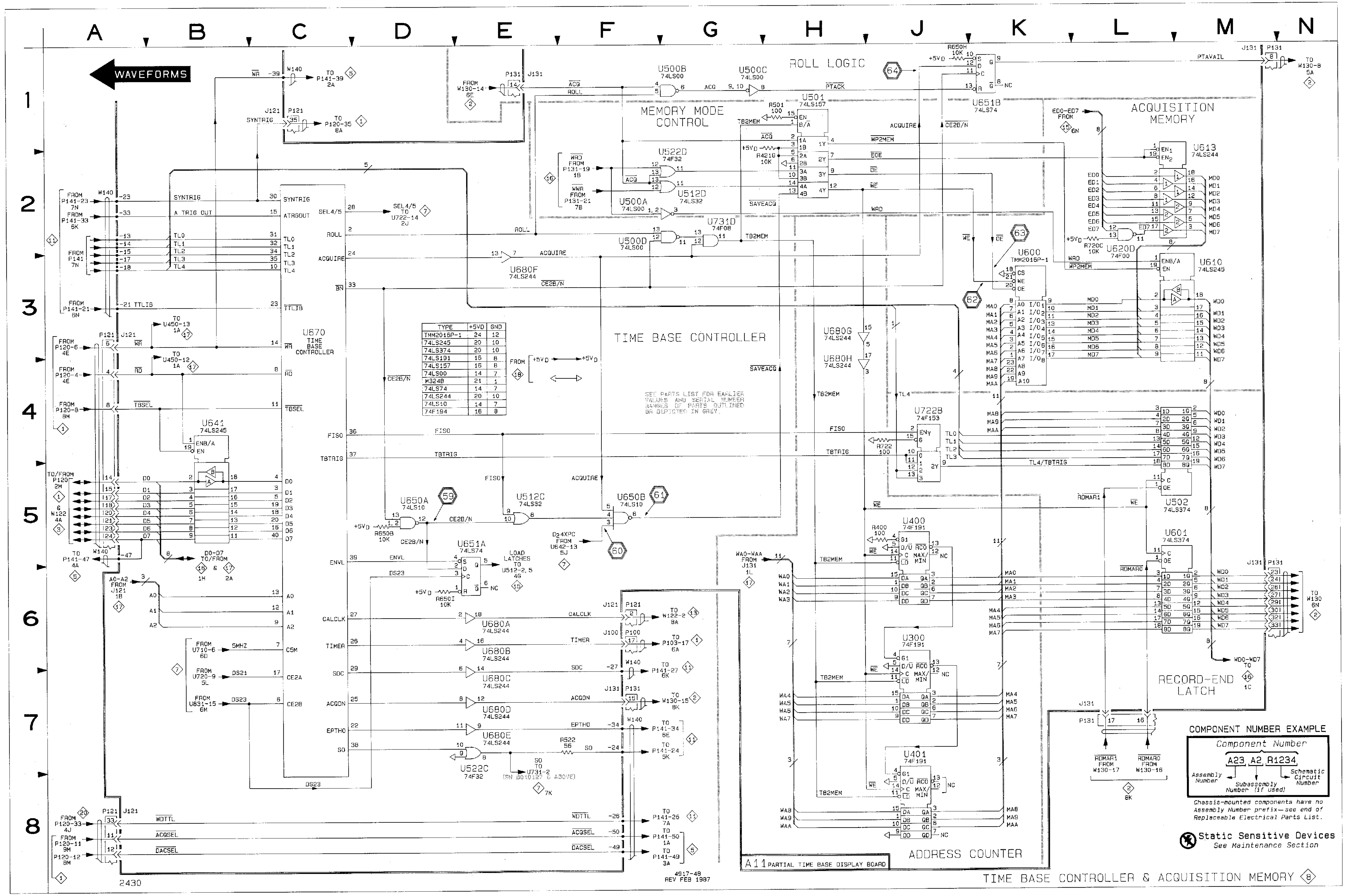
ASSEMBLY A11

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J100	6F	9D	U512D	2G	6D
J121	1C	9L	U522C	7E	6F
J121	3A	9L	U522D	2G	6F
J121	6F	9L	U600	3K	7B
J121	8A	9L	U601	5M	7C
J131	1E	1E	U610	3M	7C
J131	1M	1E	U613	2M	7E
J131	6M	1E	U620D	2L	7E
J131	7F	1E	U641	4B	7J
J131	7L	1E	U650A	5D	7K
			U650B	5F	7K
R400	5J	5B	U651A	5E	7K
R421G	1H	4E	U651B	1K	7K
R501	1H	6B	U670	3C	7L
R522	7F	6F	U680A	6E	8J
R650B	5D	7K	U680B	6E	8J
R650H	1J	7K	U680C	7E	8J
R650I	6D	7K	U680D	7E	8J
R720C	2L	8F	U680E	7E	8J
R722	4J	8G	U680F	3E	8J
			U680G	3H	8J
U300	6J	4C	U680H	4H	8J
U400	5J	5B	U722B	4J	8F
U401	7J	5C	U731D	2G	8H
U500A	2F	6B			
U500B	1G	6B	W140	1C	8K
U500C	1G	6B	W140	2A	8K
U500D	2F	6B	W140	5A	8K
U501	1H	6B	W140	6F	8K
U502	5M	6C	W140	7F	8K
U512C	5E	6D			

Partial A11 also shown on diagrams 7, 15, 16, 17 and 18.

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P100	6F	CHASSIS	P131	1E	CHASSIS
P121	1C	CHASSIS	P131	1M	CHASSIS
P121	3A	CHASSIS	P131	6M	CHASSIS
P121	6F	CHASSIS	P131	7F	CHASSIS
P121	8A	CHASSIS	P131	7L	CHASSIS



TIME BASE CONTROL & ACQ MEMORY

8

ATTENUATORS & PREAMPS DIAGRAM 9

ASSEMBLY A10

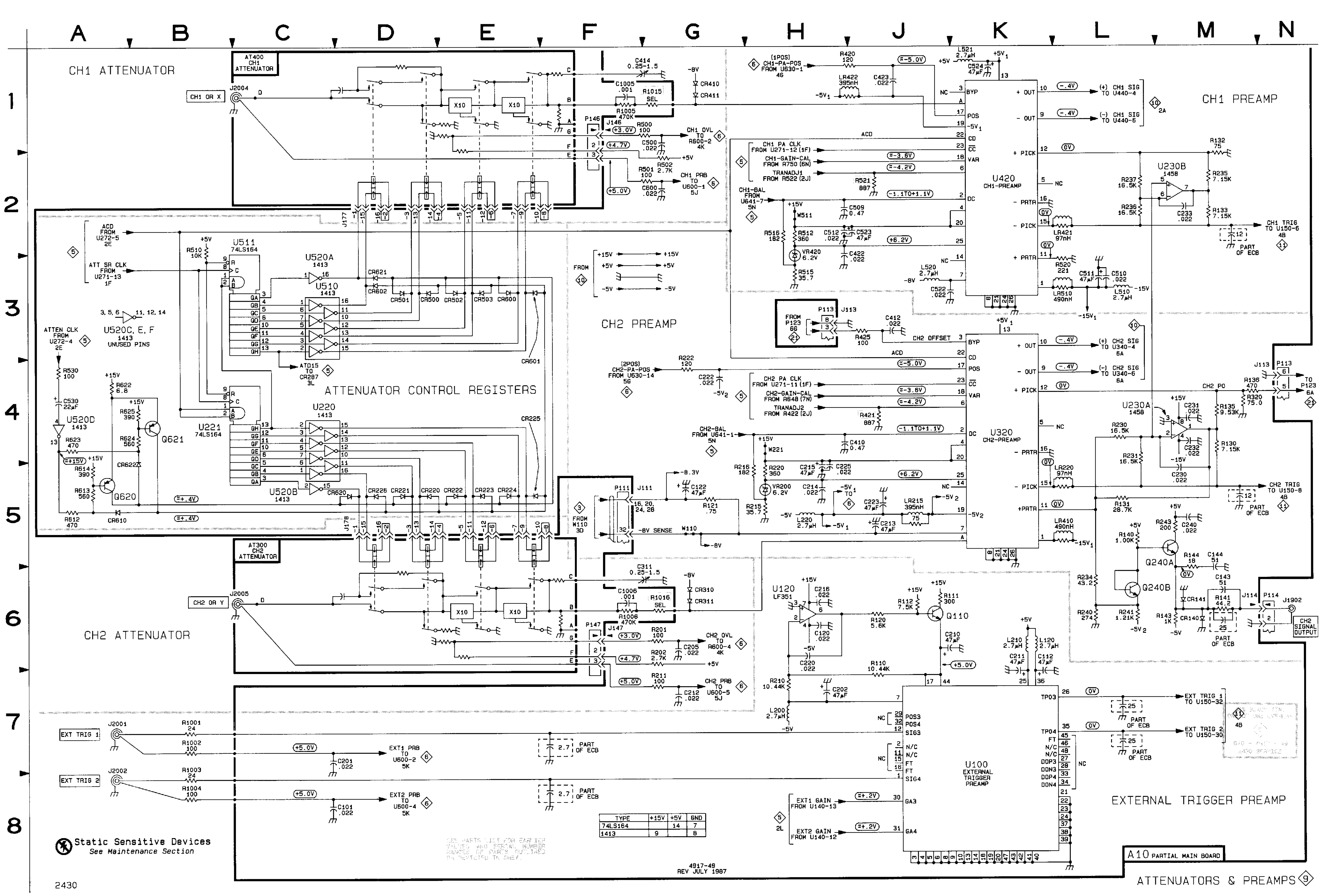
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
AT300	5C	4A	CR140	6M	2F	LR421	2L	5E	R425	3J	5C
AT400	1C	5A	CR141	6M	2G	LR422	1H	5E	R500	1F	7B
			CR220	5D	3D	LR510	3L	6C	R501	2F	7B
C101	8D	1A	CR221	5D	3D				R502	2G	6B
C112	6K	1C	CR222	5E	3D	Q110	6J	1C	R510	2B	7C
C120	6H	2D	CR223	5E	2D	Q240A	5M	2F	R512	2H	7C
C122	5G	2D	CR224	5E	2D	Q240B	6L	2F	R515	3H	7C
C143	6M	2G	CR225	4E	2D	Q620	5A	8D	R516	2H	7C
C144	5M	2F	CR226	5D	3D	Q621	4B	7D	R520	3L	6D
C201	7D	3A	CR310	6G	4C				R521	2J	6D
									R530	4A	7E
C202	7H	3B	CR311	6G	4C	R110	6J	1B	R612	5A	7C
C205	6G	3A	CR410	1G	5C	R111	6J	2C	R613	5A	7C
C210	6J	3B	CR411	1G	5C	R112	6J	2C	R614	5A	7C
C211	6K	3B	CR500	3D	7C	R120	6J	2C	R622	4A	8C
C212	7G	3C	CR501	3D	7C	R121	5G	2D	R623	4A	8D
C213	5J	3C	CR502	3E	8C	R130	4M	2E	R624	4A	8D
C214	5H	3C	CR503	3E	8C	R131	5L	2E	R625	4A	8D
C215	5H	3D	CR600	3E	8C	R132	1M	2F	R1001	7B	3A
C216	6H	3C	CR601	4E	7B	R133	2M	2F	R1002	7B	3A
C220	6H	2D	CR602	3E	7C	R135	4M	3E	R1003	7B	1A
C222	4G	3D	CR610	5A	7C	R136	4M	2E	R1004	8B	1A
C223	5J	3D	CR620	5D	7D	R140	5L	2F			
C225	5H	3D	CR621	3D	7D	R141	6M	2G	U100	7K	2B
C230	5M	2E	CR622	5A	8D	R143	6M	2G	U120	6H	2D
C231	4M	2E				R144	5M	2F	U220	4C	3D
C232	4M	2E	J111	5F	1E	R201	6G	3A	U221	4B	3E
C233	2M	2F	J113	3H	1G	R202	6G	3A	U230A	4L	2E
C240	5M	2G	J113	4N	1G	R210	7H	3B	U230B	2M	2E
C311	6F	4C	J114	6M	2K	R211	7G	3B	U320	4K	4C
C410	4J	4B	J146	1F	6B	R215	5H	3C	U420	2K	5C
C412	3J	4C	J147	6F	3A	R216	5G	3C	U510	3C	7B
C414	1F	5C	J177	2D	6A	R220	5H	3C	U511	2C	7C
C422	2J	7D	J178	5D	4A	R222	4G	3D	U520A	3C	7D
C423	1J	5D				R230	4L	2E	U520B	5C	7D
C500	1G	7B	L120	6K	1C	R231	4L	2E	U520D	4A	7D
C509	2J	6B	L200	7H	3B	R234	6L	3E			
C510	3L	7C	L210	6K	3C	R235	2M	2F	VR200	5H	3C
C511	3L	7C	L220	5H	3D	R236	2L	2F	VR420	2H	7D
C512	2H	6C	L510	3L	7C	R237	2L	2F			
C522	3J	7D	L520	3J	7D	R240	6L	2F			
C523	2J	7D	L521	1K	7D	R241	6L	3F	W110	5G	3C
C524	1K	7D				R243	5M	2G	W221	4H	3D
C530	4A	7E	LR215	5J	3E	R320	4M	3E	W511	2H	6C
C600	2G	7B	LR220	5L	3E	R420	1H	5E			
			LR410	5L	7C	R421	4J	5D			

Partial A10 also shown on diagrams 5, 6, 10, 11, 12, 13, 14 and 19.

CHASSIS MOUNTED PARTS

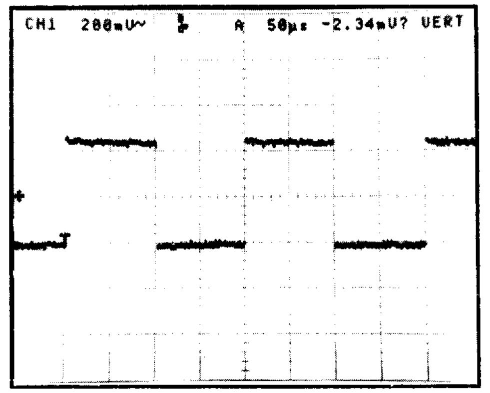
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1005	1F	CHASSIS	J2004	1C	CHASSIS	P114	6N	CHASSIS	R1003	7B	CHASSIS
C1006	6F	CHASSIS	J2005	6C	CHASSIS	P146	1F	CHASSIS	R1004	8B	CHASSIS
						P147	6F	CHASSIS	R1005	1F	CHASSIS
J1902	6N	CHASSIS	P111	5F	CHASSIS				R1006	6F	CHASSIS
J2001	7A	CHASSIS	P113	3H	CHASSIS	R1001	7B	CHASSIS	R1015*	1G	CHASSIS
J2002	7A	CHASSIS	P113	4N	CHASSIS	R1002	7B	CHASSIS	R1016*	6G	CHASSIS

***See Parts List for serial number ranges.**



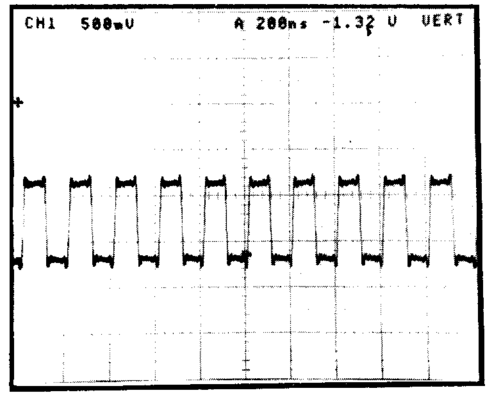
WAVEFORMS FOR DIAGRAM 10

65

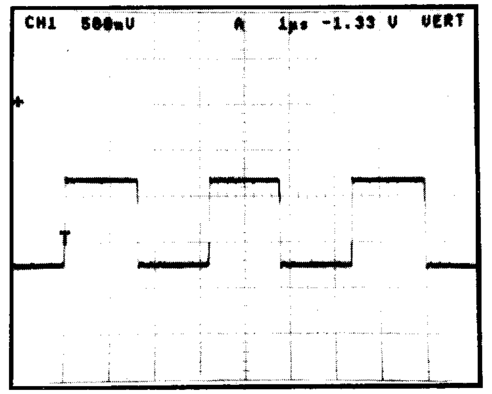


CAL SIGNAL ON CH1 INPUT
NORMAL ACQUISITION

68



71



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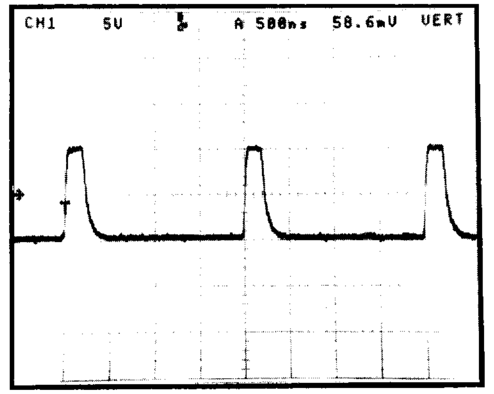

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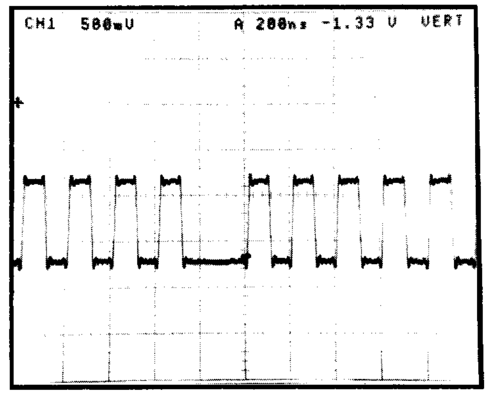
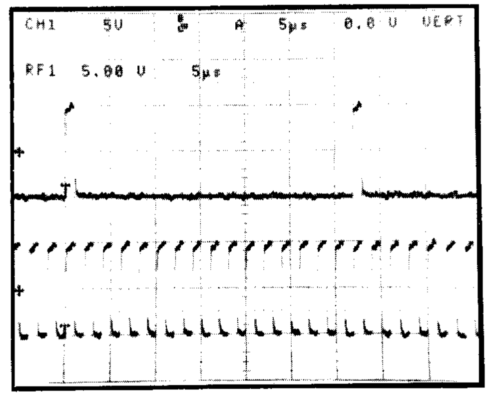


72

TP345
FISO

TP345
SHORTPIPE



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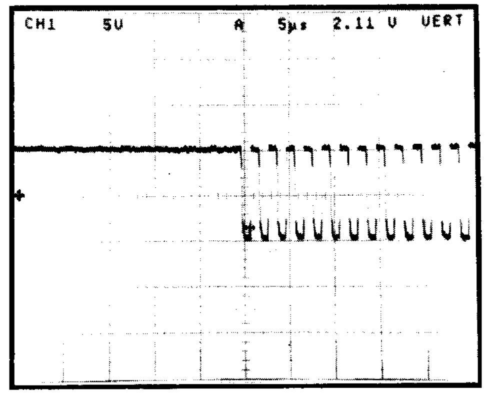

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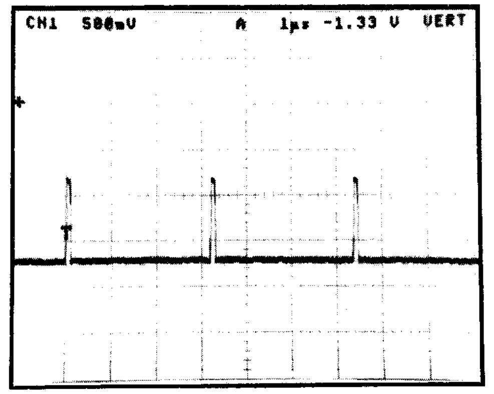


MORE

4917-78A

PEAK DETECTORS & CCD/CLOCK DRIVERS DIAGRAM 10

ASSEMBLY A10

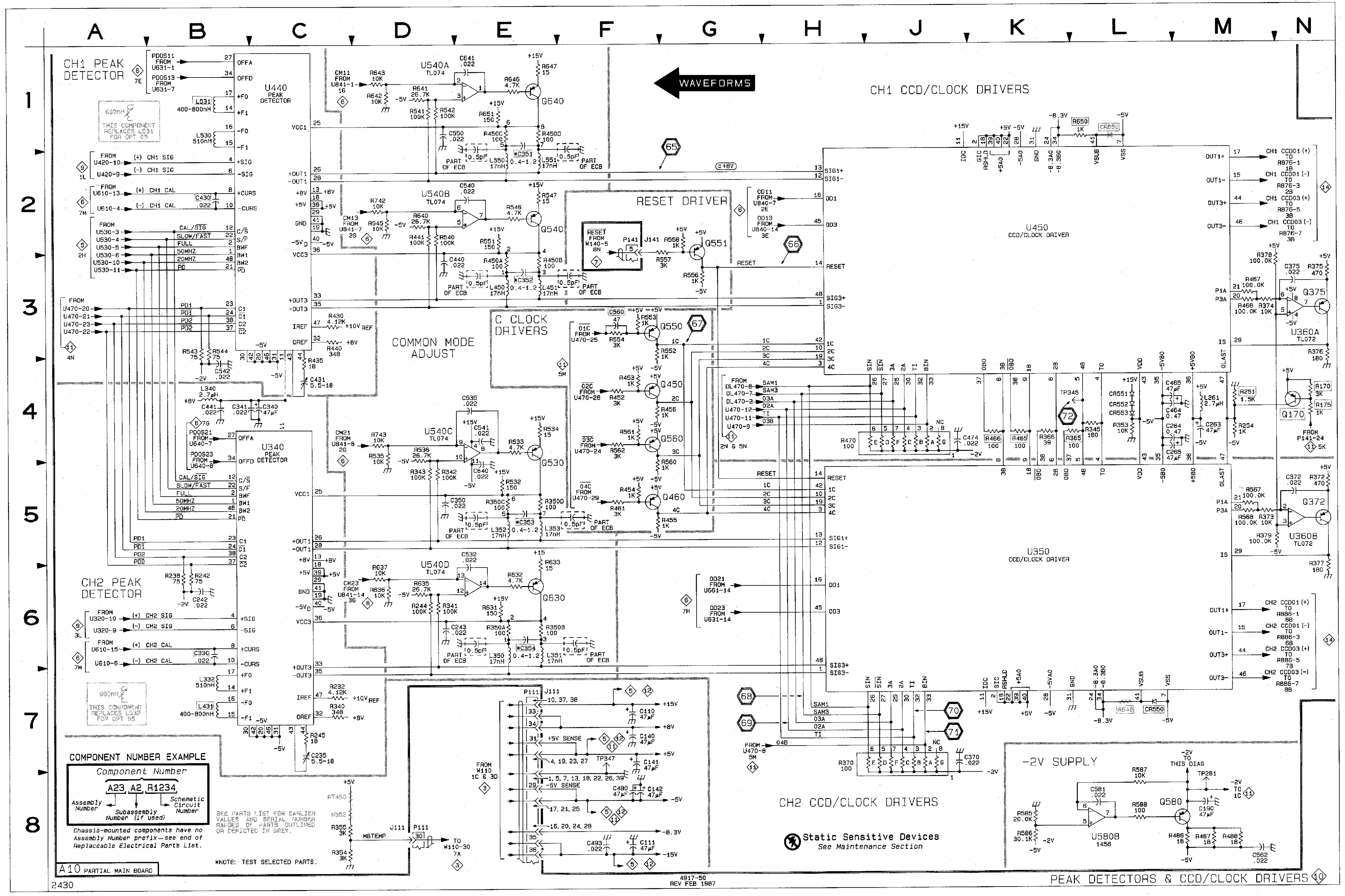
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C110	7F	1C	J111	8D	1E	R353	4L	7J	R552	3G	7J
C111	8F	1C	J141	2F	2L	R354	8C	4K	R553	3F	7J
C140	7F	2D				R355	8C	4K	R554	3F	7J
C141	7F	1F	L261	4M	2K	R365	4L	3J	R556	3G	7K
C142	8F	1F	L332	7B	4E	R366	4K	3J	R557	3G	7K
C190	8M	2N	L340	4B	3E	R370	7H	4K	R558	2G	7K
C235	7C	3G	L350	6E	3H	R372	5N	4K	R560	5G	7J
C242	6B	2F	L351	6E	3H	R373	5M	4K	R561	4F	7K
C243	6E	3G	L352	5E	4H	R374	3M	4L	R562	4F	7K
C263	4M	3K	L353	5E	4H	R375	3N	4L	R567	5M	5J
C264	4M	3K	L431	7B	4E	R376	3N	4K	R568	5M	5J
C265	4M	3K	L450	3E	5H	R377	6N	4K	R585	8K	7L
C330*	6B	4E	L451	3E	5H	R378	3M	4L	R586	8K	7L
C340	4C	3E	L530	1B	6E	R379	5M	4L	R587	8L	7L
C341	4B	3E	L531	1B	6E	R430	3C	5E	R588	8L	6L
C350	5E	4G	L550	2E	6H	R435	4C	5G	R631	6E	8C
C351*	2E	6H	L551	2E	6H	R440	3C	6G	R632	6E	8C
C352*	3E	5H				R441	2D	5G	R633	6E	8C
C353*	5E	4H	Q170*	4N	2K	R450A	3E	6G	R635	6D	7F
C354*	6E	3H	Q372	5N	4K	R450B	3E	6G	R636	6D	7F
C370	7K	4K	Q375	3N	4K	R450C	1E	6G	R637	6D	7F
C372	5N	4L	Q450	4G	6K	R450D	1E	6G	R640	2D	7G
C375	3N	4L	Q460	5G	5K	R452	4F	6K	R641	1D	7G
C430*	2B	6E	Q530	5E	8D	R453	4F	6K	R642	1D	7G
C431	4C	5G	Q540	2E	6G	R454	5F	5K	R643	1D	7G
C440	3D	5H	Q550	3G	7J	R455	5G	5K	R646	1E	7G
C441	4B	5E	Q551	2G	7K	R456	4G	6K	R647	1E	7G
C464	4M	5K	Q560	4G	7K	R461	5F	5K	R650*	1L	5J
C465	4M	5K	Q580	8L	6L	R465	4K	5J	R651	1E	7G
C474	4K	6K	Q630	6E	8C	R466	4K	5J	R742	2D	9G
C480	8F	6L	Q640	1E	7G	R467	3M	7J	R743	4D	9G
C493	8F	5N				R468	3M	7J			
C532	5E	7F	R170*	4N	2K	R470	4H	6K	RT450*	8C	4K
C535	4E	7F	R175*	4N	2L	R486	8M	6L			
C540	2E	6F	R232	7C	3E	R487	8M	6L	TP281	7M	3M
C541	4E	7F	R238	6B	2F	R488	8M	6L	TP345	4L	4H
C542	4B	7G	R242	6B	3F	R532	5E	8D	TP347	7F	4G
C550	1E	6G	R244	6D	3G	R533	4E	8C			
C560*	3F	7J	R245	7C	3G	R534	4E	8D	U340	4C	4F
C562	8M	6K	R251	4M	3H	R535	4D	7F	U350	5K	4J
C581	8L	7L	R254	4M	3G	R536	4D	7F	U360A	3N	4L
C640	5E	7F	R340	7C	4G	R540	2D	6G	U360B	5N	4L
C641	1E	7G	R341	6D	4G	R541	1D	6G	U440	1C	5F
			R342	5D	4G	R542	1D	6G	U450	2K	6J
CR550*	7L	4J	R343	5D	4G	R543	3B	7G	U540A	1D	7F
CR551	4L	7H	R345	4L	4H	R544	3B	7G	U540B	2D	7F
CR552	4L	7H	R350A	6E	4G	R545	2D	7G	U540C	4D	7F
CR553	4L	7H	R350B	6E	4G	R546	2E	7G	U540D	6D	7F
CR650*	1L	5J	R350C	5E	4G	R547	2E	7G	U580B	8L	7L
			R350D	5E	4G	R548*	7L	4J			
J111	7E	1E	R352*	8C	4K	R551	2E	7G			

Partial A10 also shown on diagrams 5, 6, 9, 11, 12, 13, 14 and 19.

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P111	7E	CHASSIS	P111	8D	CHASSIS	P141	2F	CHASSIS			

***See Parts List for serial number ranges.**

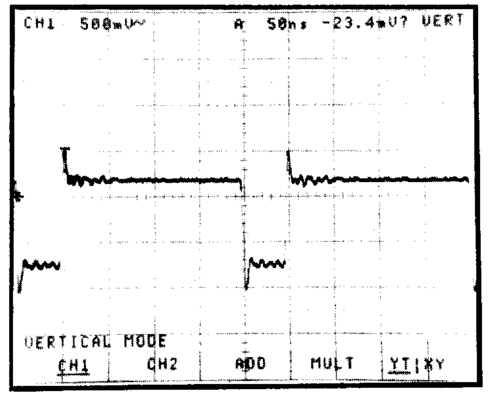


PEAK DETECTORS & CCD/CLOCK DRIVERS

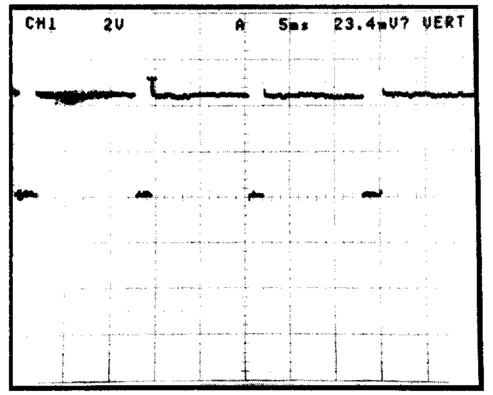
10

WAVEFORMS FOR DIAGRAM 11

73

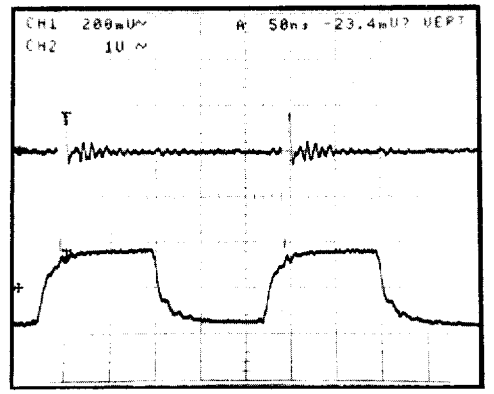


78



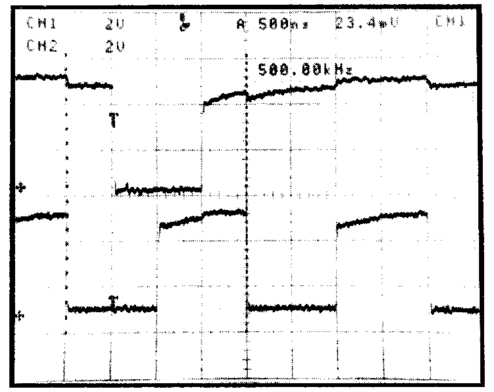
74

75



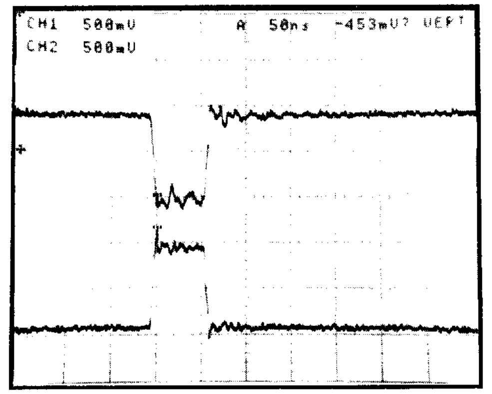
79

80



76

77



4917-79

TRIGGERS & PHASE CLOCKS DIAGRAM 11

ASSEMBLY A10

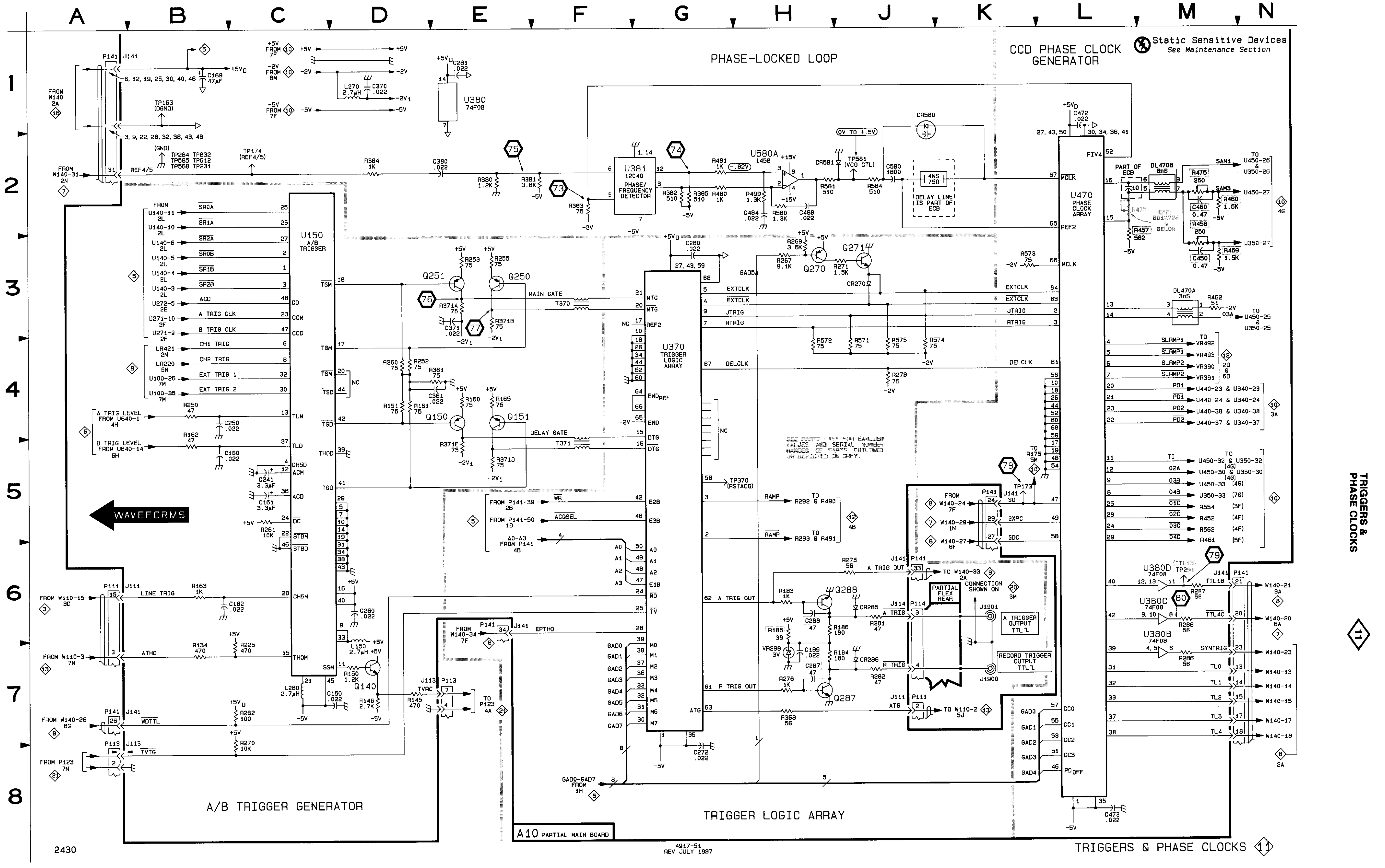
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C150	7D	1G	J114	6J	2K	R252	4D	4K	R571	4J	6L
C160	5C	1K	J141	1B	2L	R253	3E	3K	R572	4H	6L
C161	5C	1K	J141	5K	2L	R255	3E	4K	R573	3K	6L
C162	6C	2K	J141	6E	2L	R260	4D	3K	R574	4J	6M
C169	1B	2N	J141	6J	2L	R261	5C	2K	R575	4J	6M
C189	7H	3N	J141	6M	2L	R262	7C	2L	R580	2H	7L
C241	5C	2G	J141	7B	2L	R267	3H	4M	R581	2H	7L
C250	4B	2G				R268	3H	4M	R584	2J	6L
C260	6D	3K	L150	7D	2G	R270	7C	3K			
C272	8G	3L	L260	7C	3H	R271	3J	4M	T370	3F	3K
C280	3G	3M	L270	1D	3K	R275	6J	3M	T371	5F	4K
C281	1E	3M				R276	7H	3M			
C287	7H	2N	Q140	7D	1G	R278	4J	4L	TP163	1B	2M
C288	6H	2N	Q150	4E	1K	R281	6J	2K	TP173	5K	2L
C361	4E	2K	Q151	4E	1K	R282	7J	2K	TP174	2C	2L
C370	1D	4K	Q250	3E	3K	R286	7M	2N	TP231	2B	3E
C371	3E	3K	Q251	3E	3K	R287	6M	2N	TP284	2B	3M
C380	2E	4M	Q270	3H	3N	R288	6M	2N	TP291*	6M	2N
C450*	3M	5L	Q271	3J	4M	R361	4E	4K	TP370	5H	3M
C460*	2M	6L	Q287	7J	2N	R368	7H	3M	TP568	2B	6L
C472	1L	5L	Q288	6J	2N	R371A	3E	3K	TP581	2J	7L
C473	8L	5L				R371B	3E	3K	TP585	2B	7M
C484	2H	7L	R134	7B	1F	R371D	5E	3K	TP612	2B	9B
C488	2H	7L	R145	7D	1G	R371E	5E	3K	TP832	2B	10F
C580	2J	6L	R146	7D	1G	R380	2E	4M			
			R150	7D	1G	R381	2E	4M	U150	3C	2H
CR270	3J	4L	R151	4D	1K	R382	2G	4M	U370	4G	3L
CR285	6J	3N	R160	4E	1K	R383	2F	4M	U380B	6M	3M
CR286	7J	3N	R161	4D	1K	R384	2D	4M	U380C	6M	3M
CR580	1J	6L	R162	4B	1K	R385	2G	4M	U380D	6M	3M
CR581	2H	7L	R162	4B	1K	R457*	2M	6L	U380	1E	3M
			R163	6B	2K	R458*	2M	5K	U381	2G	4M
DL470A	3M	5L	R165	4E	1K	R459*	3M	5L	U470	2L	5M
DL470B	2M	5L	R183	6H	3M	R460*	2M	5K	U580A	2H	7L
			R184	7J	3N	R462	3M	6K			
J111	6B	1E	R185	6H	3N	R475	2M	6L	VR298	7H	2N
J111	7J	1E	R186	6J	3N	R480	2G	6L			
J113	7B	1G	R225	7C	1G	R481	2G	6L			
J113	7D	1G	R250	4B	3H	R499	2H	7L			

Partial A10 also shown on diagrams 5, 6, 9, 10, 12, 13, 14 and 19.

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J1900	7K	CHASSIS	P111	7J	CHASSIS	P141	1A	CHASSIS	P141	6N	CHASSIS
J1901	6K	CHASSIS	P113	7A	CHASSIS	P141	5K	CHASSIS	P141	7A	CHASSIS
			P113	7E	CHASSIS	P141	6E	CHASSIS			
P111	6A	CHASSIS	P114	6J	CHASSIS	P141	6J	CHASSIS			

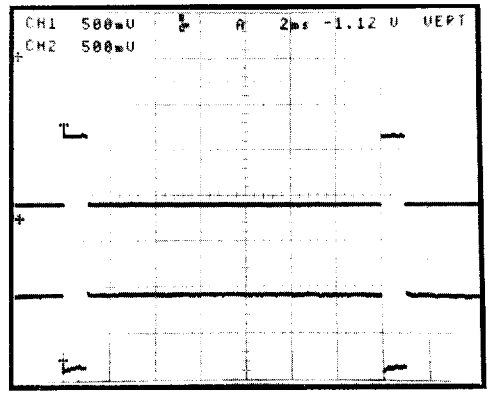
***See Parts List for serial number ranges.**



WAVEFORMS FOR DIAGRAM 12

81

82

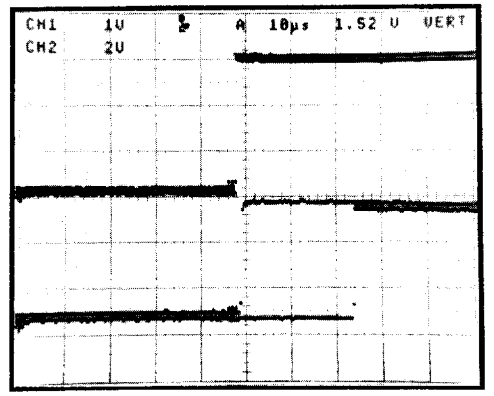


CAL SIGNAL INPUT
TRIGGERED-ACQUIRING
SEC/DIV at 100 ms

TEST SCOPE TRIGGERED ON START

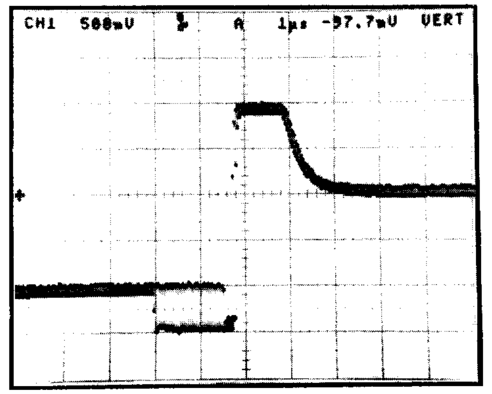
86

87



+SLOPE ENVELOPE AQUISITION MODE

83

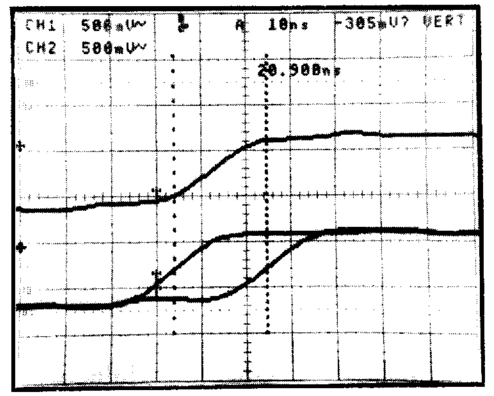


2430 SEC/DIV at 5nS

TEST SCOPE TRIGGERED
ON SLRMP1 +SLOPE

88

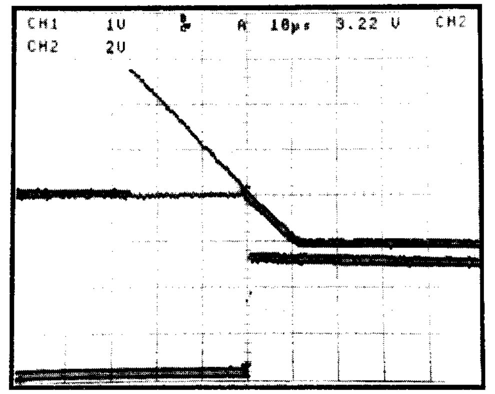
89



TEST SCOPE TIGGERED ON STOP
ENVELOPE ACQUISITION MODE

84

85



4917-80

JITTER CORRECTION RAMPS DIAGRAM 12

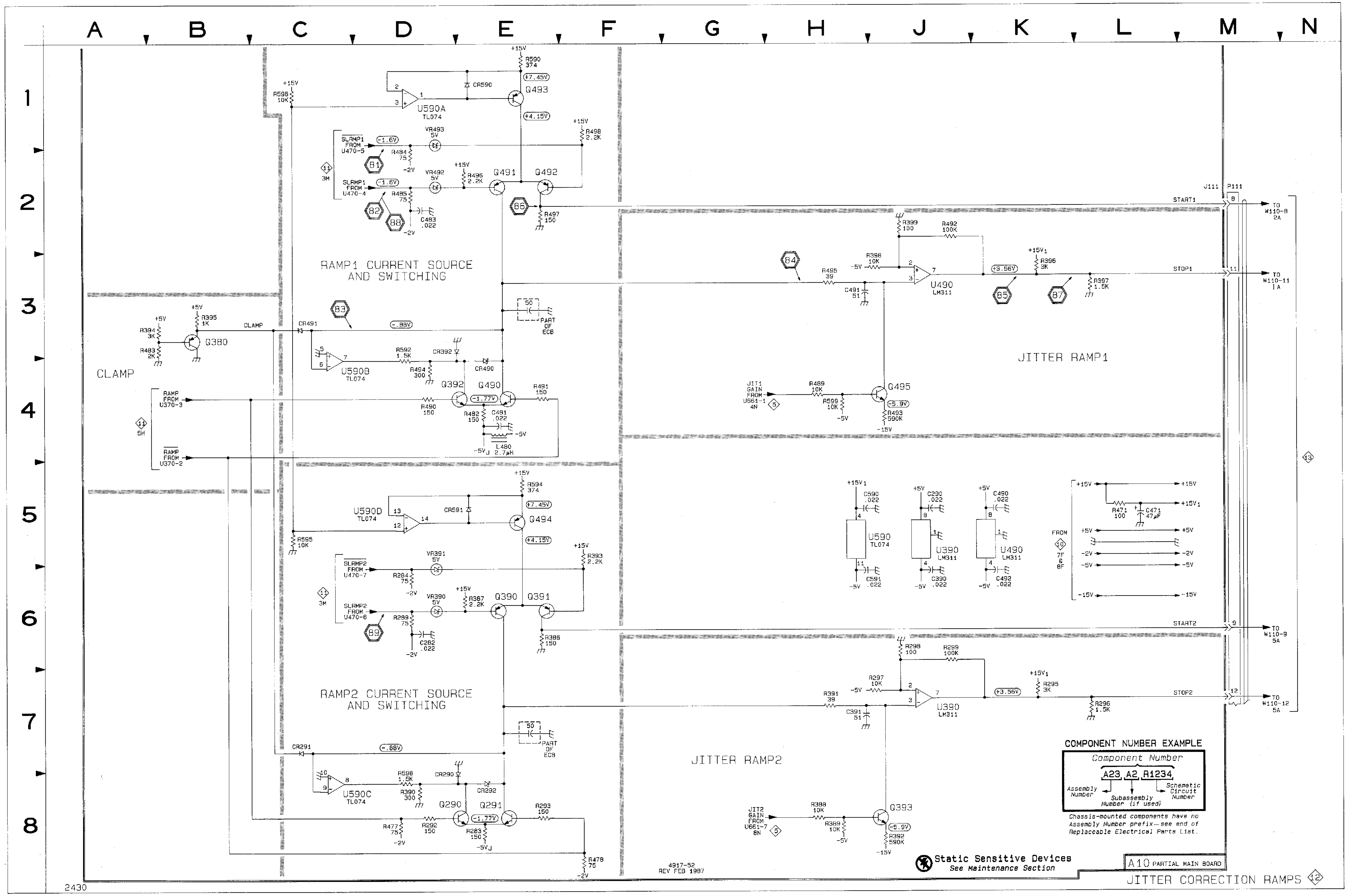
ASSEMBLY A10

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C282	6D	3N	Q491	2E	6N	R483	3B	5M
C290	5J	3N	Q492	2E	6N	R484	2D	6M
C390	6J	4N	Q493	1E	4N	R485	2D	6M
C391	7H	4N	Q494	5E	4N	R489	4H	6M
C471	5L	4N	Q495	4J	6N	R490	3D	5N
C481	4E	5M				R491	4E	6N
C483	2D	6M	R283	8E	3M	R492	2J	5N
C490	5K	5N	R284	6D	4N	R493	4J	6N
C491	3H	6N	R289	6D	3M	R494	3D	5N
C492	6K	6N	R292	8C	3N	R495	3H	6N
C590	5J	4N	R293	8E	3N	R496	2E	6N
C591	6J	5N	R295	7K	3N	R497	2E	6N
			R296	7L	3N	R498	1F	6M
CR290	8D	3N	R297	7J	3N	R590	1E	4N
CR291	7C	3N	R298	6J	3N	R592	3D	5N
CR292	8D	3N	R299	6J	3N	R594	5E	4N
CR392	3D	5N	R386	6E	3N	R595	5C	4N
CR490	4E	5N	R387	6E	4N	R596	1C	4N
CR491	3C	5N	R388	8H	4N	R598	8C	5N
CR590	1E	5M	R389	8H	5N	R599	4H	6M
CR591	5D	4N	R390	8C	3N			
			R391	7H	3N	U390	7J	3N
J111	2M	1E	R392	8J	3N	U490	3J	6N
			R393	5F	4N	U590A	1D	5N
L480	4E	6M	R394	3B	5M	U590B	4C	5N
			R395	3B	5M	U590C	8C	5N
Q290	8D	3N	R396	3K	5N	U590D	5D	5N
Q291	8E	3N	R397	3L	5N	U590	5J	5N
Q380	3B	4M	R398	3J	5N			
Q390	6E	4N	R399	2J	5N	VR390	6D	4N
Q391	6E	4N	R471	5L	4N	VR391	5D	4N
Q392	4D	5N	R477	8C	6M	VR492	2D	6N
Q393	8J	4N	R478	8F	6M	VR493	1D	6N
Q490	4E	5N	R482	4E	6M			

Partial A10 also shown on diagrams 5, 6, 9, 10, 11, 13, 14 and 19.

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P111	2M	CHASSIS						

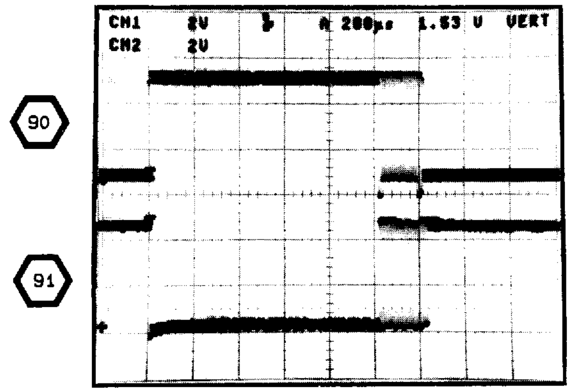


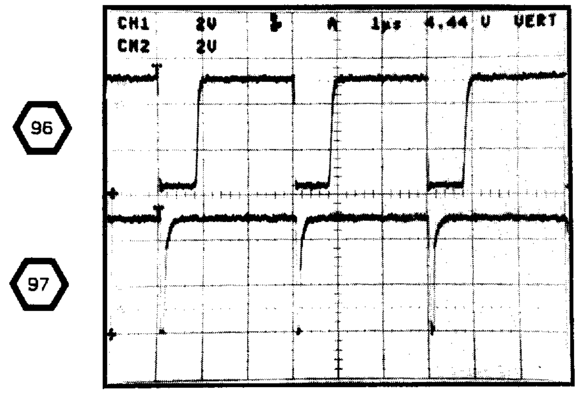
JITTER CORRECTION RAMPS

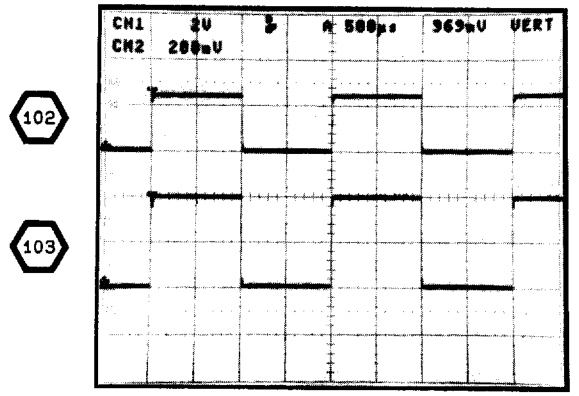
12

WAVEFORMS FOR DIAGRAM 13

TEST SCOPE IN ENVELOPE

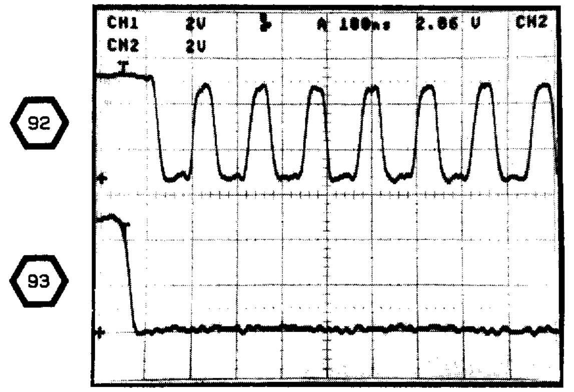


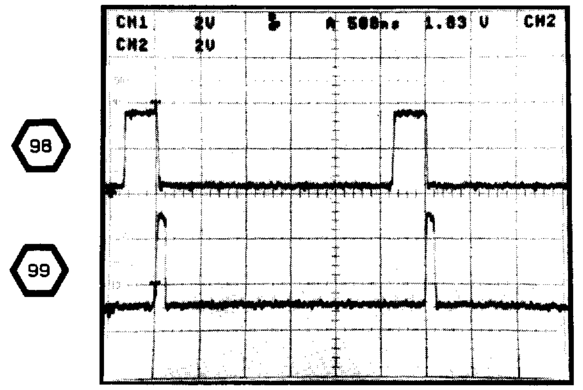


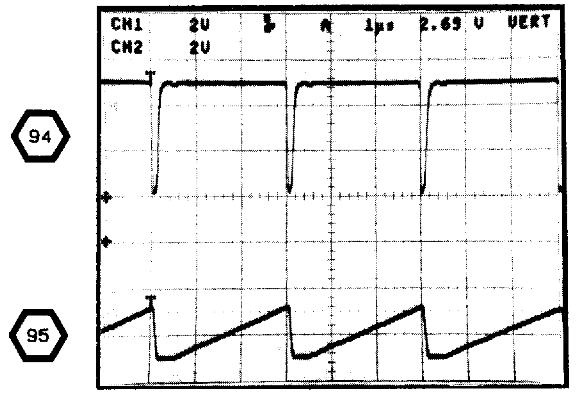


2430 INIT FRONT PANEL

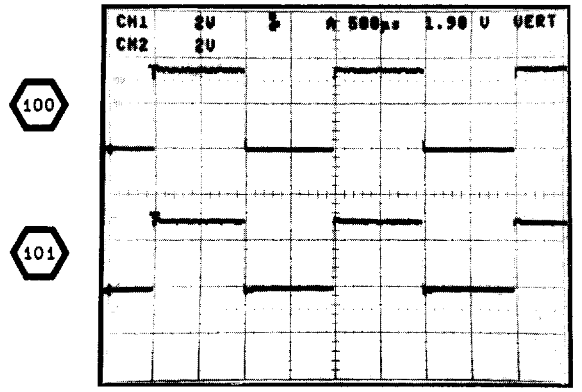
TRIG ON -SLOPE







2430 AT 5 NS/DIV-NO HOLDOFF



2430 INIT FRONT PANEL

MORE

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TRIGGER HOLDOFF, JITTER COUNTERS & CALIBRATOR DIAGRAM 13

ASSEMBLY A10

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C102	7E	2A	J111	7E	1E	J2006	7F	2A			

Partial A10 also shown on diagrams 5, 6, 9, 10, 11, 12, 14 and 19.

ASSEMBLY A13

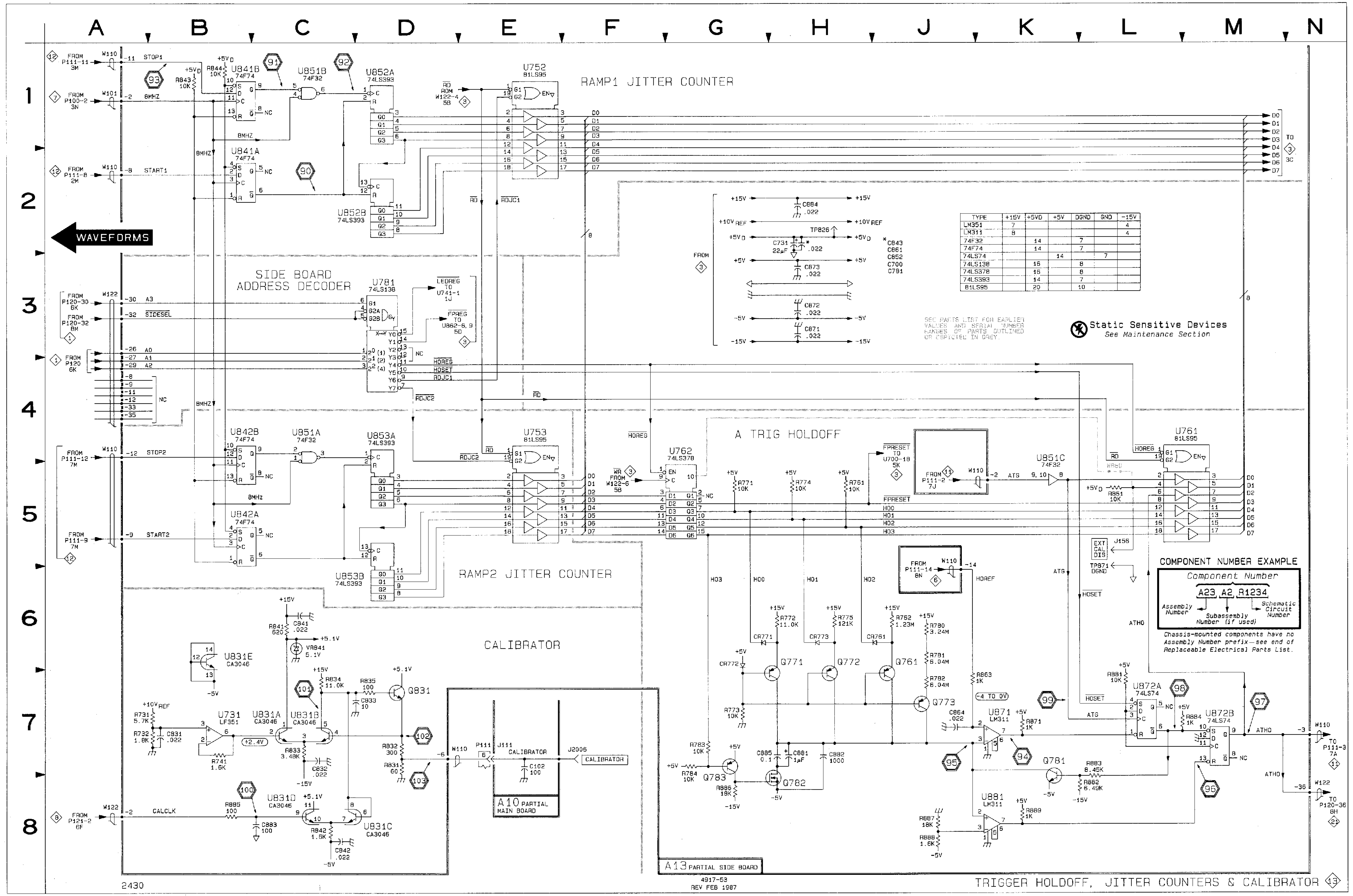
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C700	3J	1A	Q772	6H	2L	R844	1B	3G	U842A	5B	3G
C731	2H	1F	Q773	7J	2L	R861	5L	2J	U842B	4B	3G
C781	3J	1M	Q781	7K	2M	R863	7K	2K	U851A	4C	3H
C831	7B	2E	Q782	7H	2M	R871	7K	2L	U851B	1C	3H
C832	7C	2F	Q783	7G	2M	R881	7L	2M	U851C	4K	3H
C833	7D	2F	Q831	7D	3E	R882	8L	3M	U852A	1D	3H
C841	6C	3F				R883	7L	3M	U852B	2D	3H
C842	3C	3F	R731	7A	2E	R884	7M	3M	U853A	4D	3H
C843	2J	2G	R732	7A	2E	R885	8B	3M	U853B	6C	3H
C852	3J	2H	R741	7B	2F	R886	8G	2M	U871	7K	2K
C861	2J	2J	R761	5H	1K	R887	8J	2M	U872A	7L	3L
C864	7J	2K	R762	6J	2K	R888	8J	2M	U872B	7M	3L
C871	3H	3K	R771	5G	1L	R889	8K	2M	U881	8K	3M
C872	3H	2L	R772	6H	2K						
C873	3H	3L	R773	7G	2K	TP826	2H	2E	VR841	6C	3F
C881	7H	2M	R774	5H	1L	TP871	5L	2J			
C882	7H	2M	R775	6H	2L				W101	1A	2E
C883	8C	3M	R780	6J	2M	U731	7B	2F	W110	1A	3E
C884	2H	3M	R781	6J	2M	U752	1E	2H	W110	2A	3E
C885	7G	3M	R782	7J	2M	U753	4E	2H	W110	4A	3E
			R783	7G	1M	U761	4M	2J	W110	5J	3E
CR761	6J	2K	R784	7G	1M	U762	4G	1J	W110	5K	3E
CR771	6G	2L	R831	7D	2E	U781	3D	1M	W110	7N	3E
CR772	6G	2L	R832	7D	2E	U831A	7C	3F	W122	3A	1L
CR773	6H	2L	R833	7C	3E	U831B	7C	3F	W122	8A	1L
			R834	7C	3E	U831C	8D	3F	W122	8N	1L
J156*	5L	2J	R835	7D	3E	U831D	8C	3F	W860*	5L	2J
			R841	6C	3F	U831E	6B	3F			
Q761	6J	2K	R842	8C	3F	U841A	2B	3G			
Q771	6H	2K	R843	1B	2G	U841B	1B	3G			

Partial A13 also shown on diagram 3.

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P111	7E	CHASSIS									

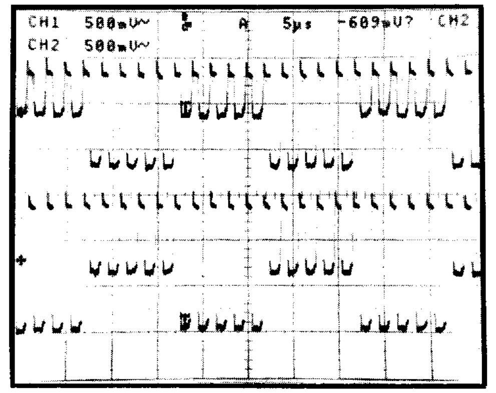
***See Parts List for serial number ranges.**



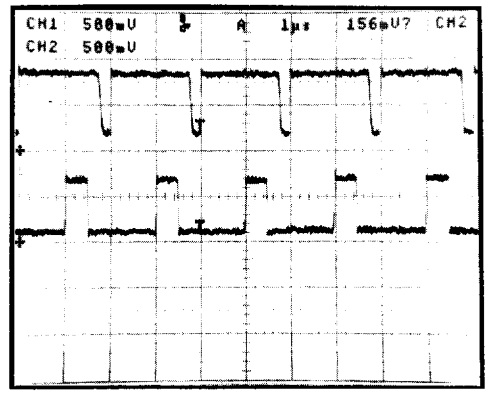
WAVEFORMS FOR DIAGRAM 14

TEST SCOPE LF REJ COUPLING
TRIGGERED ON 2430 CALIBRATOR SIGNAL

104
105

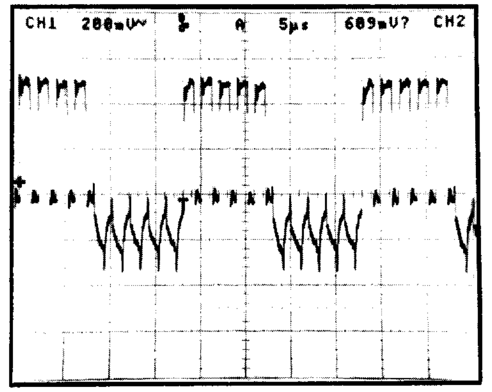


108
109

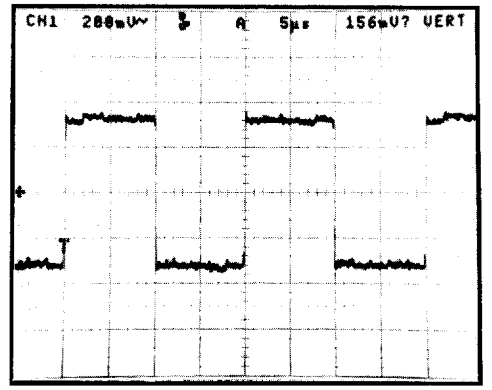


2430 VOLTS/DIV AT 100mV
SEC/DIV AT 5µs;
CALIBRATOR SIGNAL APPLIED
TO CH 1 INPUT; AC COUPLED.
VERT MODE CH 1 (CH 2 FOR
CHANNEL 2 TROUBLESHOOTING)

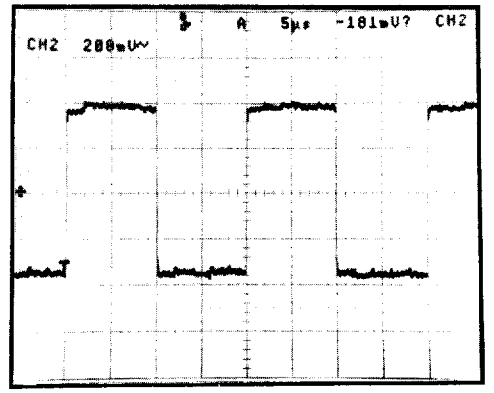
106



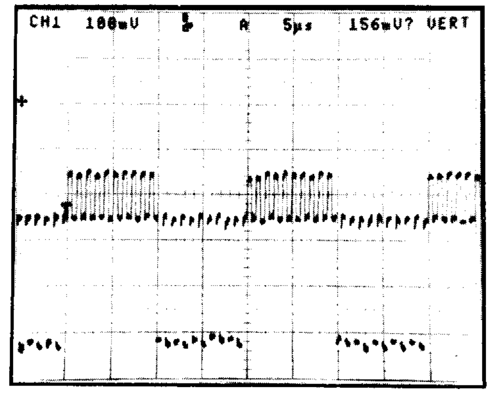
110



107



111



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CCD OUTPUT DIAGRAM 14

ASSEMBLY A10

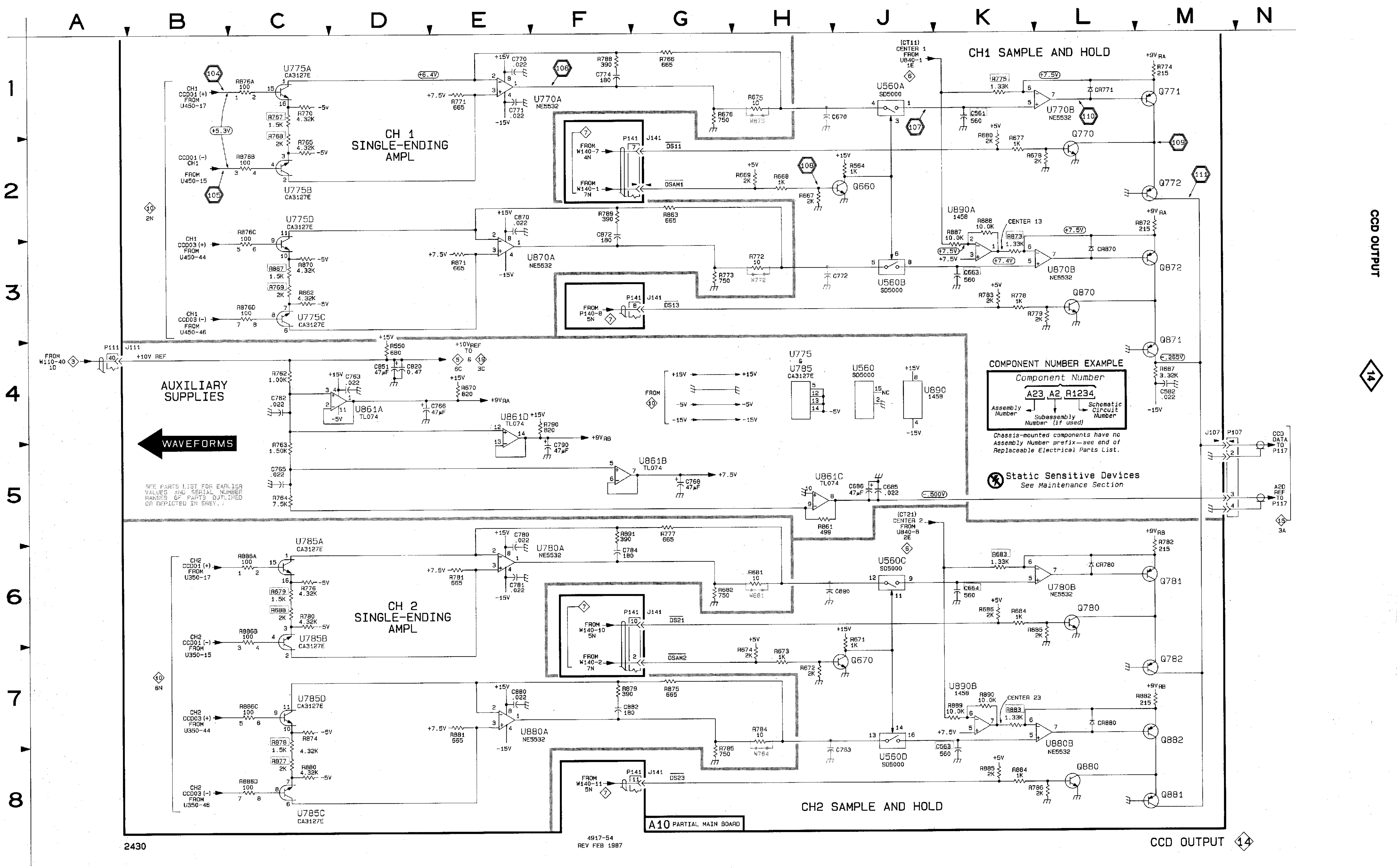
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C561	1K	7K	Q770	2L	8L	R769*	3C	8L	R886A	6C	9M
C563	8K	7K	Q771	1M	8L	R770	1C	8K	R886B	6C	9M
C582	4M	7M	Q772	2M	8L	R771	1E	8K	R886C	7C	9M
C663	3K	7K	Q780	6L	7N	R772*	3H	9L	R886D	8C	9M
C664	6K	7K	Q781	6M	8N	R773	3G	9L	R887	2K	9N
C670*	1H	7K	Q782	7M	7N	R774	1M	8L	R888	2K	9N
C680*	6H	8M	Q870	3L	8M	R775	1K	8M	R889	7K	8N
C685	5J	7M	Q871	4M	9M	R776	6C	8M	R890	7K	8N
C686	5J	7N	Q872	3M	8L	R777	5G	8M	R891*	5F	9N
C762	4C	8J	Q880	8L	8N	R778	3K	8L			
C763	4D	9J	Q881	8M	8N	R779	3L	8M	U560A	1J	7K
C765	5C	8K	Q882	7M	9N	R780	6C	8M	U560B	3J	7K
C766	4E	9K				R781	6E	8M	U560C	6J	7K
C768	5G	9K	R550	4D	7G	R782	6M	8N	U560D	8J	7K
C770	1E	8L	R564	2J	7K	R783	3K	8M	U770A	1F	8L
C771	1E	8L	R667	2H	8K	R784*	7H	9N	U770B	1L	8L
C772*	3H	8L	R668	2H	8K	R785	8G	9N	U775A	1C	9L
C774	1F	8L	R669	2H	8K	R786	8L	8N	U775B	2C	9L
C780	5E	8N	R670	4E	7L	R788	1F	8L	U775C	3C	9L
C781	6E	8N	R671	6J	7L	R789	2F	8M	U775D	2C	9L
C783*	8H	9M	R672	7H	8K	R790	4F	9N	U780A	6F	8N
C784	6F	8N	R673	7H	8K	R861	5H	9K	U780B	6L	8N
C790	5F	9K	R674	7H	8K	R862	3C	9K	U785A	5C	9M
C820	4D	10F	R675*	1H	8K	R863	2G	9K	U785B	7C	9M
C851	4D	10H	R676	1G	8L	R867	3C	8K	U785C	6C	9M
C870	2E	9L	R677	2K	8M	R870	3C	9K	U785D	7C	9M
C872	2F	9L	R678	2L	8M	R871	3E	9K	U861A	4D	9J
C880	7E	9N	R679	6C	8M	R872	2M	9L	U861B	5G	9J
C882	7F	9N	R680	2K	8M	R873	3K	9L	U861C	5H	9J
			R681*	6H	8M	R874	7C	9M	U861D	4E	9J
CR771	1L	8L	R682	6G	8M	R875	7G	9M	U870A	3F	9L
CR780	6L	8N	R683	6K	7N	R876A	1C	9K	U870B	3L	9L
CR870	3L	9L	R684	6K	8N	R876B	2C	9K	U880A	7F	9N
CR880	7L	9N	R685	6L	8N	R876C	2C	9K	U880B	7L	9N
			R686	6K	8N	R876D	2C	9K	U890A	2K	8N
J107	4M	7M	R687	4M	7L	R877	8C	8L	U890B	7K	8N
J111	4B	1E	R688*	6C	8L	R878	7C	9L			
J141	2G	2L	R762	4C	8J	R879	7F	9L	W675*	1H	8K
J141	3G	2L	R763	5C	8J	R880	8C	9M	W681*	6H	8M
J141	6G	2L	R764	5C	8K	R881	7E	9M	W772*	3H	9L
J141	8G	2L	R765	2C	8K	R882	7M	9N	W784*	8H	9N
			R766	1G	8K	R883	7K	8N			
Q660	2J	7K	R767	1C	8K	R884	8K	8N			
Q670	7J	7K	R768*	1C	7K	R885	8K	8N			

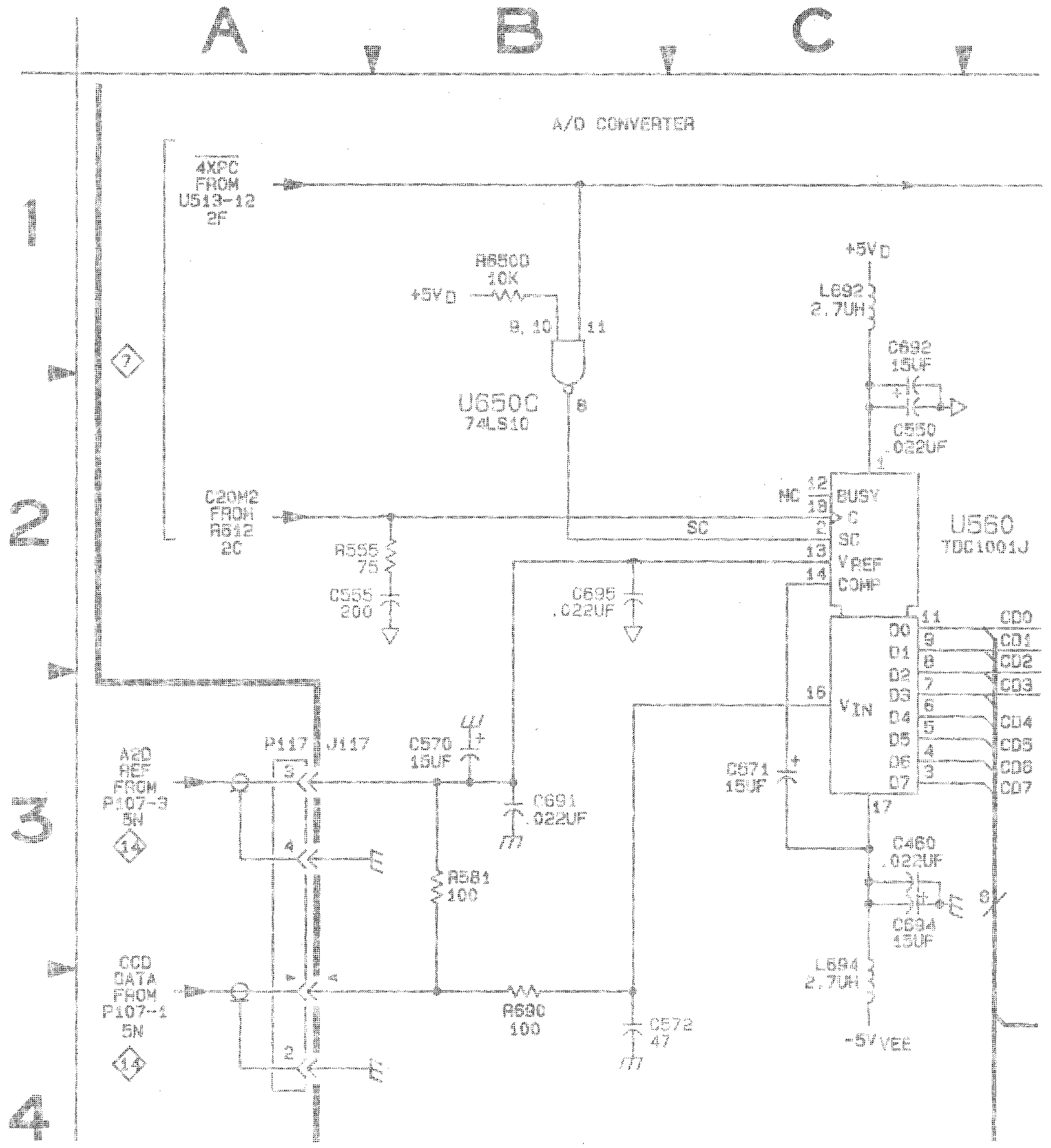
Partial A10 also shown on diagrams 5, 6, 9, 10, 11, 12, 13 and 19.

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P107	4M	CHASSIS	P141	2G	CHASSIS	P141	6F	CHASSIS			
P111	4A	CHASSIS	P141	3G	CHASSIS	P141	8G	CHASSIS			

***See Parts List for serial number ranges.**





4917-69A

A/D CONVERTER

In instruments with serial numbers below B011146, A/D Converter U560 is an 8-bit, successive-approximation device that digitizes the analog samples from the CCD arrays at an overall conversion rate of 2 MHz (shown in the partial diagram 15).

The A2D REF voltage (−0.5 V) is high- and low-pass filtered by C691 and C570 respectively. A reference level of −0.5 V allows conversion of input levels from −0.5 V down to 0 V. The time-multiplexed CCD Data signal current develops a voltage across R581 corresponding to the selected CCD output voltage. This signal is applied to the analog input of U560 (V_{IN}, pin 16) via a low-pass filter (R690-C572).

Sample conversion is initiated by the 2 MHz $\overline{4XPC}$ clock from NAND-gate U650C (acting as an inverter), setting up U560 to start the conversion. The first rising edge of the C20M2 (20 MHz) clock applied to pin 18 gets the A/D Converter ready, and the next eight rising edges clock the data conversion process of the A/D Converter. A valid output data byte, present on the ninth clock, is applied to the 8-bit Magnitude Comparator formed by U740 and U732, with the four LSB going to U740 and the four MSB of the byte going to U732. The 10th clock allows time for the next input data to the A/D Converter to settle before conversion starts.

A/D CONVERTER & ACQUISITION LATCHES DIAGRAM 15

ASSEMBLY A11

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C213	6C	3D	C520	6C	5E	C703	6C	8C	R780*	3B	8M
C223	6C	2F	C521	6C	5F	C711	6C	7D	R781*	2B	7M
C231	6C	2H	C522	6C	5F	C712	6C	7D	R880*	4B	8M
C240	6C	2J	C523	6C	5F	C720	6C	8E	R881*	3B	8M
C243	6C	2K	C531	6C	5H	C730	6C	7G	R884*	3B	7M
C261	5C	1G	C532	6C	5H	C731	6C	7H	R890*	4A	8M
C270	5C	2L	C540	6C	5J	C732	6C	7H	R891*	4B	8M
C290	5B	2M	C541	6C	5J	C740	6C	7J			
C291	7B	4M	C550	5C	6M	C770	4C	7M	TP400	7B	5B
C292	7B	3M	C551	6C	5K	C772*	4C	7M	TP530	7C	5G
C312	6C	4D	C555	1C	7M	C774*	3C	7M	TP601	7C	7A
C313	6C	4D	C560	6C	6L	C776*	2C	7M			
C323	6C	3F	C570	2C	7M	C820	6C	9G	U510A	4J	6C
C324	6C	4F	C571*	3C	7M	C832	6C	9H	U510B	3J	6C
C331	6C	3H	C572*	3C	7M	C890*	3B	8M	U511A	7J	6D
C340	6C	3J	C601	6C	6C	C891	4A	8M	U511B	5J	6D
C341	6C	3J	C610	6C	6C	C892	4B	8M	U512A	3G	6D
C342	6C	3K	C611	6C	6D				U512B	4G	6D
C350	6C	3K	C612	6C	6D	J117	3A	8M	U520A	4K	6E
C392	8B	4M	C613	6C	6E				U520B	3K	6E
C400	6C	4B	C620	6C	6E	L692	5B	6M	U521A	7K	6F
C401	6C	4C	C621	6C	6F	L694	8B	6M	U521B	6K	6F
C402	6C	5C	C622	6C	6F	L770*	2B	7M	U560	2D	7L
C414	6C	4D	C623	6C	6F	L780*	3B	7M	U630	7M	7G
C415	6C	4D	C630	6C	6G				U631	5M	7H
C416	6C	4E	C631	6C	6H	R421H	3H	4E	U632	4M	7H
C420	6C	4F	C632	6C	6H	R421I	3K	4E	U640	3M	7J
C422	6C	5F	C640	6C	6J	R421	1J	4E	U650C	2H	7K
C450	6C	4K	C642	6C	6J	R555	2C	6L	U732	2F	8H
C460	3B	4B	C643	6C	7J	R581	3B	8M	U740	2D	8J
C490	5C	5M	C680	6C	7J	R650D	2H	7K	U780*	3B	8M
C500	6C	5B	C691	7C	6M	R650G	2D	7K	U880*	2B	7M
C510	6C	5C	C692	5B	6M	R650	1J	7K			
C511	6C	5D	C694	7B	6M	R690	3B	8M			
C513	6C	5E	C695*	2B	7M	R720	1J	8F			

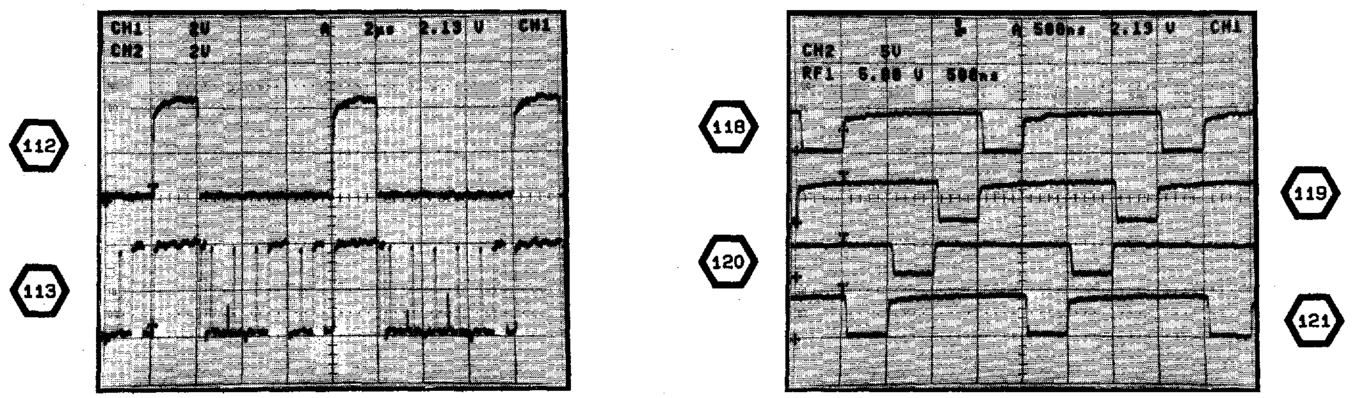
Partial A11 also shown on diagrams 7, 8, 16, 17 and 18.

***See Parts List for serial number ranges.**

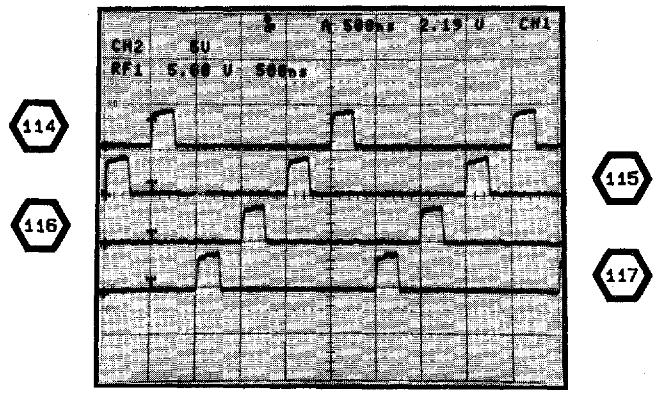
CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P117	3A	CHASSIS									

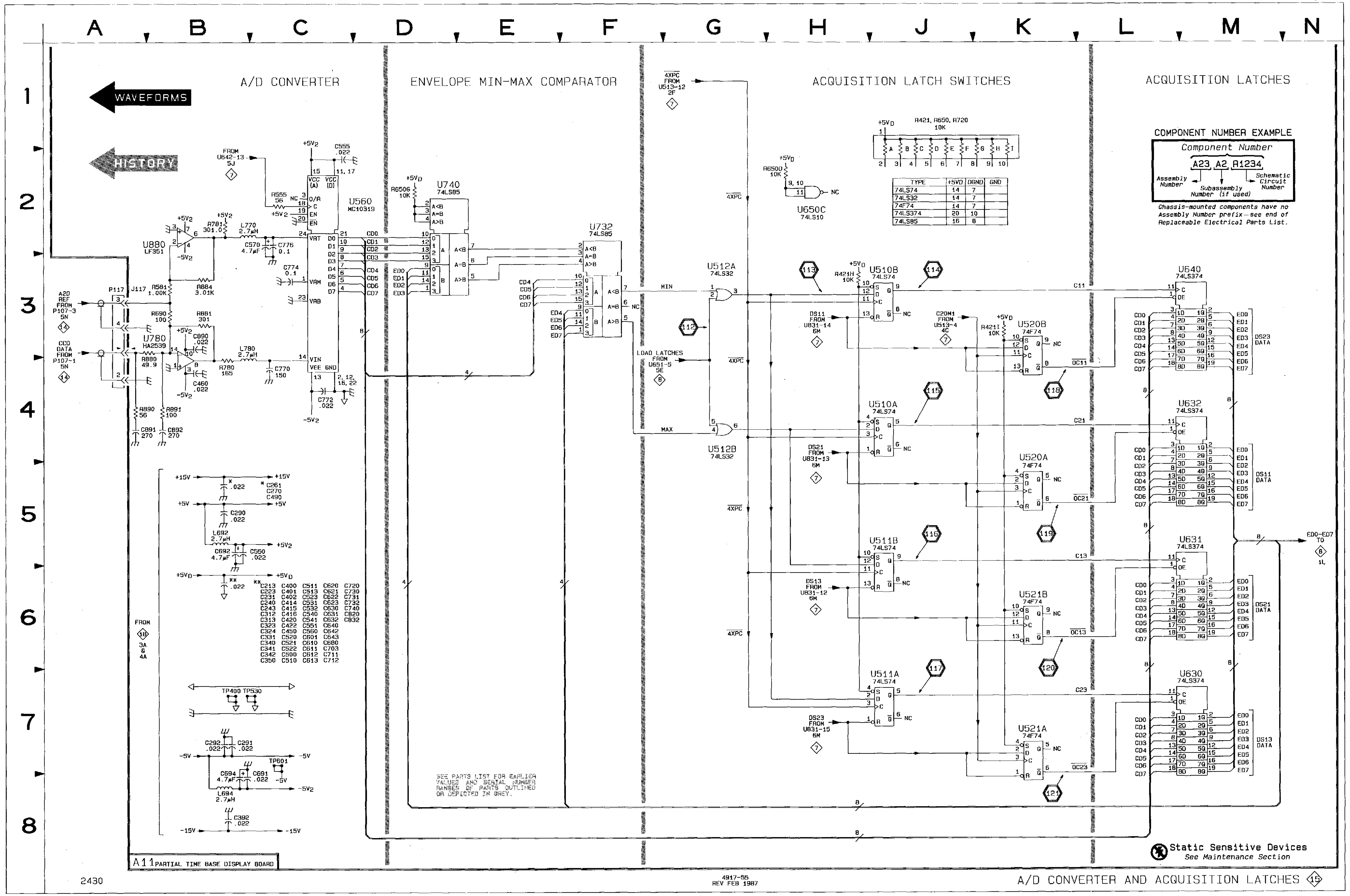
WAVEFORMS FOR DIAGRAM 15



2430 ENVELOPE MODE 100 µS/DIV



4917-83



A/D CONVERTER & ACQ. LATCHES

15

DISPLAY & ATTRIBUTES MEMORY DIAGRAM 16

ASSEMBLY A11

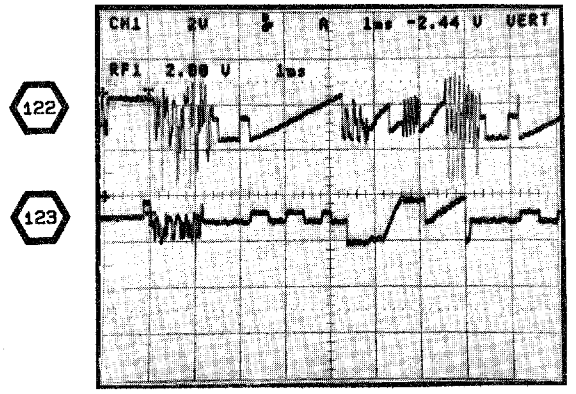
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C150	1L	1K	U322	2E	3F
C250	5L	2K	U323B	2B	3F
			U323C	5B	3F
J131	1A	1E	U323D	4B	3F
J131	7A	1E	U350A	2L	3K
			U350D	6L	3K
R151	1M	1K	U413B	4B	4E
R152	1M	1K	U421A	2C	4F
R155	5M	2K	U421B	2C	4F
R156	5M	2K	U421C	5C	4F
R450	8K	5K	U421D	4C	4F
			U422A	7B	4F
U130	7G	1H	U422B	7C	4F
U140	7J	1J	U422C	7C	4F
U141	2M	1J	U422D	6C	4F
U142	1M	1K	U423A	8D	5F
U240	7K	3J	U430	7E	4G
U241	2J	2J	U431	2E	4H
U243	4M	2K	U440	5E	4J
U250	5M	2K	U441	4J	4J
U314	4E	3E	U450C	8H	4K
U320	3G	3E			
U321	5G	3F	W140	8M	8K

Partial A11 also shown on diagrams 7, 8, 15, 17 and 18.

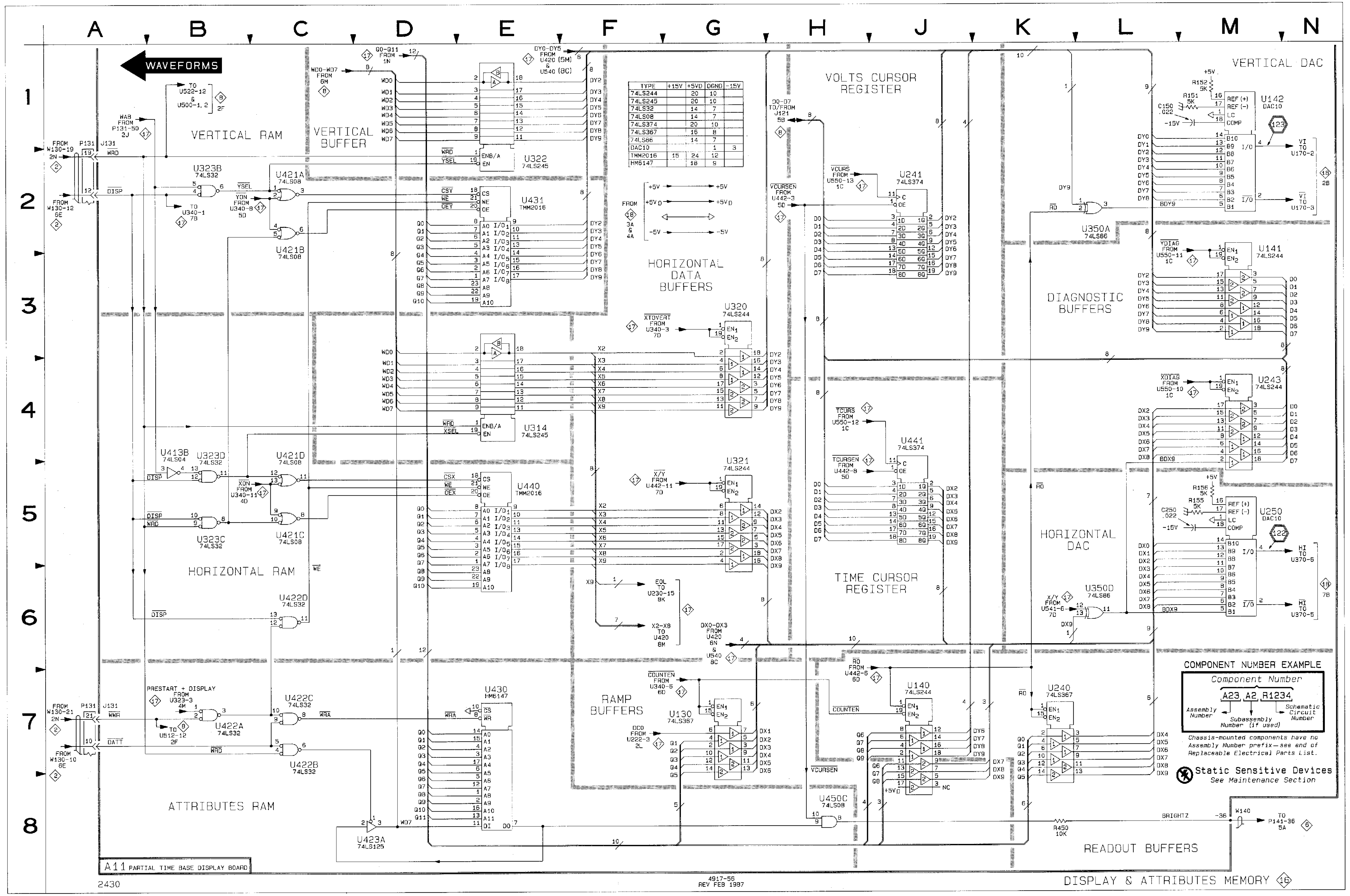
CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P131	1A	CHASSIS	P131	7A	CHASSIS

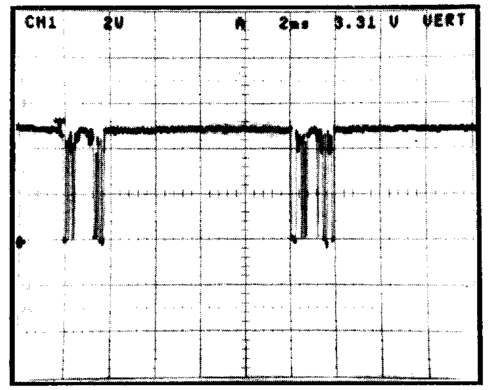
WAVEFORMS FOR DIAGRAM 16

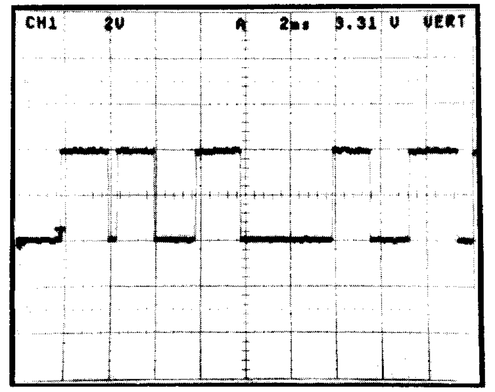


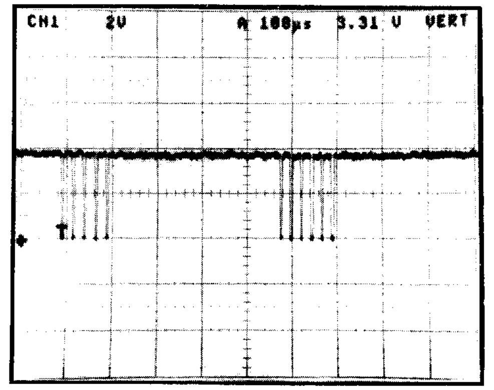
4917-84

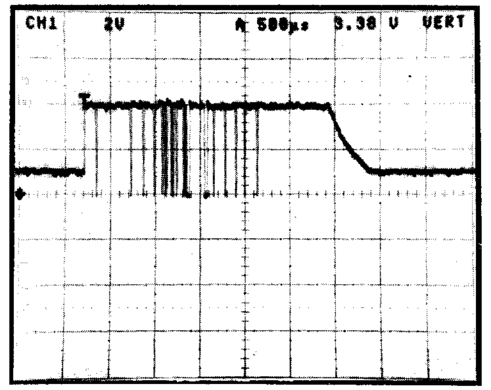


WAVEFORMS FOR DIAGRAM 17

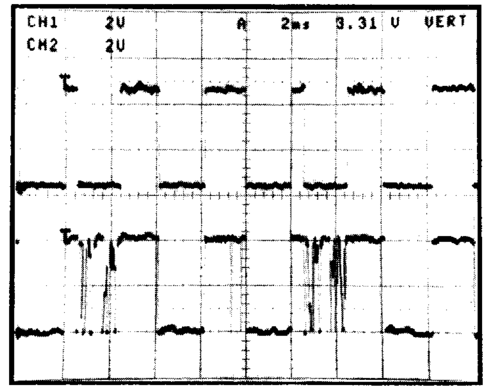
124


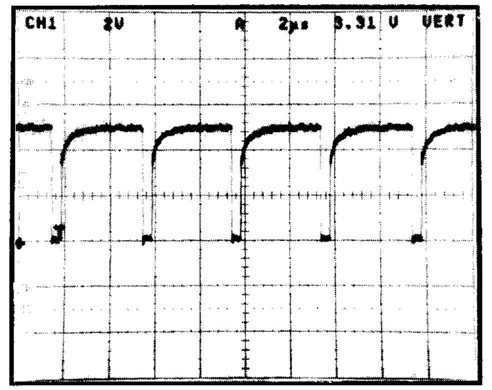
128


125


129


TEST SCOPE TRIGGERED ON 126

126
127


130


4917-85

DISPLAY CONTROL DIAGRAM 17

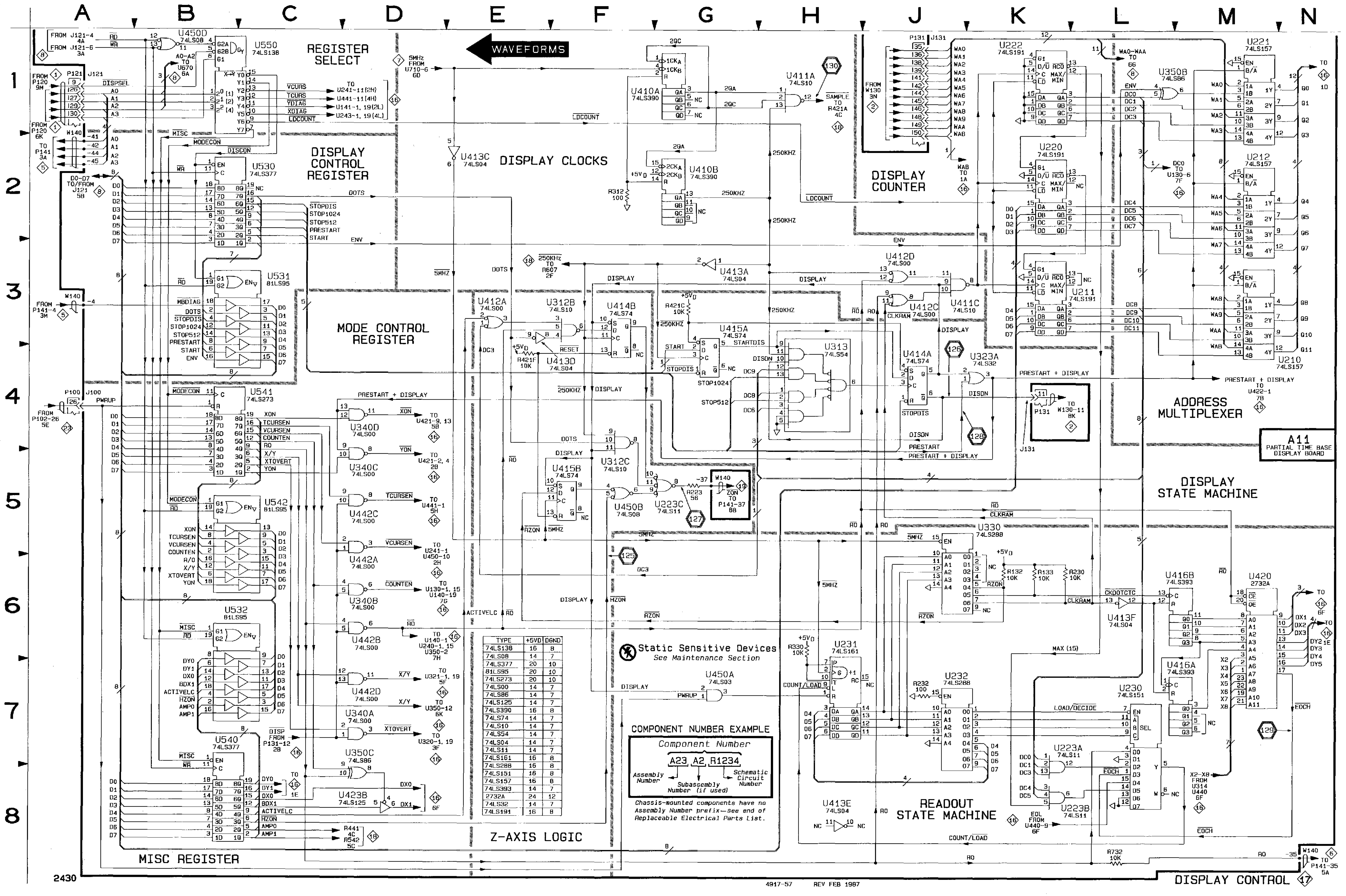
ASSEMBLY A11

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J100	4A	9D	U231	6H	3H	U414B	3F	5C
J121	1A	9L	U232	7J	3H	U415A	3G	5D
J131	1J	1E	U312B	3F	3D	U415B	5F	5D
J131	4K	1E	U312C	5F	3D	U416A	7N	5E
			U313	3H	3D	U416B	6M	5E
R132	6K	1H	U323A	4K	3F	U420	4M	4E
R133	6K	2H	U330	5K	3G	U423B	8D	5F
R223	5G	2F	U340A	7D	3K	U442A	6D	4K
R230	6L	2H	U340B	6D	3K	U442B	6D	4K
R232	7J	2H	U340C	5D	3K	U442C	5D	4K
R312	2F	3C	U340D	4D	3K	U442D	7D	4K
R330	6H	3H	U350B	1L	3K	U450A	7G	4K
R421C	3G	4E	U350C	7D	3K	U450B	5F	4K
R421F	4E	4E	U410A	1F	4C	U450D	1B	4K
R732	8L	8H	U410B	2G	4C	U530	2C	5G
			U411A	1H	4D	U531	3C	5H
U210	4N	2D	U411C	3J	4D	U532	6B	5H
U211	3L	2D	U412A	3E	4D	U540	7B	5J
U212	2M	2E	U412C	3J	4D	U541	4C	5J
U220	2K	2E	U412D	3J	4D	U542	5C	5J
U221	1M	2F	U413A	3G	4E	U550	1C	5K
U222	1K	2F	U413C	2E	4E			
U223A	7L	2F	U413D	4F	4E	W140	2A	8K
U223B	8L	2F	U413E	7F	4E	W140	3A	8K
U223C	5G	2F	U413F	6L	4E	W140	5G	8K
U230	7L	2G	U414A	4J	5C	W140	8N	8K

Partial A11 also shown on diagrams 7, 8, 15, 16 and 18.

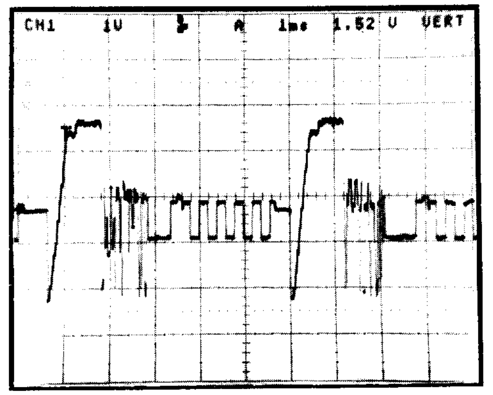
CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P100.	4A	CHASSIS	P131	1J	CHASSIS			
P121	,1A	CHASSIS	P131	4K	CHASSIS			

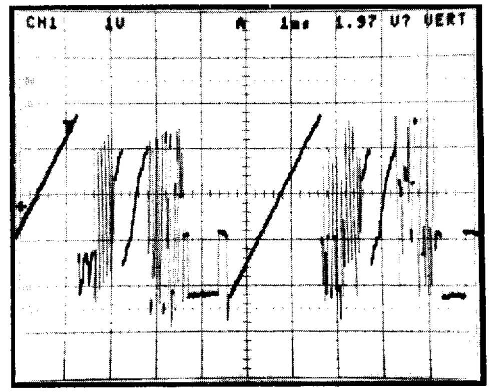


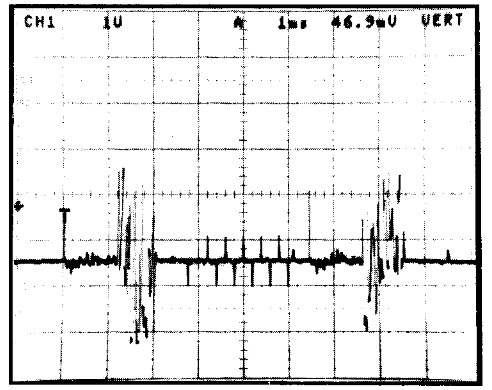
WAVEFORMS FOR DIAGRAM 18

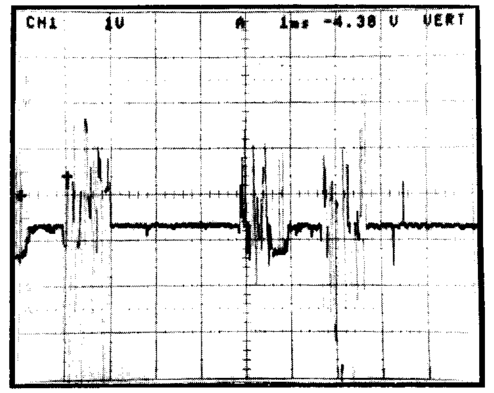
TEST SCOPE HF REJ COUPLING

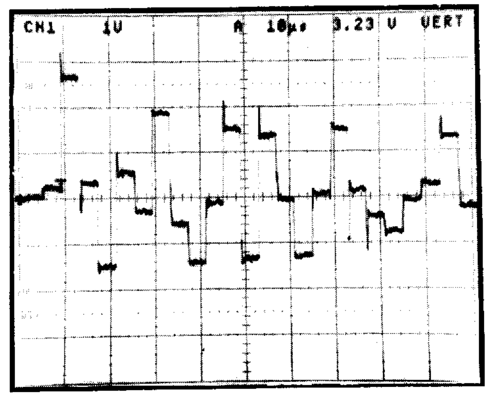
131


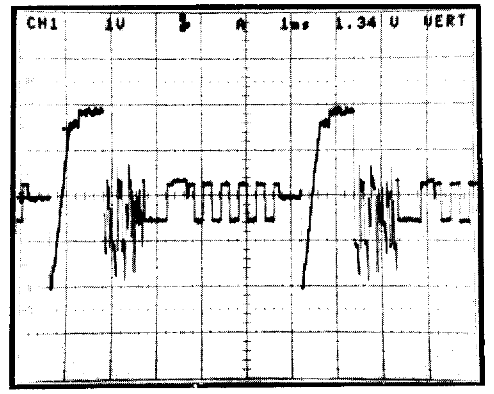
2430 TRIGGERED ON
AND DISPLAYING CAL SIGNAL
1 mS/DIV, 200 mV/DIV
TRIG POS 1/2, SAVE MODE

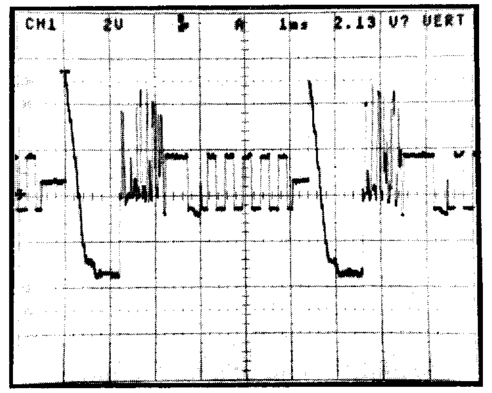
132


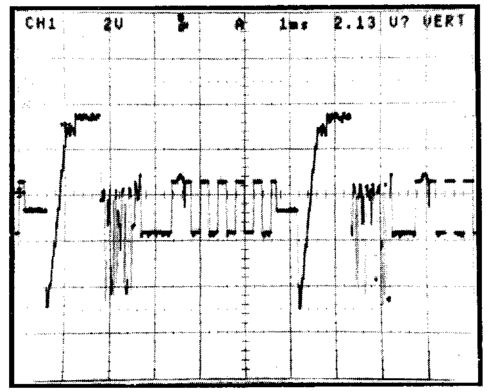
133


134


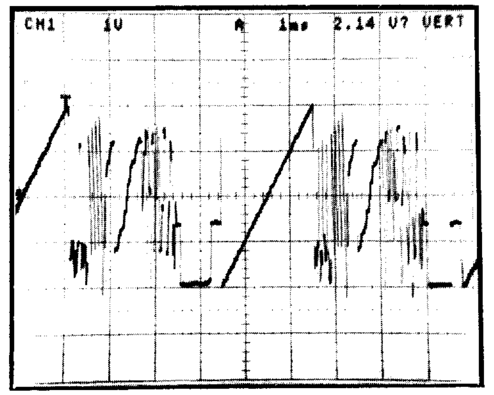
135


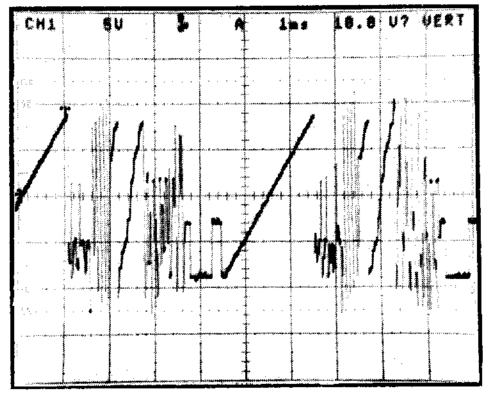
136


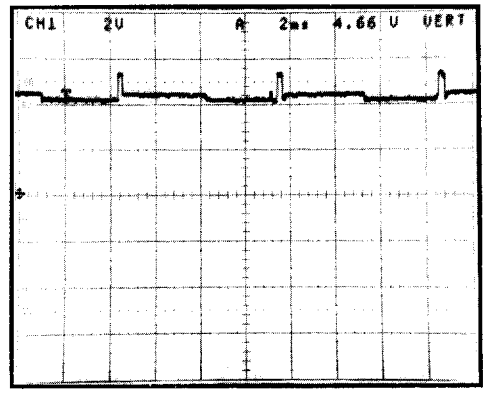
137


138


HF REJ COUPLING

139


140


141


MORE

4917-86

DISPLAY OUTPUT DIAGRAM 18

ASSEMBLY A11

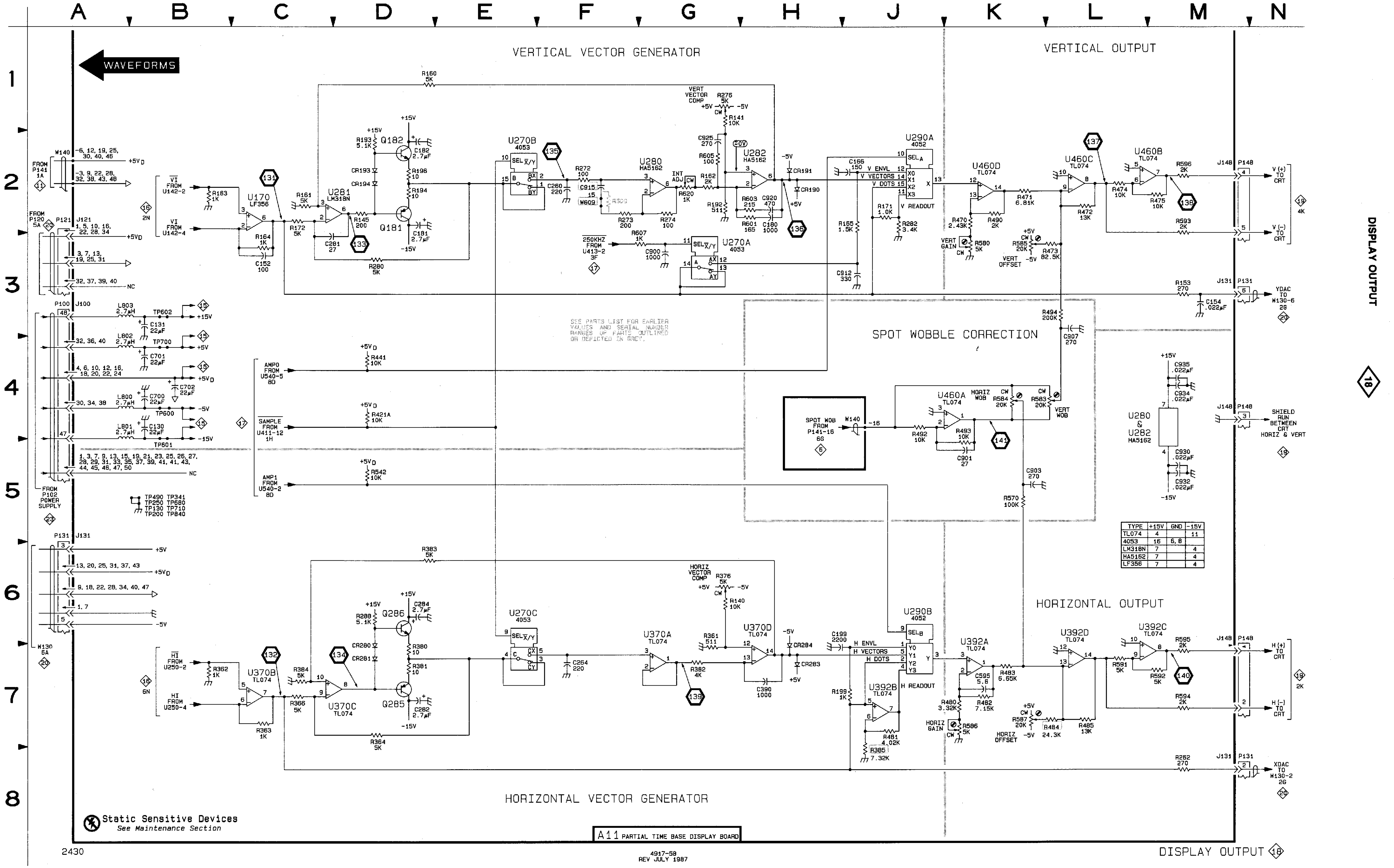
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C130	4B	1G	J131	5A	1E	R364	7D	4L	R605	2G	1M
C131	3B	1G	J131	8M	1E	R366	7C	4L	R607	2G	5E
C152	3C	1L	J148	2M	5M	R376	6G	3M	R609*	2F	1M
C154	3M	1K	J148	4M	5M	R380	7D	4M	R620	2G	1M
C166	2J	2M	J148	6M	5M	R381	7D	4M			
C180	2H	2M				R382	7G	3L	TP130	5B	2H
C181	2D	2L	L800	4A	8B	R383	6D	5M	TP200	5B	2C
C182	2D	2L	L801	4A	8B	R384	7C	5M	TP250	5B	2K
C199	6H	2M	L802	4A	8B	R385	7J	4M	TP341	5B	3J
C260	2F	2M	L803	3A	8B	R421A	4D	4E	TP490	5B	5M
C264	7F	3L				R441	4D	4J	TP600	4B	7A
C281	3D	2L	Q181	2D	2L	R470	2K	4L	TP602	3B	7A
C282	7D	4M	Q182	2D	2L	R471	2K	5L	TP680	5B	5K
C284	6D	4M	Q285	7D	4M	R472	2L	4L	TP700	4B	7A
C390	7H	3M	Q286	6D	4M	R473	3L	5L	TP710	5B	7D
C595	7K	5M				R474	2L	5L	TP840	5B	9J
C700	4B	8A	R140	6G	3M	R475	2M	4L			
C701	4B	8A	R141	6G	2M	R480	2K	5M	U170	2C	1L
C702	4B	8B	R145	2D	2L	R480	7K	5M	U270A	3G	3M
C900	3G	5F	R153	3M	1K	R481	7J	4M	U270B	2E	3M
C901	5K	4L	R160	1D	2L	R482	7K	5M	U270C	6E	3M
C903	5K	5M	R161	2C	1L	R483	7K	5M	U280	2G	1M
C907	3L	5L	R162	2G	1M	R484	7L	5M	U281	2D	1L
C912	3J	2M	R163	2B	1L	R485	7L	5M	U282	2H	2M
C915	2F	2M	R164	3C	1L	R490	2K	4L	U290A	2J	3M
C920	2H	2M	R165	2J	3M	R492	4J	4L	U290B	6J	3M
C925	2G	1M	R171	2J	3M	R493	4K	4L	U370A	6G	3M
C930	5M	2L	R172	2C	1L	R494	3L	5L	U370B	7C	3M
C932	5M	1M	R192	2G	2M	R542	5D	4J	U370C	7D	3M
C934	4M	1M	R193	2D	3L	R570	5K	5M	U370D	6H	3M
C935	4M	1L	R194	2D	2L	R580	3K	5L	U392A	6K	4M
			R196	2D	2L	R583	4K	5L	U392B	7H	4M
CR190	2H	2M	R199	7H	2M	R584	4K	6L	U392C	6M	4M
CR191	2H	2M	R262	8M	1G	R585	3K	6L	U392D	6L	4M
CR193	2D	3L	R272	2F	1L	R586	7K	5M	U460A	4K	4M
CR194	2D	3L	R273	2F	1M	R587	7K	6M	U460B	2M	4M
CR280	7D	4M	R274	2G	1M	R591	7L	5M	U460C	2L	4M
CR281	7D	4M	R276	1G	2M	R592	7M	5M	U460D	2K	4M
CR283	7H	3M	R280	3D	2L	R593	2M	6M			
CR284	7H	3M	R282	2J	3M	R594	7M	5M	W140	2A	8K
			R288	6D	5M	R595	6M	6M	W140	4J	8K
J100	3A	9D	R361	6G	3L	R596	2M	6M	W609*	2F	1M
J121	2A	9L	R362	7B	3L	R601	2H	2M			
J131	3M	1E	R363	7C	3L	R603	2H	2M			

Partial A11 also shown on diagrams 7, 8, 15, 16 and 17.

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P100	3A	CHASSIS	P131	3M	CHASSIS	P131	8M	CHASSIS	P148	4M	CHASSIS
P121	2A	CHASSIS	P131	5A	CHASSIS	P148	2M	CHASSIS	P148	6M	CHASSIS

***See Parts List for serial number ranges.**



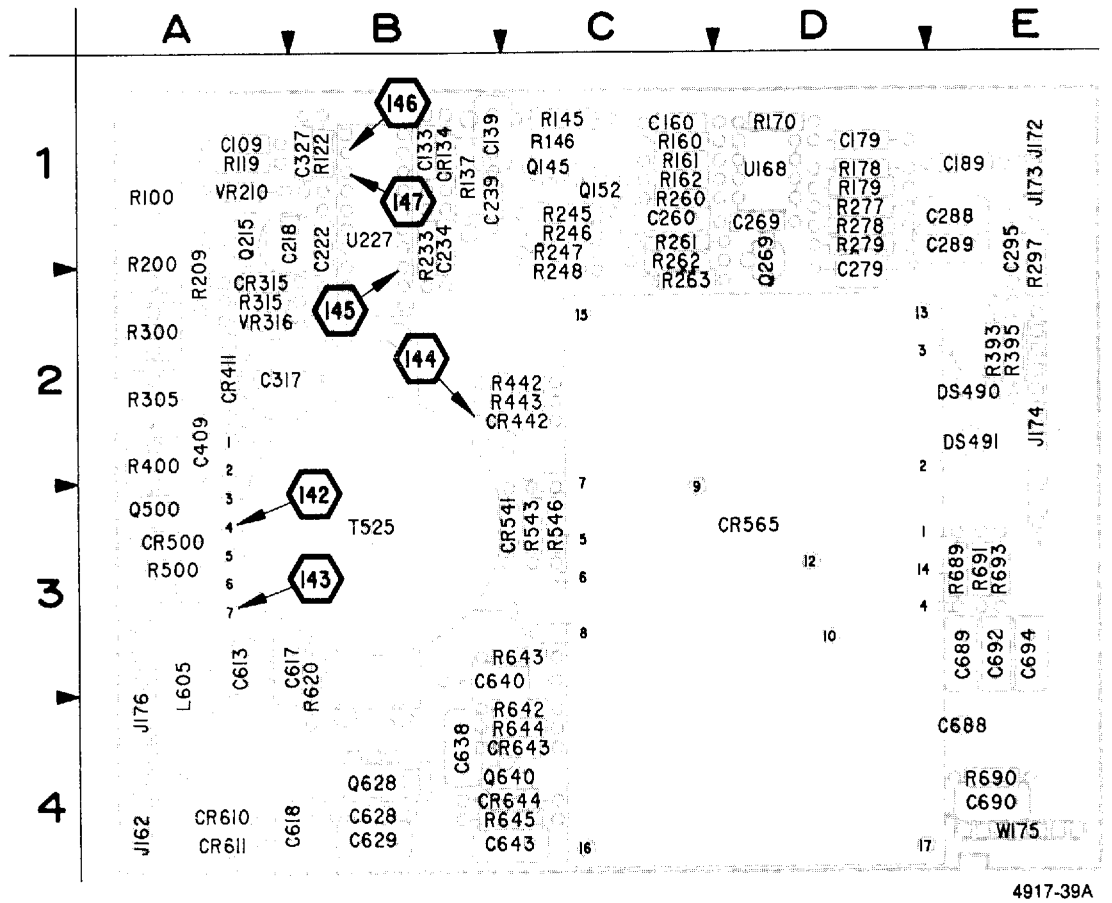


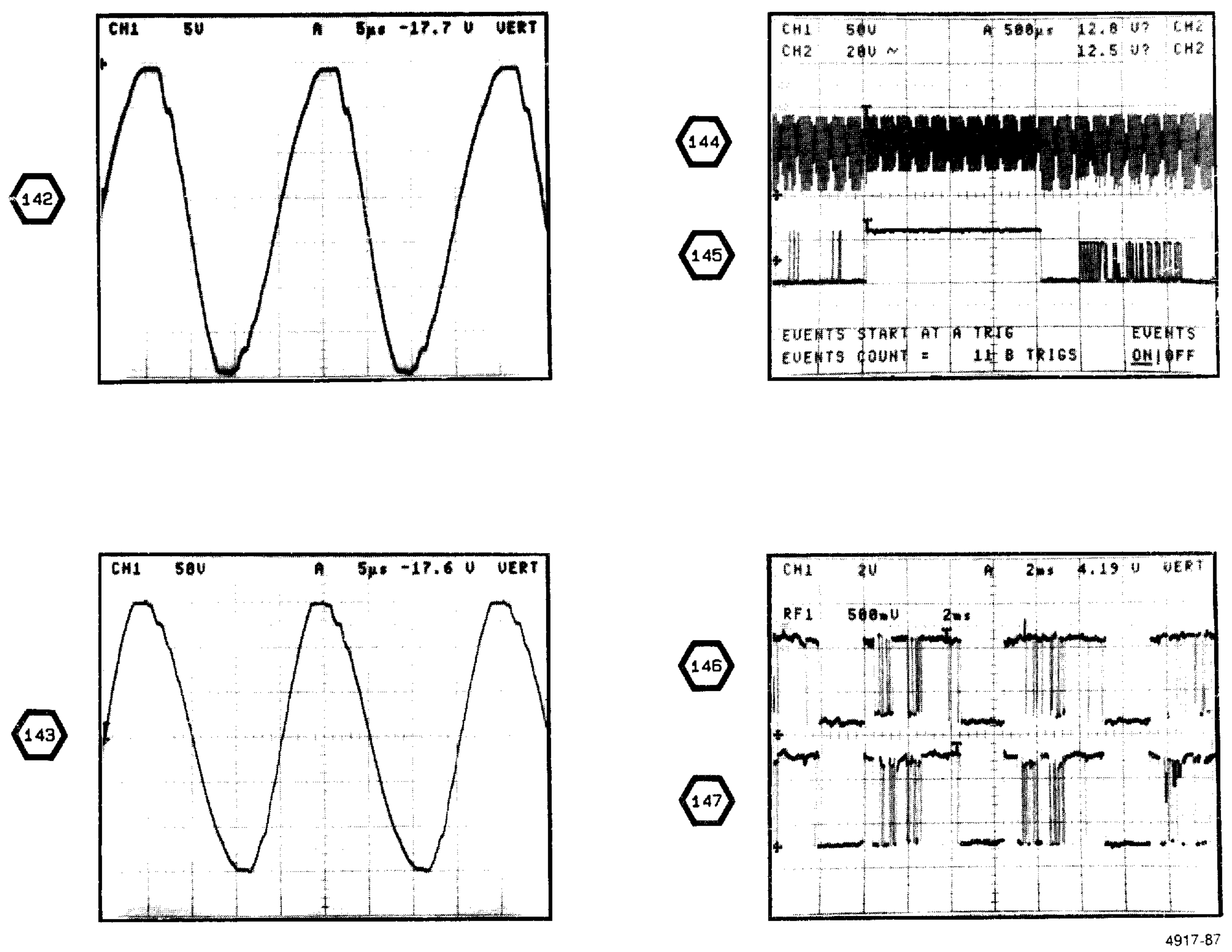
Figure 9-10. A17-High Voltage board.

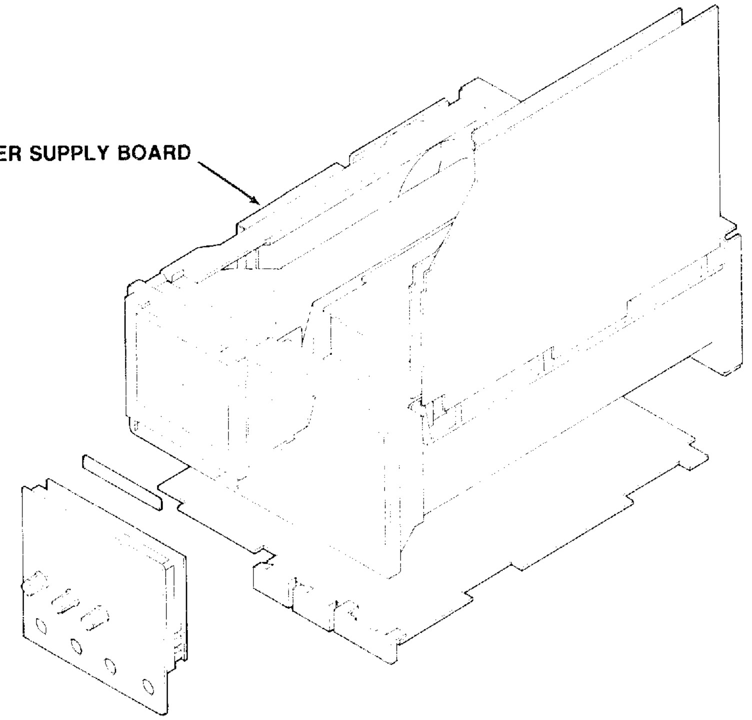
A17—HIGH VOLTAGE BOARD

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C109	19	C618	19	CR644	19	R122	19	R278	19	R691	19
C133	19	C628	19	DS490	19	R137	19	R279	19	R693	19
C139	19	C629	19	DS491	19	R145	19	R297	19	T525	19
C160	19	C638	19	J162	19	**R146***	**19**	R300	19	U168	19
C179	19	C640	19	J172	19	R160	19	R305	19	U168	19
C189	19	C643	19	J173	19	R161	19	R315	19	U227	19
C218	19	C688	19	J174	19	R162	19	R393	19	VR210	19
C222	19	C689	19	J176	19	R170	19	R395	19	VR316	19
C234	19	C690	19	L605	19	R178	19	R400	19	W175	19
C239	19	C692	19	Q145	19	R179	19	R442	19		
C260	19	C694	19	Q152	19	R200	19	R443	19		
C269	19	CR134	19	Q215	19	R209	19	R500	19		
C279	19	CR315	19	Q269	19	R233	19	R543	19		
C288	19	CR411	19	Q500	19	R245	19	R546	19		
C289	19	CR442	19	Q628	19	R246	19	R620	19		
C295	19	CR500	19	Q640	19	R247	19	R642	19		
C317	19	CR541	19	R100	19	R248	19	R643	19		
C327	19	CR565	19	R119	19	R260	19	R644	19		
C409	19	CR610	19			R261	19	R645	19		
C613	19	CR611	19			R262	19	R689	19		
C617	19	CR643	19			R263	19	R690	19		
						R277	19				

WAVEFORMS FOR DIAGRAM 19

TEST SCOPE A DELAY BY EVENTS





Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

Component Number
A23 A2 R1234
Assembly Number — Subassembly Number (if used) — Schematic Circuit Number

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts list.

HIGH VOLTAGE SUPPLY & CRT DIAGRAM 19

ASSEMBLY A10

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J105	1C	10E	J105	8C	10E	J108	1B	8B	J141	8B	2L

Partial A10 also shown on diagrams 5, 6, 9, 10, 11, 12, 13 and 14.

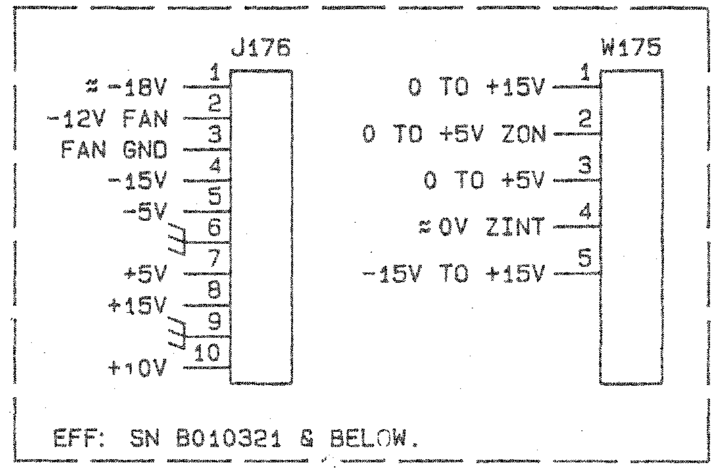
ASSEMBLY A17

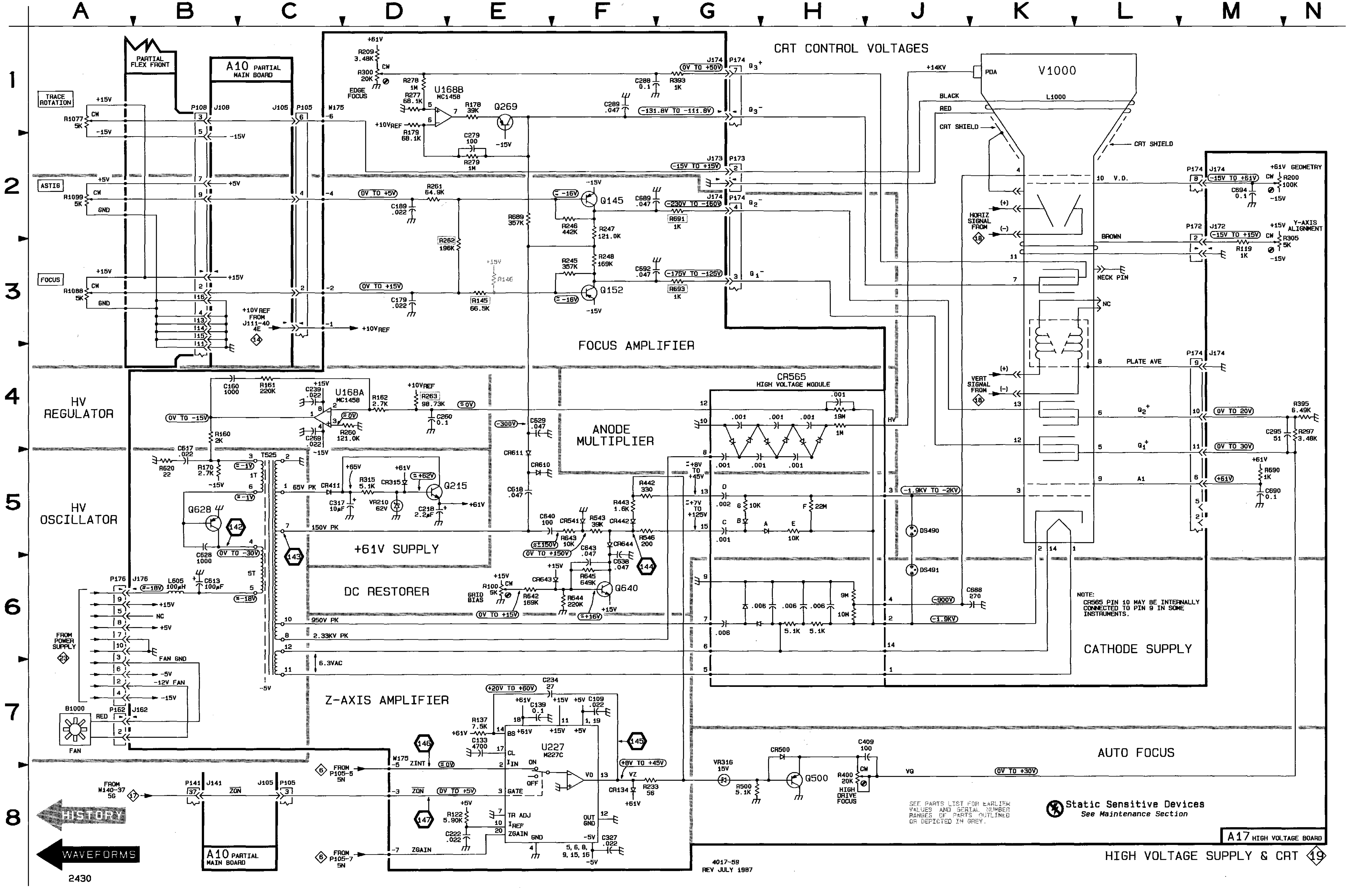
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C109	7F	1A	CR134	8F	1B	Q640	6F	4C	R393	1F	2E
C133	7E	1B	CR315	5D	2A				R395	4N	2E
									R400	8H	2A
C139	7E	1B	CR411	5C	2A	R100	6E	1A	R442	5E	2C
C160	4B	1C	CR442	5E	2C	R119	3M	1A	R443	5E	2C
C179	3D	1D	CR500	7H	3A	R122	8E	1B	R500	7G	3A
C189	2D	1E	CR541	5E	3B	R137	7E	1B	R543	5E	3C
C218	5D	1A	CR565	4H	2C	R145	3E	1C	R546	5E	3C
C222	8E	1B	CR610	5E	4B	R146*	3E	1C	R620	4B	3B
C234	7F	1B	CR611	5E	4B	R160	4B	1C	R642	6E	4C
C239	4C	1B	CR643	6E	4C	R161	4C	1C	R643	5E	3C
C260	4D	1C	CR644	5E	4C	R162	4D	1C	R644	6F	4C
C269	4C	1D				R170	4B	1D	R645	6F	4C
C279	2E	2D	DS490	5J	2E	R178	1E	1D	R689	2E	3E
C288	1F	1E	DS491	6J	2E	R179	1D	1D	R690	5M	4E
C289	1F	1E				R200	2N	2A	R691	2G	3E
C295	4M	1E	J162	7B	4A	R209	1D	2A	R693	3G	3E
C317	5C	2A	J172	2M	1E	R233	8F	1B			
C327	8F	1B	J173	2G	1E	R245	3F	1C	T525	5C	3B
C409	7J	2A	J174	1G	3E	R246	2F	1C			
C613	6B	3A	J174	2G	3E	R247	2F	1C	U168A	4D	1D
C617	4B	3A	J174	2M	3E	R248	3F	2C	U168B	1E	1D
C618	5E	4A	J174	4M	3E	R260	4D	1C	U227	7F	1B
C628	4B	4B	J176	6B	4A	R261	2D	1C			
C629	4E	4B				R262	3E	2C	VR210	5D	1A
C638	6F	4B	L605	6B	3A	R263	4D	2C	VR316	7G	2B
C640	5E	3B				R277	1D	1D			
C643	5F	4C	Q145	2F	1C	R278	1D	1D	W175	1C	4E
C688	6K	4E	Q152	3F	1C	R279	2E	1D	W175	8D	4E
C689	2F	3E	Q215	5E	1A	R297	4N	1E			
C690	5M	4E	Q269	1E	1D	R300	1D	2A			
C692	3F	3E	Q500	8H	3A	R305	2N	2A			
C694	2M	3E	Q628	4B	4B	R315	5D	2A			

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
B1000	7A	CHASSIS	P108	1B	CHASSIS	P174	2G	CHASSIS	R1088	3A	CHASSIS
			P141	8B	CHASSIS	P174	2M	CHASSIS	R1099	2A	CHASSIS
L1000	1K	CHASSIS	P162	7A	CHASSIS	P174	4M	CHASSIS			
			P172	2M	CHASSIS	P176	6A	CHASSIS	V1000	1K	CHASSIS
P105	1C	CHASSIS	P173	2G	CHASSIS						
P105	8C	CHASSIS	P174	1G	CHASSIS	R1077	1A	CHASSIS			

***See Parts List for serial number ranges.**

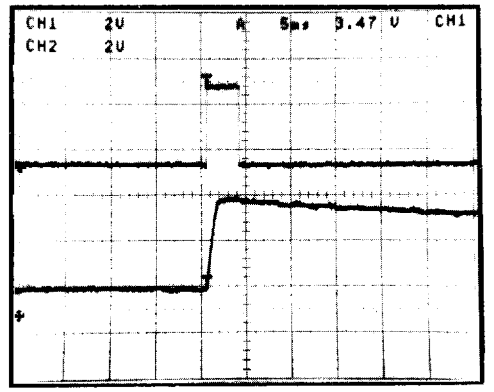




WAVEFORMS FOR DIAGRAM 20

TEST SCOPE IN NORM TRIGGER

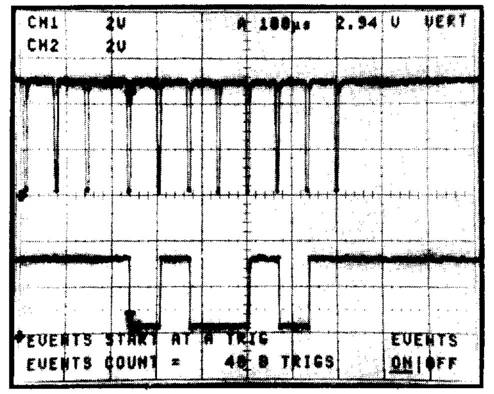
148
149



PRESS GPIB TRANSMIT TO RING BELL ON 2430

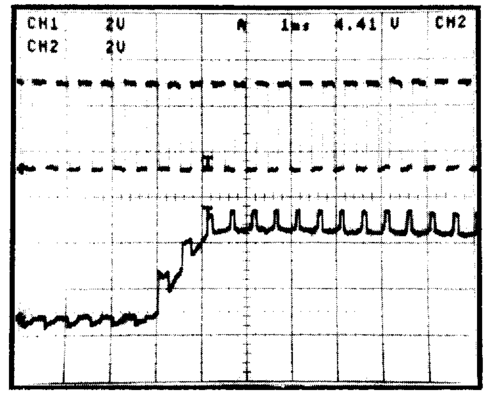
EVENTS SOURCE CH 1

152
CH 1 SIGNAL
154



154 IS LAST BYTE OUT

150
151

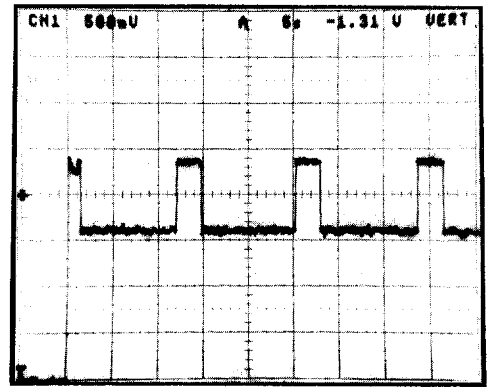


NORM TRIGGER ON 151 +SLOPE LEVEL 4.4

PRESS GPIB TRANSMIT TO RING BELL ON 2430

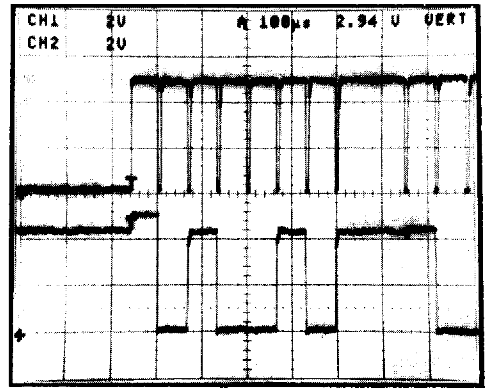
TEST SCOPE IN ROLL MODE

155



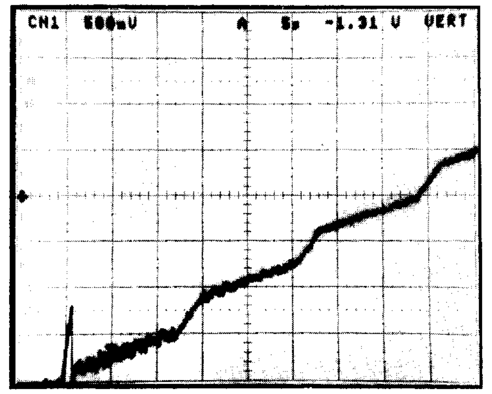
CAL SIGNAL INPUT 1ms/DIV
200mV/DIV FOR 155 and 156

152
153



153 IS FIRST BYTE IN

156



4917-88

SYSTEM I/O DIAGRAM 20

ASSEMBLY A12

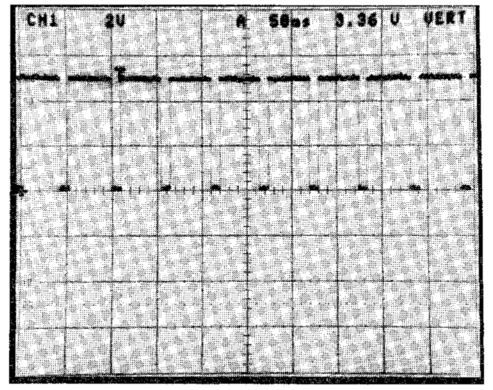
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C116	3B	1B	C646	3C	6F	L984	3B	8L	R718	4K	7C
C118	2K	1B	C670	3C	6J	L990	2B	8L	R722	4J	7C
C120	2K	1D	C720	3C	7C	L992	4B	9L	R792	6K	7M
C122	4C	1D	C748	4C	7F				R794	6K	7M
C124	4C	1D	C764	3C	7J	LS498	1D	4M	R796	6K	7M
C150	3A	1G	C766	3C	7J						
C202	4L	2A	C774	4C	7K	Q402	1J	4A	TP332	4B	3E
C204	4L	2A	C780	4C	7K	Q588	1B	5L	TP372	4B	3J
C206	5L	2A	C790	3C	7L	Q592	1C	5M	TP572	4B	5J
C208	2H	2A	C850	3C	8G	Q594	1C	5M	TP574	4B	5J
C210	2J	2B	C862	4C	8H	Q596	1B	5M	TP774	4B	7K
C238	3C	2E	C882	3B	8L	Q720	4K	7D	TP902	4B	9A
C336	3C	3E	C884	2B	8L						
C348	3C	3F	C886	4B	8L	R104	2K	1B	U120A	2J	1C
C358	3C	3G	C894	3C	8M	R106	2K	1B	U120B	2J	1C
C360	3C	3H	C936	2B	9E	R116	2K	1C	U120C	2K	1C
C370	3C	3J	C964	3A	8J	R120	2K	1D	U120D	2K	1C
C372	2A	3K	C980	4C	8K	R122	1H	1D	U130	1H	1E
C374	2B	3K				R124	1H	1D	U264D	5D	3J
C386	3C	3L	CR300	1K	4A	R130	2H	1D	U270F	5E	3J
C452	3C	4G	CR400	1K	4A	R132	1H	1D	U274	2B	2K
C462	3C	4H	CR594	2D	5M	R140	2G	1F	U332B	7C	3E
C464	3C	4J	CR722	3J	7C	R142	2G	1F	U332C	8D	3E
C466	4C	4J	CR992	3B	9L	R274	1A	2K	U532	8E	5E
C472	3B	4J				R276	2A	2K	U624	5E	6D
C474	3C	4K	J103	2A	9K	R300	1L	4A	U630	5D	6E
C484	3C	4L	J120	4J	9C	R332	8D	3E	U720	5F	7D
C532	4C	5E	J120	5A	9C	R400	1J	4A	U750	7J	7G
C532	4C	5E	J125	4H	3A	R592	2C	5M	U754	5J	7G
C542	3C	5F	J125*	1L	3A	R594	1C	5M	U844D	4J	8F
C550	4C	5G	J181	2F	8C	R596	1B	5M			
C572	4C	5K	J207	6L	9M	R597	1B	5M	VR717	3K	7C
C580	4C	5K				R598	1B	5M			
C590	1C	5M	K302	1K	3A	R628	4C	6C	W130	2G	1J
C592	3C	5M				R716	3K	7C	W130	5A	1J
C626	3C	6D	L976	4B	8K	R717	3K	7C			

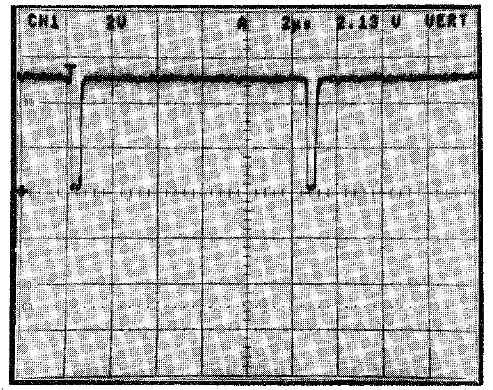
Partial A12 also shown on diagrams 1, 2 and 21.

CHASSIS MOUNTED PARTS

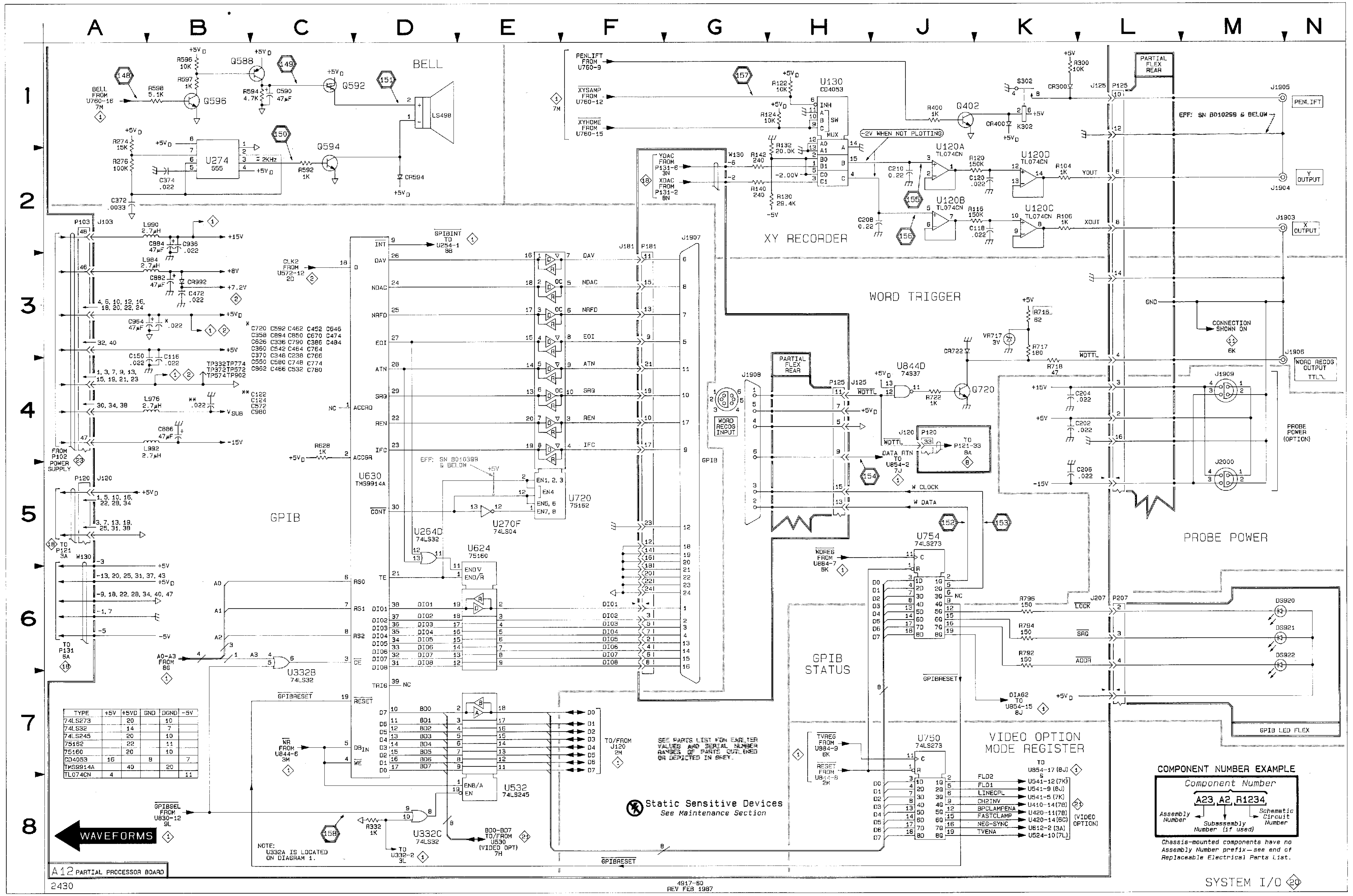
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J1903	2M	CHASSIS	J1908	4G	CHASSIS	P103	2A	CHASSIS	P181	2F	CHASSIS
J1904	2M	CHASSIS	J1908	5M	CHASSIS	P120	4J	CHASSIS	P207	6L	CHASSIS
J1905	1M	CHASSIS	J1909	4M	CHASSIS	P120	5A	CHASSIS			
J1906	3N	CHASSIS	J2000	5M	CHASSIS	P125	1L	CHASSIS			
J1907	2G	CHASSIS				P125	4H	CHASSIS			

***See Parts List for serial number ranges.**

157


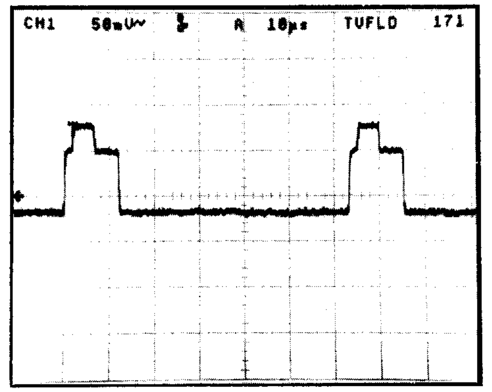
158


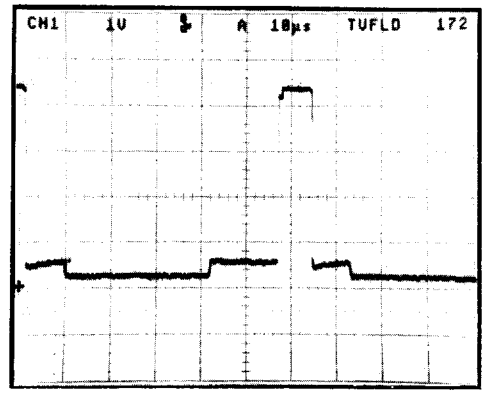
GRAT & READOUT OFF
ACQUIRING GROUND LEVEL

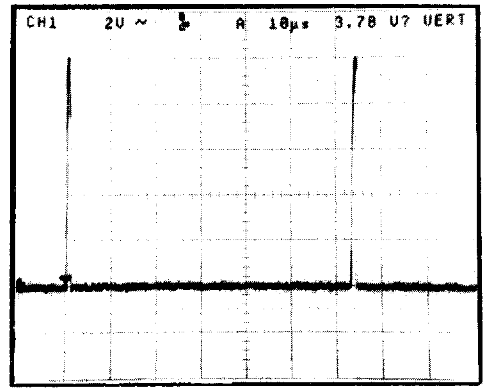


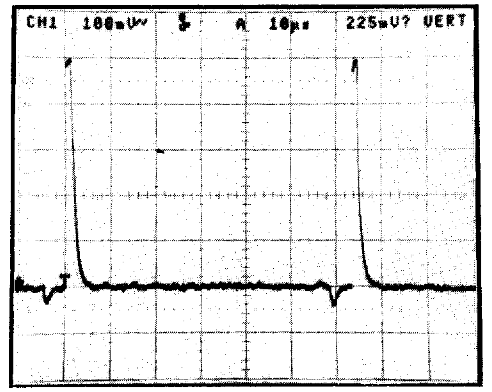
WAVEFORMS FOR DIAGRAM 21

BW LIMIT;
20 MHz ON TEST SCOPE

159


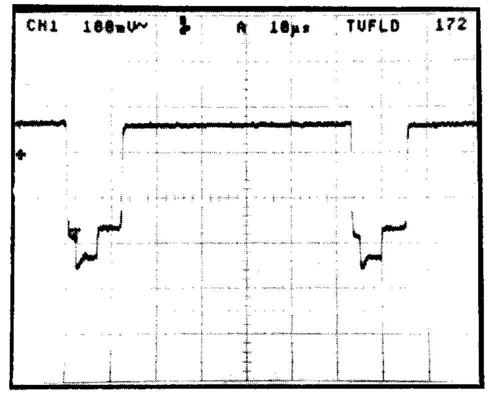
162


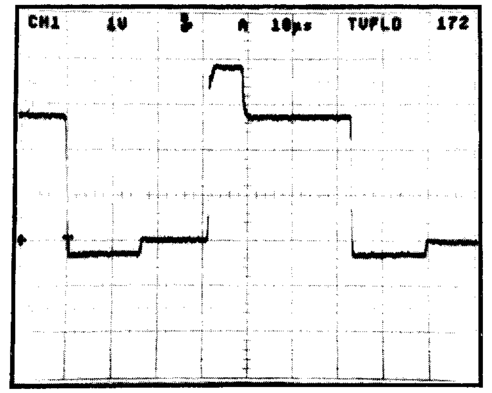
165


168


TV CLAMP ON; CH 2 INVERT ON

COMPOSITE FLAT-FIELD NEG-SYNC VIDEO SIGNAL APPLIED TO CH 2 INPUT OF 2430. TRIG SOURCE, CH 2; TRIG CPLG, TV; A TV COUPLING, ALT.

160


163


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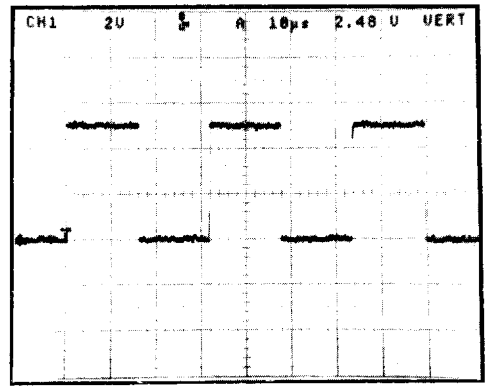

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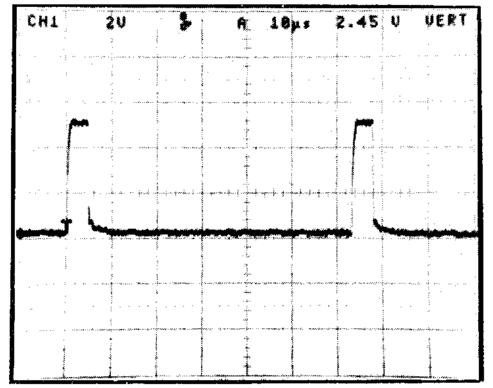

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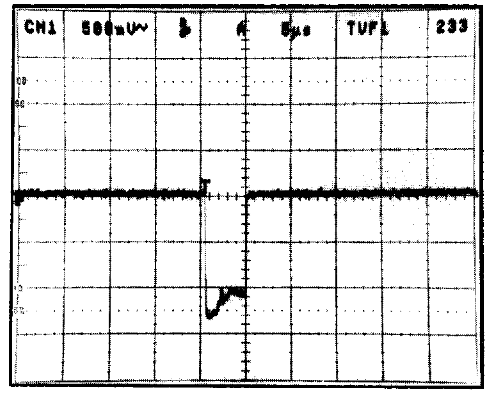

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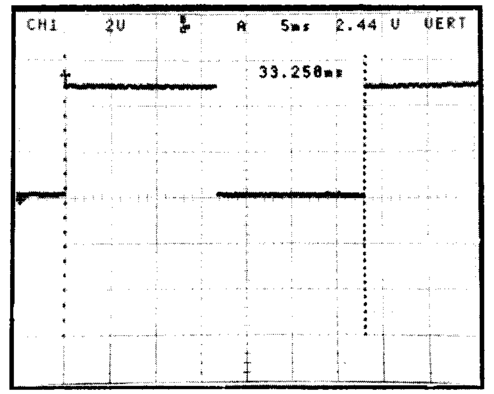

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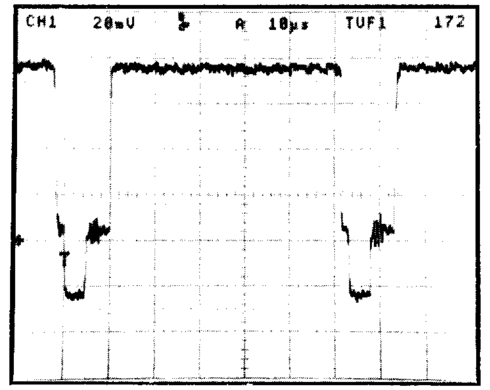

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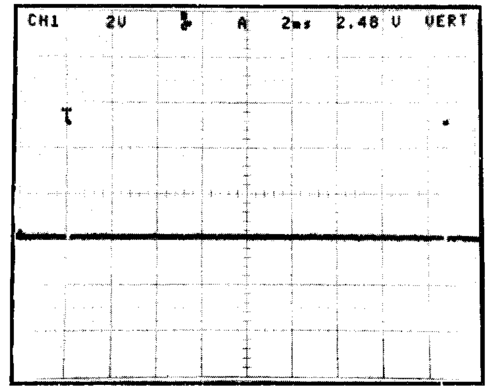


MORE

4917-90

VIDEO OPTION DIAGRAM 21

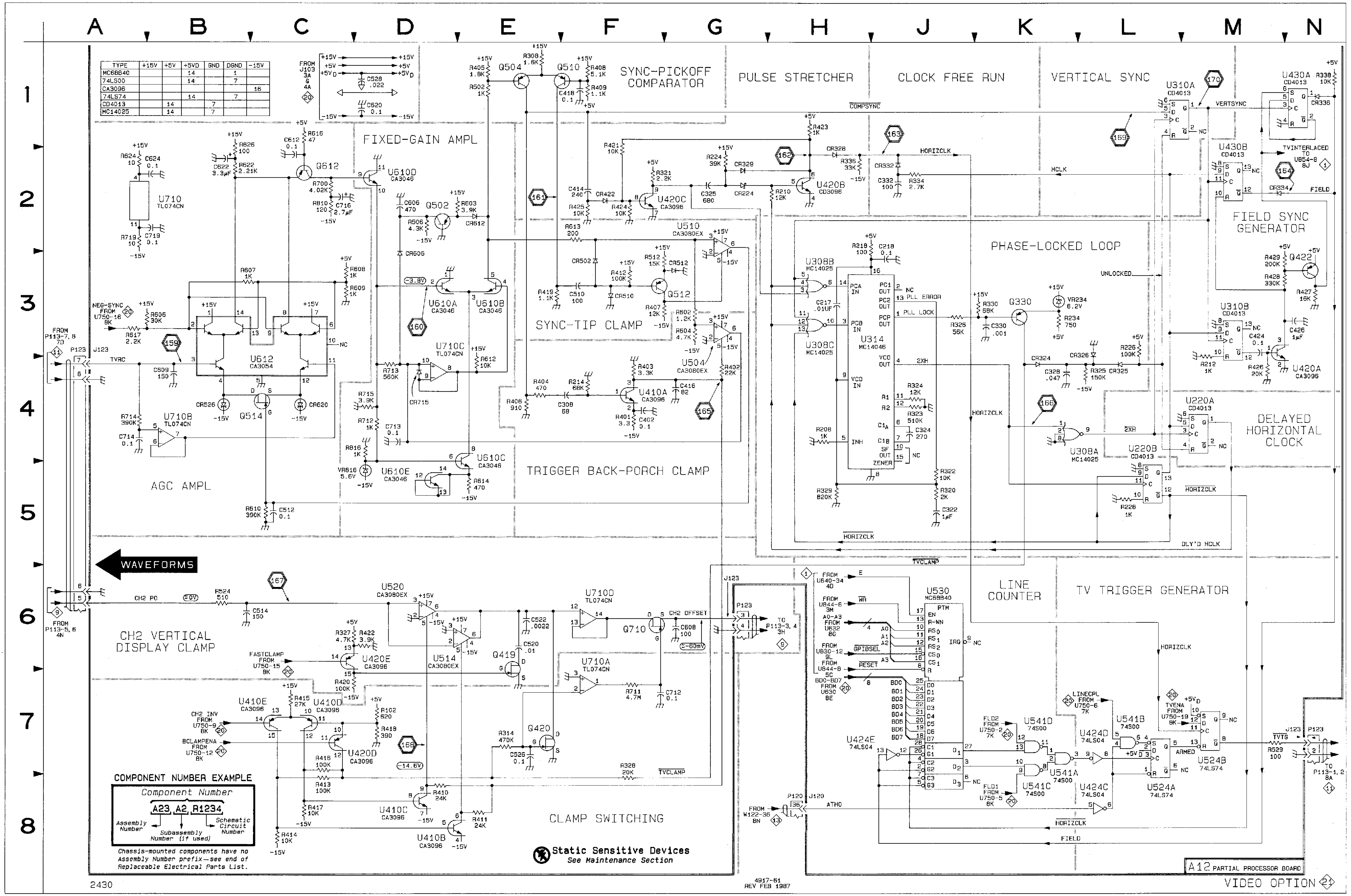
ASSEMBLY A12

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C217	3H	2C	CR715	4D	7C	R408	1F	4A	R816	4D	7B
C218	2J	3C				R409	1F	4A			
C308	4F	3B	J120	8H	9C	R410	8D	4B	U220A	4M	3D
C322	5J	3C	J123	3A	5C	R411	8E	4B	U220B	4L	3D
C324	4J	3C	J123	6G	5C	R412	3F	4B	U308A	4L	3B
C325	2G	3C	J123	7N	5C	R413	8C	4C	U308B	3H	3B
C328	4K	3D				R414	8C	4C	U308C	3H	3B
C330	3K	3E	Q330	3K	3D	R415	7C	4C	U310A	1L	3B
C332	2J	3E	Q419	6E	4C	R416	7C	4C	U310B	3M	3B
C402	4F	4B	Q420	7E	4C	R417	8C	4C	U314	3J	3B
C414	2F	4C	Q422	3N	4C	R418	7D	4C	U410A	4F	4B
C416	4G	4C	Q502	2D	5A	R419	3E	4C	U410B	8D	4B
C418	1F	4C	Q504	1E	5B	R420C	2G	4D	U410C	8D	4B
C424	3M	4D	Q510	1F	5B	R420	7C	4D	U410D	7C	4B
C426	3N	4D	Q512	3G	5B	R421	1F	4D	U410E	7C	4B
C510	3F	5B	Q514	4C	5B	R422	6D	4D	U420A	4N	4C
C512	5C	5B	Q612	2C	6C	R423	1H	4D	U420B	2H	4C
C514	6C	5C	Q710	6F	7B	R424	2F	4D	U420C	2G	4C
C520	6E	5C				R425	2F	4D	U420D	7D	4C
C522	6E	5C	R102	7D	1A	R426	4M	4D	U420E	6D	4C
C526	7E	5D	R208	4H	3A	R427	3N	4D	U424C	8L	5D
C528	1D	5C	R210	2H	2B	R428	3M	4D	U424D	7L	5D
C606	2D	6B	R212	4M	2B	R429	3M	4D	U424E	7H	5D
C608	6G	6B	R214	4F	3B	R502	1E	5A	U430A	1N	4E
C609	4B	6B	R218	2H	2C	R506	2D	5B	U430B	1M	4E
C612	1C	6C	R224	2G	2C	R512	3F	5C	U504	4G	5B
C620	1D	6C	R226	3L	2D	R524	6B	5C	U510	2G	5B
C622	2B	6C	R228	5L	3D	R529	7M	5D	U514	6D	5C
C624	2B	7C	R234	3K	3E	R602	3G	6B	U520	6D	5C
C712	7G	7B	R308	1E	3B	R603	2E	6B	U524A	8L	5D
C713	4D	7B	R314	7E	3C	R604	3G	6B	U524B	7M	5D
C714	4A	7B	R320	5J	3C	R606	3B	6B	U530	6J	5E
C716	2C	8D	R321	2F	3C	R607	3B	6B	U541A	7K	5F
C719	2B	7C	R322	5J	3C	R608	3D	6B	U541B	7L	5F
			R323	4J	3C	R609	3D	6B	U541C	8K	5F
CR224	2G	2C	R324	4J	3C	R610	5C	6B	U541D	7K	5F
CR324	3K	3D	R325	4L	3D	R612	4E	6B	U610A	3D	6B
CR325	4L	3D	R326	3J	3D	R613	2F	6B	U610B	3E	6B
CR326	3L	3D	R327	6C	3D	R614	5E	6B	U610C	4E	6B
CR328	1H	3D	R328	7F	3D	R616	1C	6C	U610D	2D	6B
CR329	2G	3D	R329	5H	3C	R617	3A	6C	U610E	5D	6B
CR332	2J	3E	R330	3K	3E	R622	2B	6C	U612	4C	6C
CR334	2M	3E	R334	2J	3E	R624	2A	7C	U710A	6F	7C
CR336	1N	3E	R336	2H	3E	R626	1B	6C	U710B	4B	7C
CR422	2F	4D	R338	1N	3E	R700	2C	7B	U710C	3D	7C
CR502	3F	5A	R401	4F	4B	R711	7F	7B	U710D	6F	7C
CR510	3F	5B	R402	4G	4B	R712	4D	7B			
CR512	3G	5C	R403	4F	4B	R713	4D	7B	VR234	3K	2E
CR526	4B	5C	R404	4E	4B	R714	4A	7B	VR816	5C	8B
CR606	3D	6B	R405	1E	4B	R715	4D	7C			
CR612	2E	6B	R406	4E	4B	R719	2A	7C			
CR620	4C	6C	R407	3F	4A	R810	2C	7B			

Partial A12 also shown on diagrams 1, 2 and 20.

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P120	8H	CHASSIS	P123	3A	CHASSIS	P123	6G	CHASSIS	P123	7N	CHASSIS



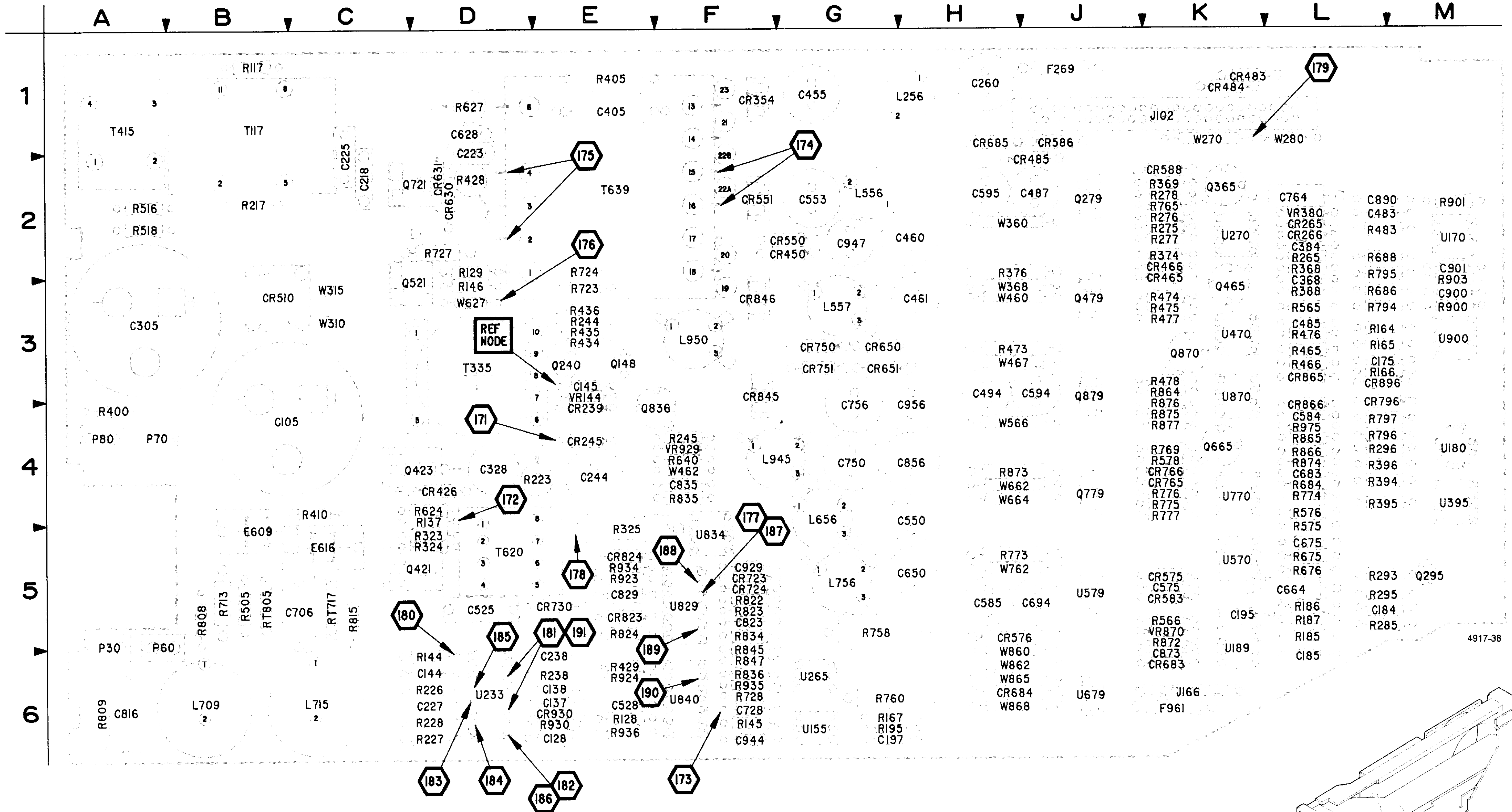
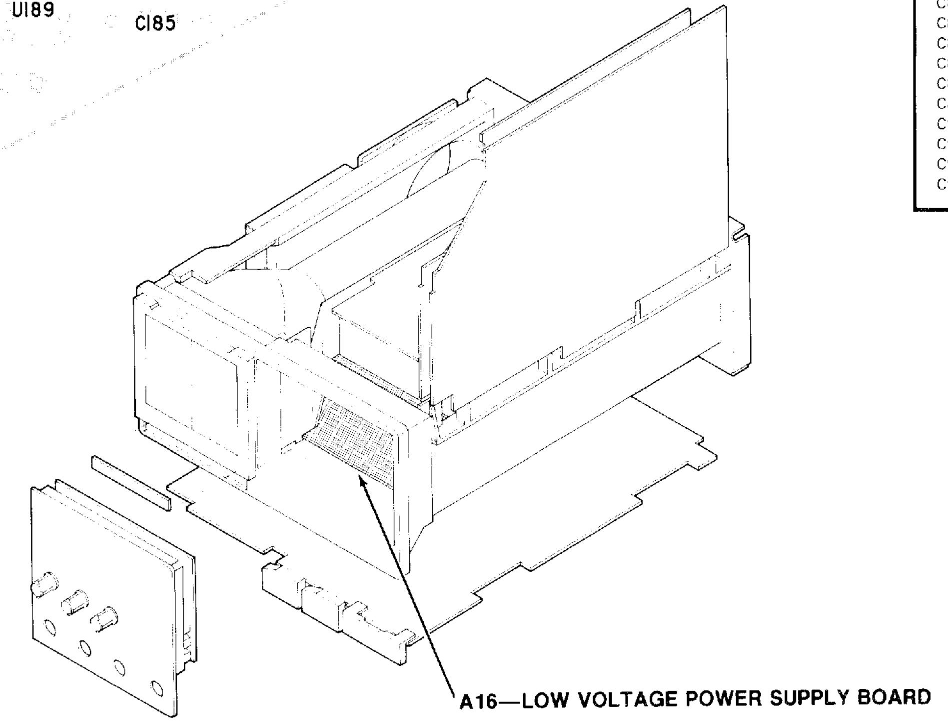


Figure 9-11. A16-Power Supply board

A16—POWER SUPPLY BOARD

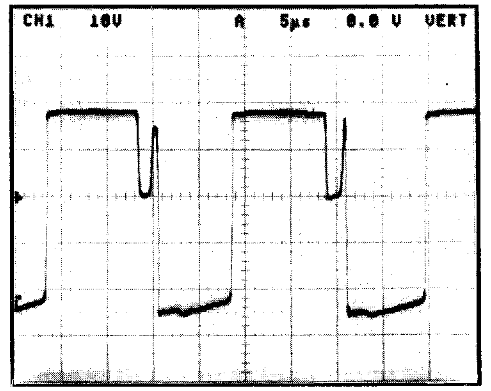
CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C105	22	C947	22	J166	23	R296	23	R796	23	U834	22
C128	22	C956	22	L256	22	R323	22	R797	23	U834	22
C137	22	CR239	22	L556	22	R324	22	R808	22	U840	22
C138	22	CR245	22	L557	22	R325	22	R809	22	U840	22
C144	22	CR265	23	L656	22	R368	23	R815	22	U840	22
C145	22	CR266	23	L709	22	R369	23	R822	22	U840	22
C175	23	CR354	22	L715	22	R374	23	R823	22	U870	23
C184	23	CR426	22	L756	22	R376	23	R824	22	U870	23
C185	23	CR450	22	L945	22	R388	23	R834	22	U900	23
C195	23	CR465	23	L950	22	R394	23	R835	22	VR144	22
C197	23	CR466	23	P30	22	R395	23	R836	22	VR380	23
C218	22	CR483	23	P60	22	R396	23	R845	22	VR870	23
C223	22	CR484	23	P70	22	R400	22	R847	22	VR929	22
C225	22	CR485	23	P80	22	R405	22	R864	23	W270	22
C227	22	CR510	22	Q148	22	R410	22	R865	23	W280	22
C238	22	CR550	22	Q240	22	R428	22	R866	23	W310	22
C244	22	CR551	22	Q279	23	R429	22	R872	23	W315	22
C260	22	CR575	23	Q295	23	R434	22	R873	23	W360	22
C305	22	CR576	23	Q365	23	R435	22	R874	23	W368	23
C328	22	CR583	23	Q421	22	R436	22	R875	23	W460	22
C368	23	CR586	23	Q423	22	R465	23	R876	23	W462	22
C384	23	CR588	23	Q465	23	R466	23	R877	23	W467	23
C405	22	CR630	22	Q479	23	R473	23	R900	23	W566	22
C455	22	CR631	22	Q521	22	R474	23	R901	23	W627	22
C460	22	CR650	22	Q665	23	R475	23	R903	23	W662	23
C461	22	CR651	22	Q721	22	R476	23	R923	22	W664	22
C483	22	CR683	23	Q779	23	R477	23	R924	22	W762	23
C485	23	CR684	23	Q836	22	R478	23	R930	22	W860	23
C487	23	CR685	23	Q870	23	R483	22	R934	22	W862	23
C494	23	CR723	22	Q879	23	R505	22	R935	22	W865	23
C525	22	CR724	22	R117	22	R516	22	R936	22	W868	23
C528	22	CR730	22	R128	22	R518	22	R975	23		
C550	22	CR750	22	R129	22	R565	23	RT717	22		
C553	22	CR751	22	R137	22	R566	23	RT805	22		
C575	23	CR765	23	R144	22	R575	23	T117	22		
C584	23	CR766	23	R145	22	R576	23	T335	22		
C585	23	CR796	23	R146	22	R578	23	T415	22		
C594	23	CR823	22	R164	23	R624	22	T620	22		
C595	23	CR824	22	R165	23	R627	22	T639	22		
C628	22	CR845	22	R166	23	R640	22	U155	22		
C650	22	CR846	22	R167	22	R675	23	U170	22		
C664	23	CR865	23	R185	23	R676	23	U170	23		
C675	23	CR866	23	R186	23	R684	23	U180	23		
C683	23	CR896	23	R187	23	R686	23	U189	23		
C694	23	CR930	22	R195	23	R688	23	U189	23		
C706	22	E609	22	R217	22	R713	22	U233	22		
C728	22	E616	22	R223	22	R723	22	U265	22		
C750	22	F269	22	R226	22	R724	22	U270	23		
C756	22	F961	23	R227	22	R727	22	U270	23		
C764	23	J102	22	R228	22	R728	22	U395	23		
C816	22	J102	23	R238	22	R758	23	U395	23		
C823	22	J102	23	R244	22	R760	23	U470	23		
C829	22	J102	23	R245	22	R765	23	U470	23		
C835	22	J102	23	R265	23	R769	23	U570	23		
C856	22	J102	23	R275	23	R773	23	U570	23		
C873	23	J102	23	R276	23	R774	23	U579	23		
C890	23	J166	23	R277	23	R775	23	U679	23		
C900	23	J166	23	R278	23	R776	23	U770	23		
C901	23	J166	23	R285	23	R777	23	U770	23		
C929	22	J166	23	R293	23	R794	23	U829	22		
C944	22	J166	23	R295	23	R795	23	U829	22		



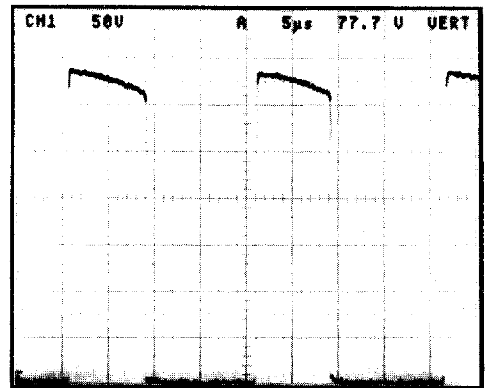
WARNING

PORTIONS OF THE 2430 POWER SUPPLY ARE AT THE AC LINE POTENTIAL-USE AN ISOLATION TRANSFORMER.

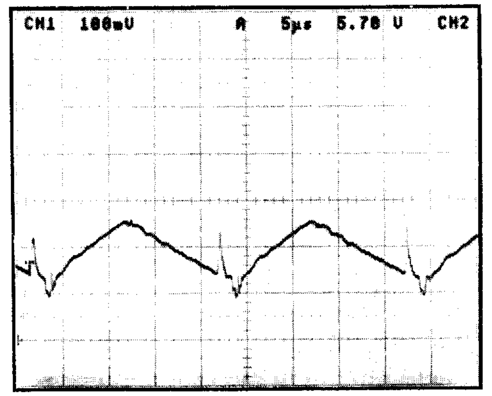
WAVEFORMS FOR DIAGRAM 22

171


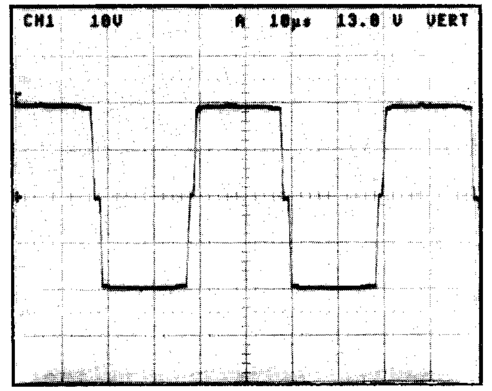
NORMAL AC LINE OPERATION

172


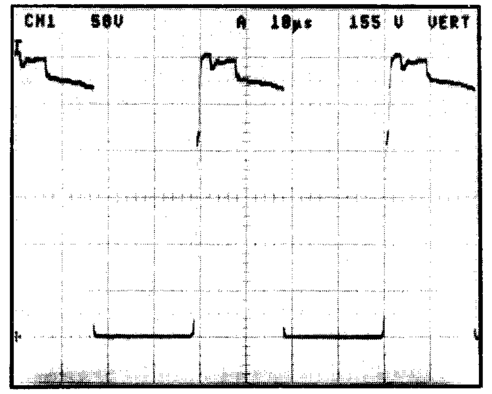
NORMAL AC LINE OPERATION

173


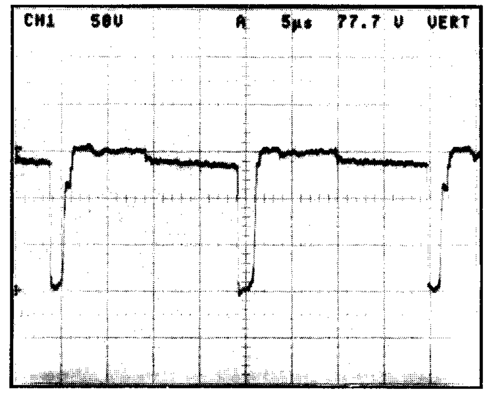
NORMAL AC LINE OPERATION

174


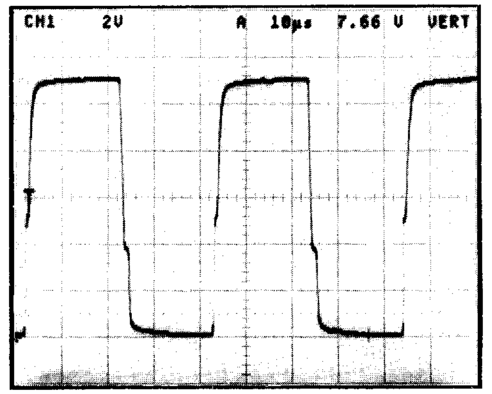
NORMAL AC LINE OPERATION

175


NORMAL AC LINE OPERATION

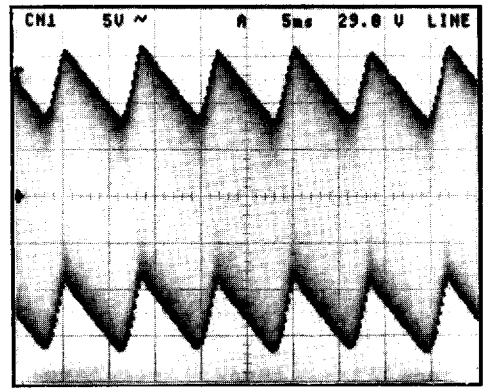
176


NORMAL AC LINE OPERATION

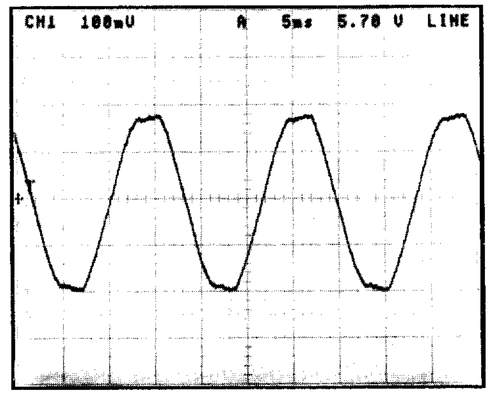
177


NORMAL AC LINE OPERATION

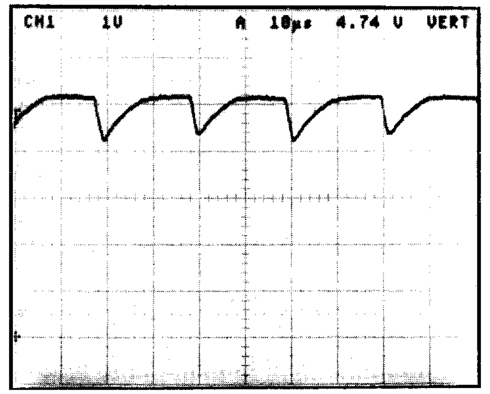
TEST SCOPE IN ENVELOPE

178


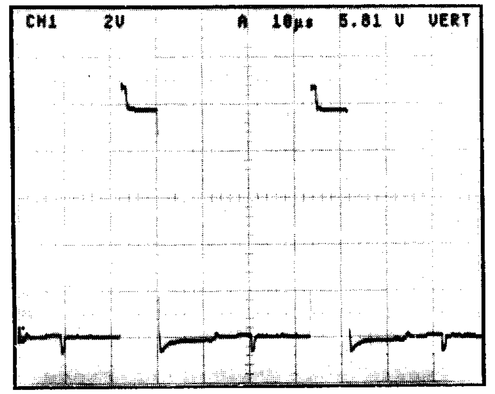
NORMAL AC LINE OPERATION

179


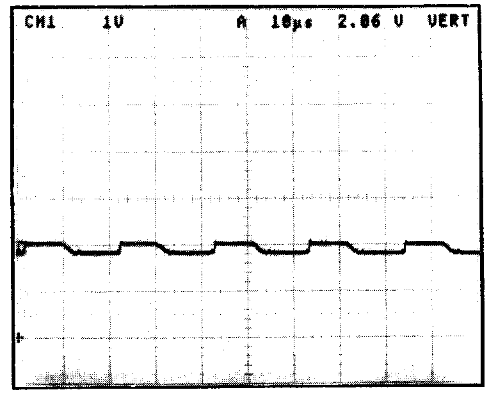
NORMAL AC LINE OPERATION

180


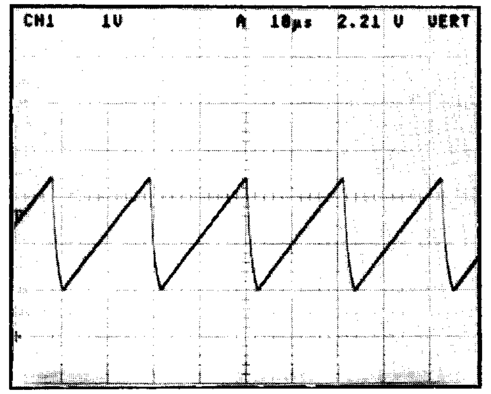
NORMAL AC LINE OPERATION

181


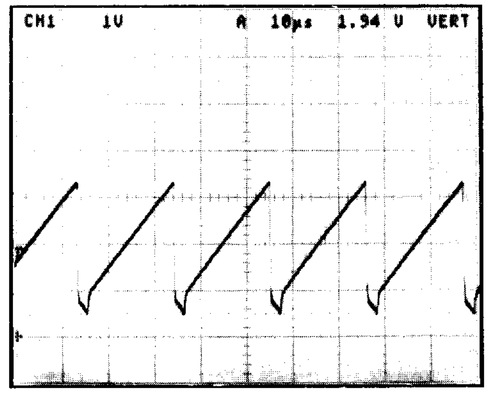
NORMAL AC LINE OPERATION

182


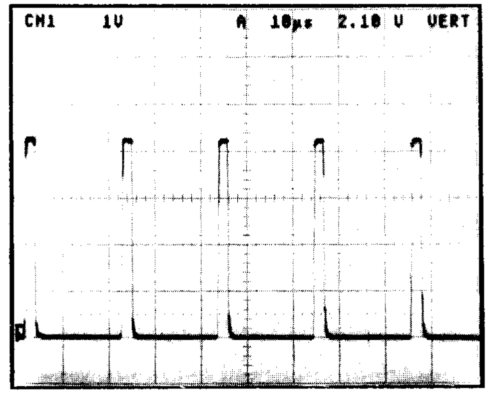
NORMAL AC LINE OPERATION

183


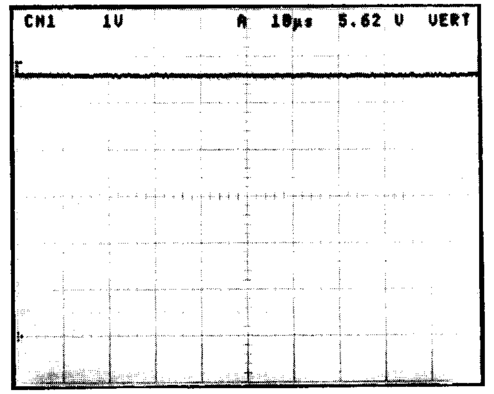
EITHER AC POWER OR CONTROL CIRCUIT POWER

184


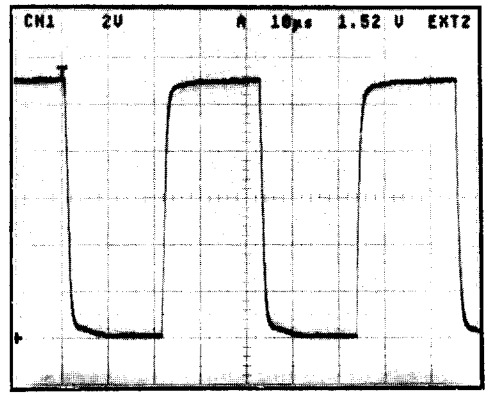
EITHER AC POWER OR CONTROL CIRCUIT POWER

185


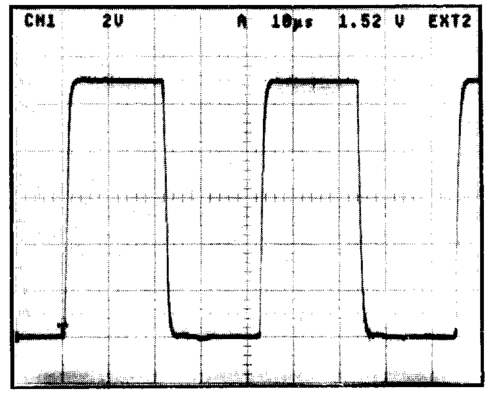
EITHER AC POWER OR CONTROL CIRCUIT POWER

186


CONTROL CIRCUIT POWER ONLY

187


CONTROL CIRCUIT POWER ONLY

188


CONTROL CIRCUIT POWER ONLY

MORE

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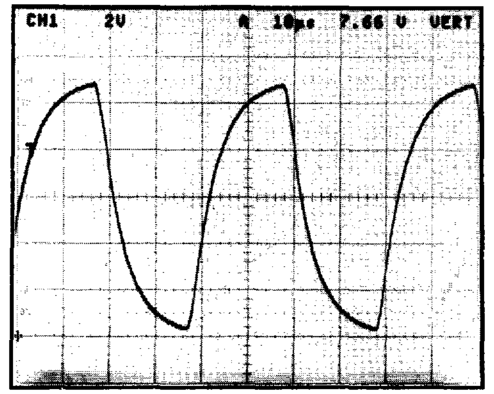
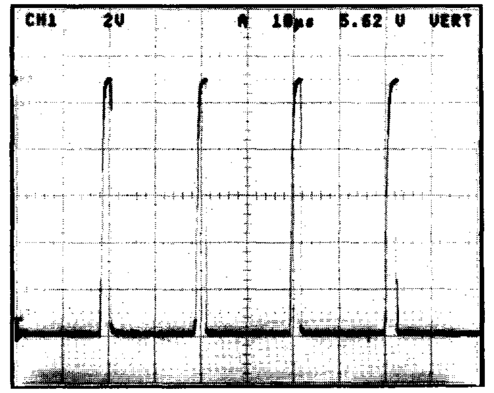
WAVEFORMS FOR DIAGRAM 22 (cont)

189



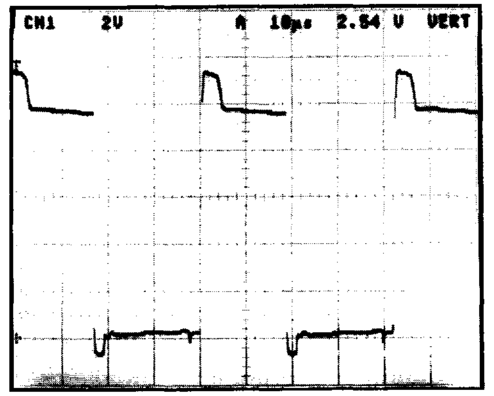
EITHER AC LINE OR
CONTROL CIRCUIT POWER

190



EITHER AC POWER OR
CONTROL CIRCUIT POWER

191



CONTROL CIRCUIT POWER ONLY

4917-92

LOW VOLTAGE POWER SUPPLY DIAGRAM 22

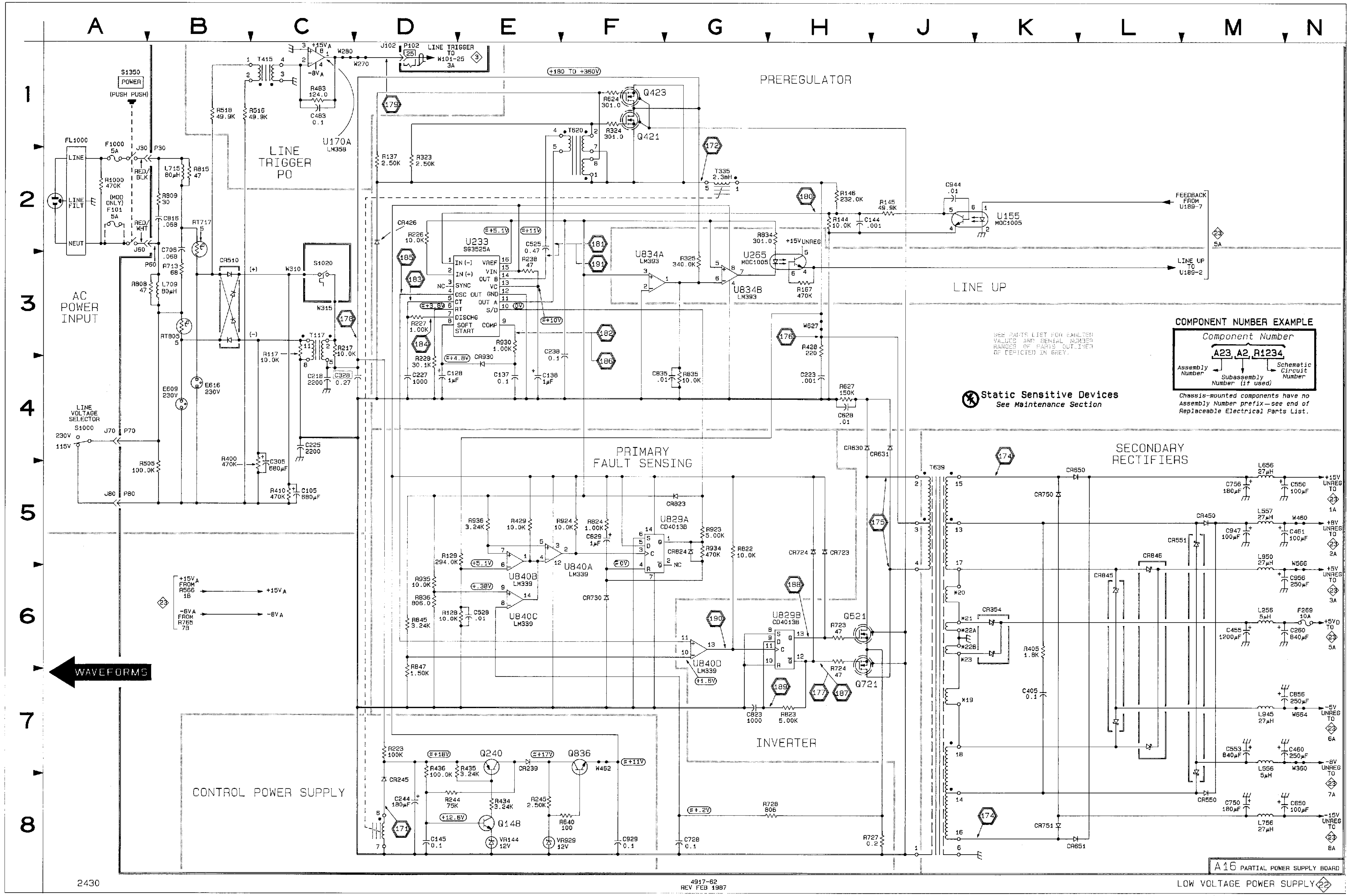
ASSEMBLY A16

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C105	5C	4B	CR551	5L	2F	R128	6D	6E	R845	6D	6F
C128	4D	6E	CR630	4H	2D	R129	5D	2D	R847	6D	6F
C137	4E	6E	CR631	4J	2D	R137	2D	5D	R923	5G	5E
C138	4E	6E	CR650	5K	3G	R144	2H	6D	R924	5F	6E
C144	2H	6D	CR651	8K	3G	R145	2J	6F	R930	3E	6E
C145	8D	3E	CR723	5H	5F	R146	2H	3D	R934	5G	5E
C218	4C	2C	CR724	5H	5F	R167	3H	6G	R935	6D	6F
C223	4H	2D	CR730	6F	5E	R217	3C	2B	R936	5E	6E
C225	4C	2C	CR750	5K	3G	R223	7D	4E			
C227	4D	6D	CR751	8K	3G	R226	2D	6D	RT717	2B	5C
C238	3E	6E	CR823	5G	5E	R227	3D	6D	RT805	3B	5B
C244	8D	4E	CR824	5G	5F	R228	4D	6D			
C260	6N	1H	CR845	6L	3F	R238	3E	6E	T117	3C	1B
C305	5C	3A	CR846	5L	3F	R244	8D	3E	T335	2G	3D
C328	4C	4D	CR930	4E	6E	R245	8E	4F	T415	1C	1A
C405	7K	1E				R323	2D	5D	T620	1F	5D
C455	6M	1G	E609	4B	5B	R324	1F	5D	T639	5J	2E
C460	7N	2H	E616	4B	5C	R325	3G	5E			
C461	5N	3H				R400	4B	4A	U155	2K	6G
C483	1C	2L	F269	6N	1J	R405	6K	1E	U170A	1C	2M
C525	2E	5D				R410	5C	4C	U233	2E	6D
C528	6E	6E	J102	1D	1K	R428	3H	2D	U265	3G	6G
C550	5N	4H				R429	5E	6E	U829A	5G	5F
C553	7M	2G	L256	6M	1H	R434	8E	3E	U829B	6H	5F
C628	4H	1D	L556	7M	2G	R435	7E	3E	U834A	3F	5F
C650	8N	5H	L557	5M	3G	R436	7D	3E	U834B	3G	5F
C706	2B	5C	L656	4M	4G	R483	1C	2L	U840A	6F	6F
C728	8G	6F	L709	3B	5B	R505	5B	5B	U840B	6E	6F
C750	8M	4G	L715	2B	5C	R516	1C	2A	U840C	6E	6F
C756	5M	3G	L756	8M	5G	R518	1B	2A	U840D	6G	6F
C816	2B	6A	L945	7M	4F	R624	1F	4D			
C823	7G	5F	L950	5M	3F	R627	4H	1D	VR144	8E	3E
C829	5F	5E				R640	8F	4F	VR929	8F	4F
C835	4F	4F	P30	2B	6A	R713	3B	5B			
C856	7N	4H	P60	3B	6A	R723	6H	3E	W270	1D	1K
C929	8F	5F	P70	4A	4A	R724	6H	2E	W280	1C	1L
C944	2J	6F	P80	5A	4A	R727	8J	2D	W310	3C	3C
C947	5M	2G				R728	8H	6F	W315	3C	3C
C956	6N	3H	Q148	8E	3E	R808	3A	5B	W360	7N	2H
			Q240	7E	3E	R809	2B	6A	W460	5N	3H
CR239	7E	4E	Q421	1F	5C	R815	2B	5C	W462	7F	4F
CR245	8D	4E	Q423	1F	4C	R822	5G	5F	W566	5N	4H
CR354	6K	1F	Q521	6H	3C	R823	7H	5F	W627	3H	3D
CR426	2D	4D	Q721	7H	2C	R824	5F	5E	W664	7N	4H
CR450	5M	2G	Q836	7F	3F	R834	2G	5F			
CR510	3B	3B				R835	4G	4F			
CR550	8M	2G	R117	3C	1B	R836	6D	6F			

Partial A16 also shown on diagram 23.

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
F1000	1A	CHASSIS	J30	1A	CHASSIS	P102	1D	CHASSIS	S1000	4A	CHASSIS
			J60	2A	CHASSIS				S1020	3C	CHASSIS
FL1000	1A	CHASSIS	J70	4A	CHASSIS	R1000	2A	CHASSIS	S1350	1A	CHASSIS
			J80	5A	CHASSIS						



LV POWER SUPPLY

22

LOW VOLTAGE REGULATORS DIAGRAM 23

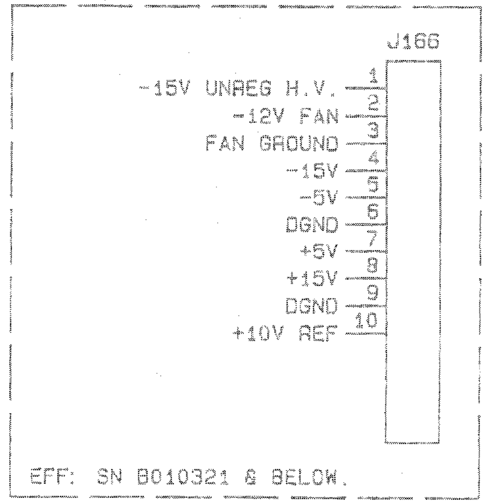
ASSEMBLY A16

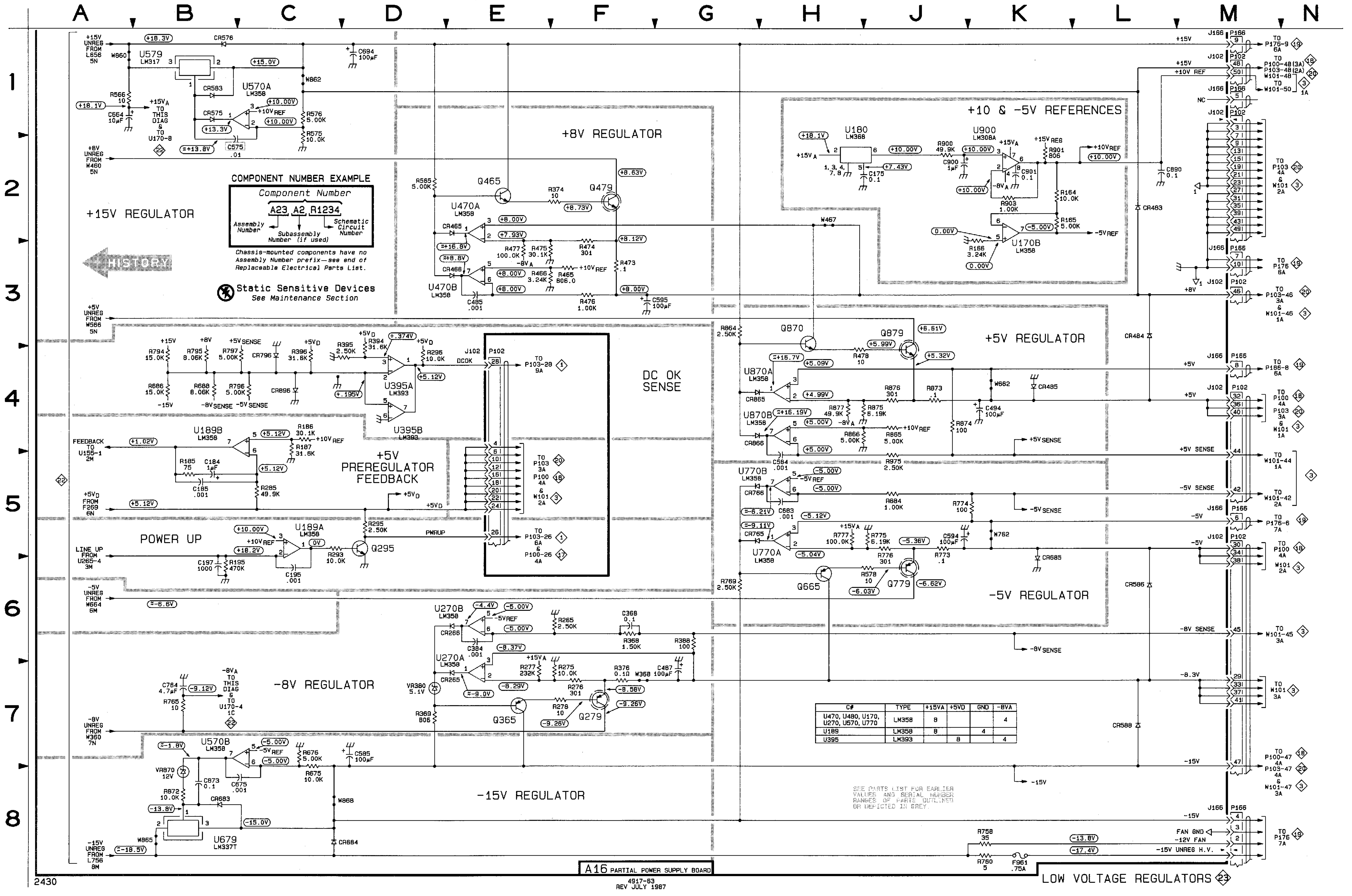
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C175	2J	3L	CR865	4G	3L	R368	6F	2L	R873	4J	4H
C184	5B	5L	CR866	4G	4L	R369	7D	2K	R874	4J	4L
C185	5B	6L	CR896	4C	3L	R374	2F	2K	R875	4J	4K
C195	6C	5K				R376	7F	3H	R876	4J	4K
C197	6B	6G	F961	8K	6K	R388	6G	3L	R877	4H	4K
C368	6F	3L				R394	3D	4L	R900	2J	3M
C384	6E	2L	J102	1M	1K	R395	3D	4L	R901	2K	2M
C485	3E	3L	J102	3M	1K	R396	4C	4L	R903	2K	3M
C487	7G	2J	J102	4E	1K	R465	3F	3L	R975	5J	4L
C494	4K	3H	J102	4M	1K	R466	3E	3L			
C575	2B	5K	J102	5M	1K	R473	3F	3H	U170B	2K	2M
C584	5H	4L	J166	1M	6J	R474	3F	3K	U180	1H	4M
C585	7D	5H	J166	3M	6J	R475	3E	3K	U189A	5C	6K
C594	5J	3J	J166	4M	6J	R476	3F	3L	U189B	4B	6K
C595	3G	2H	J166	5M	6J	R477	3E	3K	U270A	6E	2K
C664	1A	5L	J166	8M	6J	R478	4H	3K	U270B	6E	2K
C675	8C	5L				R565	2D	3L	U395A	4D	4M
C683	5H	4L	Q279	7F	2J	R566	1A	5K	U395B	4D	4M
C694	1D	5J	Q295	5D	5M	R575	1C	5L	U470A	2E	3K
C764	7B	2L	Q365	7E	2K	R576	1C	4L	U470B	3D	3K
C873	8B	6K	Q465	2E	3K	R578	6J	4K	U570A	1C	5K
C890	2L	2L	Q479	2F	3J	R675	8C	5L	U570B	7B	5K
C900	2J	3M	Q665	6H	4K	R676	7C	5L	U579	1B	5J
C901	2K	2M	Q779	6J	4J	R684	5J	4L	U679	8B	6J
			Q870	3H	3K	R686	4B	3L	U770A	5H	4K
CR265	7E	2L	Q879	3J	3J	R688	4B	2L	U770B	5G	4K
CR266	6E	2L				R758	8K	5G	U870A	4H	3K
CR465	2E	3K	R164	2K	3L	R760	8K	6G	U870B	4G	3K
CR466	3E	2K	R165	2K	3L	R765	7B	2K	U900	1K	3M
CR483	2L	1K	R166	3K	3L	R769	6G	4K			
CR484	3L	1K	R185	5B	5L	R773	5J	5H	VR380	7D	2L
CR485	4K	2J	R186	4C	5L	R774	5J	4L	VR870	8B	5K
CR575	1B	5K	R187	4C	5L	R775	5J	4K			
CR576	1B	5H	R195	6B	6G	R776	5J	4K	W368	7F	3H
CR583	1B	5K	R265	6F	2L	R777	5H	4K	W467	2H	3H
CR586	6L	1J	R275	7F	2K	R794	4B	3L	W662	4K	4H
CR588	7L	2K	R276	7F	2K	R795	4B	3L	W762	5K	5H
CR683	8B	6K	R277	7E	2K	R796	4B	4L	W860	1A	6H
CR684	8D	6H	R278	7F	2K	R797	4B	4L	W862	1C	6H
CR685	6K	1H	R285	5C	5L	R864	3G	3K	W865	8B	6H
CR765	5G	4K	R293	5C	5L	R865	4J	4L	W868	8D	6H
CR766	5G	4K	R295	5D	5L	R866	4H	4L			
CR796	4C	4L	R296	4D	4L	R872	8B	6K			

Partial A16 also shown on diagram 22.

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P102	1M	CHASSIS	P102	4M	CHASSIS	P166	3M	CHASSIS	P166	8M	CHASSIS
P102	3M	CHASSIS	P102	5M	CHASSIS	P166	4M	CHASSIS			
P102	4E	CHASSIS	P166	1M	CHASSIS	P166	5M	CHASSIS			





LV REGULATORS

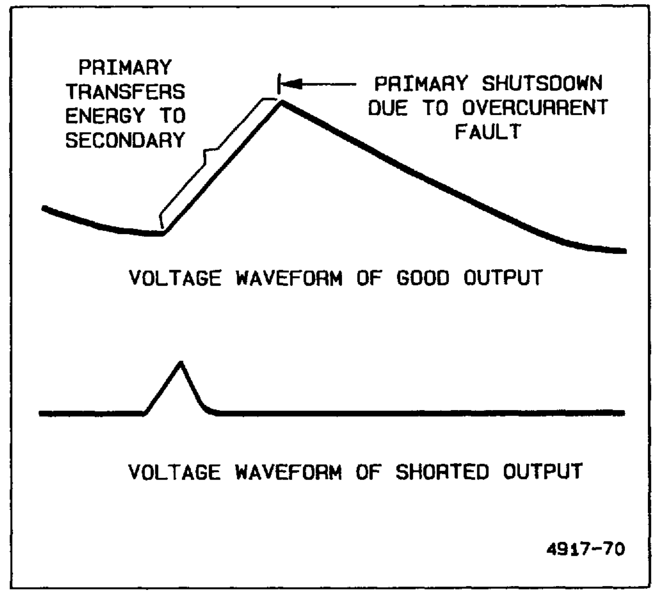
23

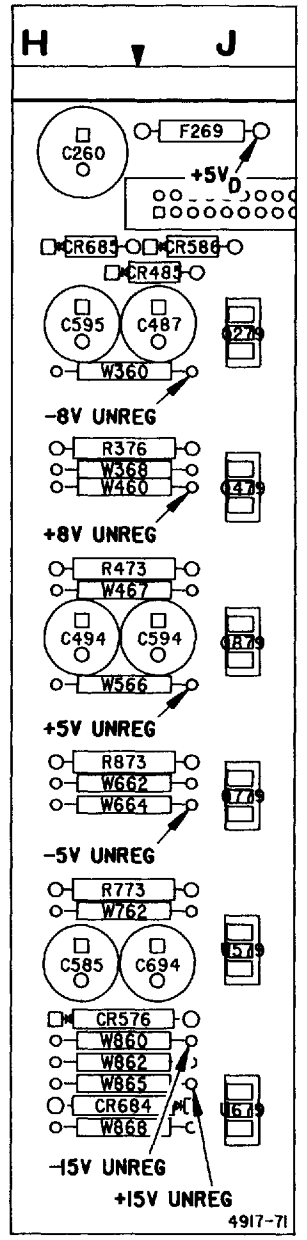
POWER SUPPLY OVERCURRENT FAULT

IN THE EVENT OF A SHORTED LOAD ON AN UNREGULATED VOLTAGE SUPPLY, THE POWER SUPPLY WILL GO INTO THE "CHIRP" MODE. IT CONTINUALLY STARTS UP AND SHUTS DOWN IN A REPEATED MANNER AS THE OVER-CURRENT SENSE CIRCUIT DETECTS THE EXCESSIVE SECONDARY LOADING. THE VOLTAGE WAVEFORM PRESENT ON THE UNREGULATED VOLTAGE LINES GIVES AN INDICATION OF WHETHER THE SECONDARY IS EXCESSIVELY LOADED. CHECK THE WAVEFORMS AT THE ZERO OHM RESISTORS INDICATED IN THE ACCOMPANYING COMPONENT LOCATION FIGURE FOR AN INDICATION OF EXCESSIVE LOADING. A SHORTED SECONDARY CIRCUIT IS IDENTIFIED BY A MUCH SMALLER VOLTAGE WAVEFORM THAN SEEN ON A GOOD SECONDARY (SEE ACCOMPANYING WAVEFORM ILLUSTRATION).

NOTE

A SHORT ON THE +5 VD SUPPLY WILL BLOW FUSE F269.





WARNING

TURN OFF ALL POWER BEFORE ATTEMPTING TO SOLDER OR REPLACE COMPONENTS OR TO MAKE RESISTANCE MEASUREMENTS.

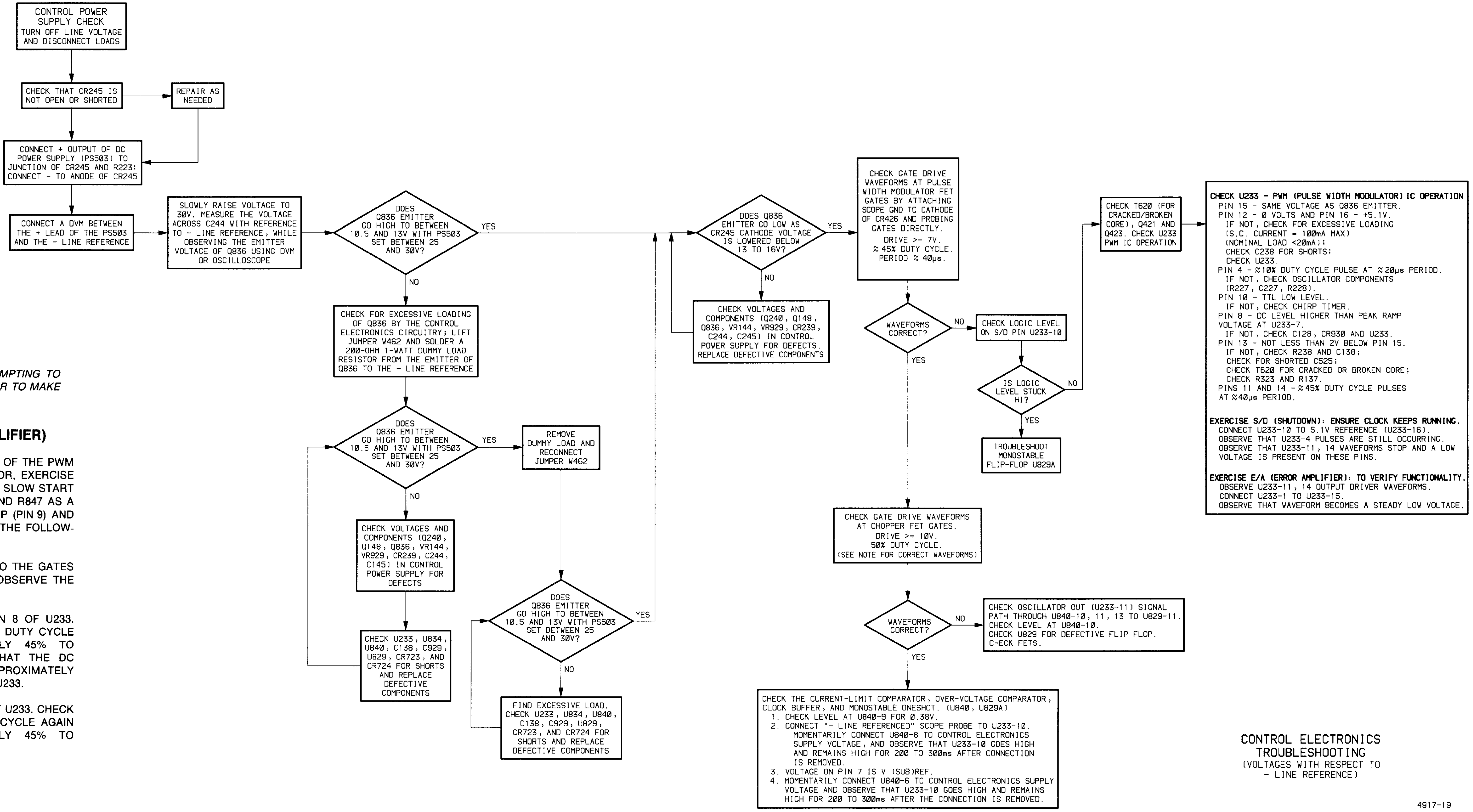
EXERCISE E/A (ERROR AMPLIFIER)

TO VERIFY THE FUNCTIONAL OPERATION OF THE PWM (PULSE-WIDTH MODULATOR) COMPARATOR, EXERCISE THE ERROR AMPLIFIER OUTPUT AND THE SLOW START INPUT. USE THE NODE BETWEEN R845 AND R847 AS A SOURCE OF +1.6 V TO DRIVE THE COMP (PIN 9) AND SOFT START (PIN 8) INPUTS OF U233 IN THE FOLLOWING MANNER:

1. MONITOR THE DRIVE WAVEFORMS TO THE GATES OF PWM FETS Q424 AND Q421 TO OBSERVE THE CHANGES THAT OCCUR.

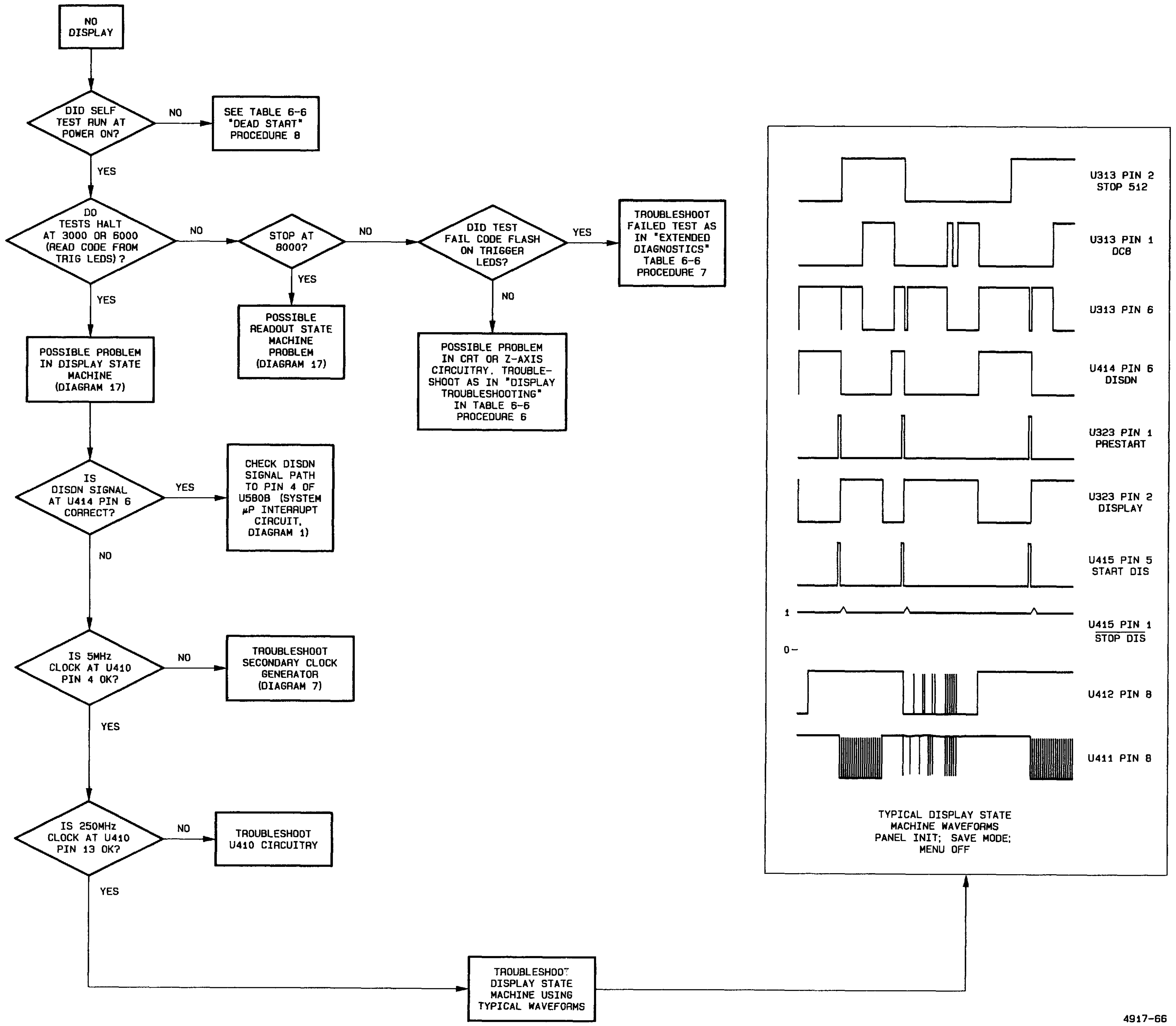
2. CONNECT THE +1.6 V LEVEL TO PIN 8 OF U233. CHECK THAT THE DRIVE WAVEFORM DUTY CYCLE DECREASES FROM APPROXIMATELY 45% TO APPROXIMATELY 15%. MEASURE THAT THE DC VOLTAGE ON PIN 9 OF U233 IS APPROXIMATELY 0.7 V MORE POSITIVE THAN PIN 8 OF U233.

3. MOVE THE +1.6 V LEVEL TO PIN 9 OF U233. CHECK THAT THE DRIVE WAVEFORM DUTY CYCLE AGAIN DECREASES FROM APPROXIMATELY 45% TO APPROXIMATELY 15%.

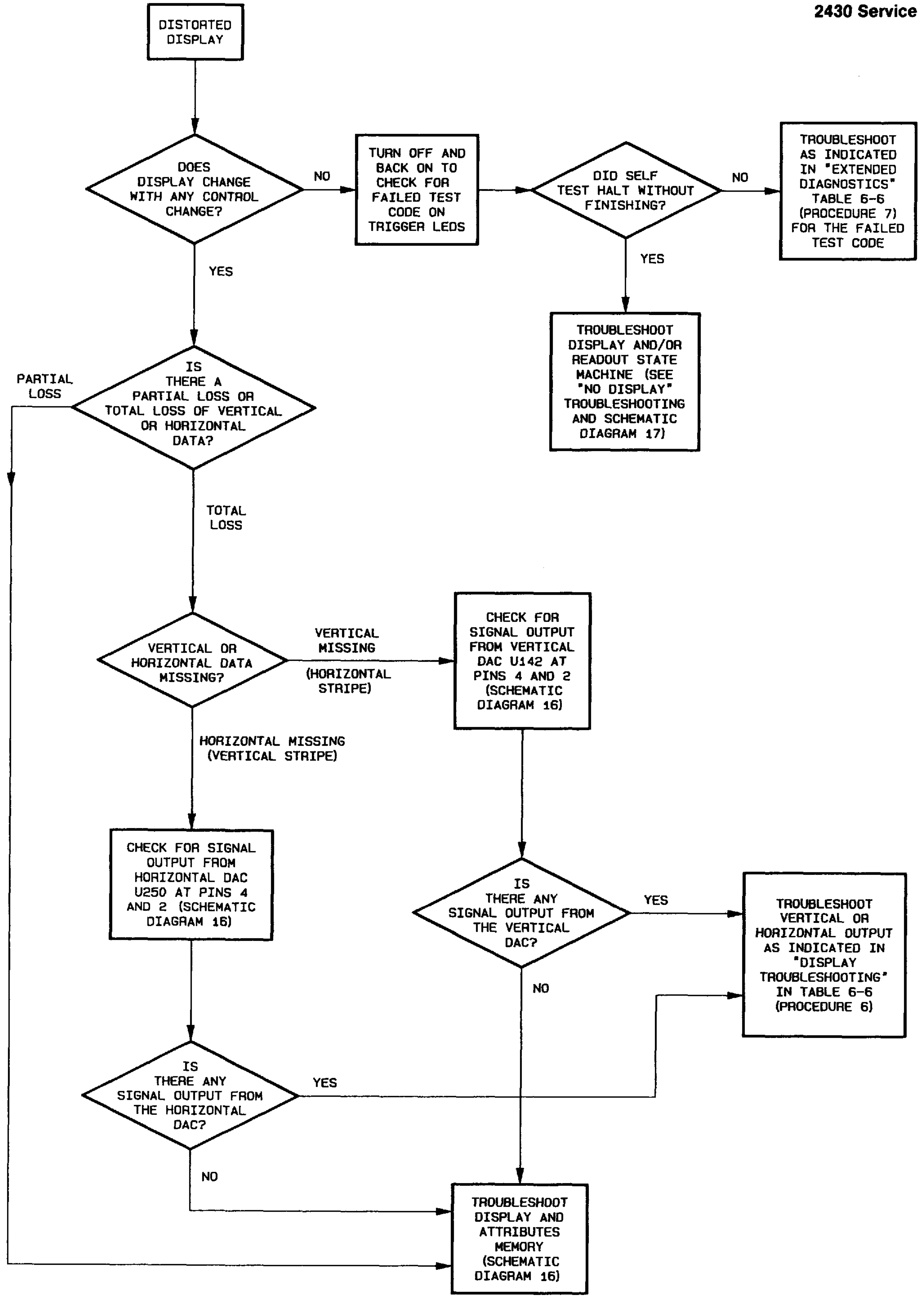


CONTROL ELECTRONICS TROUBLESHOOTING
(VOLTAGES WITH RESPECT TO − LINE REFERENCE)

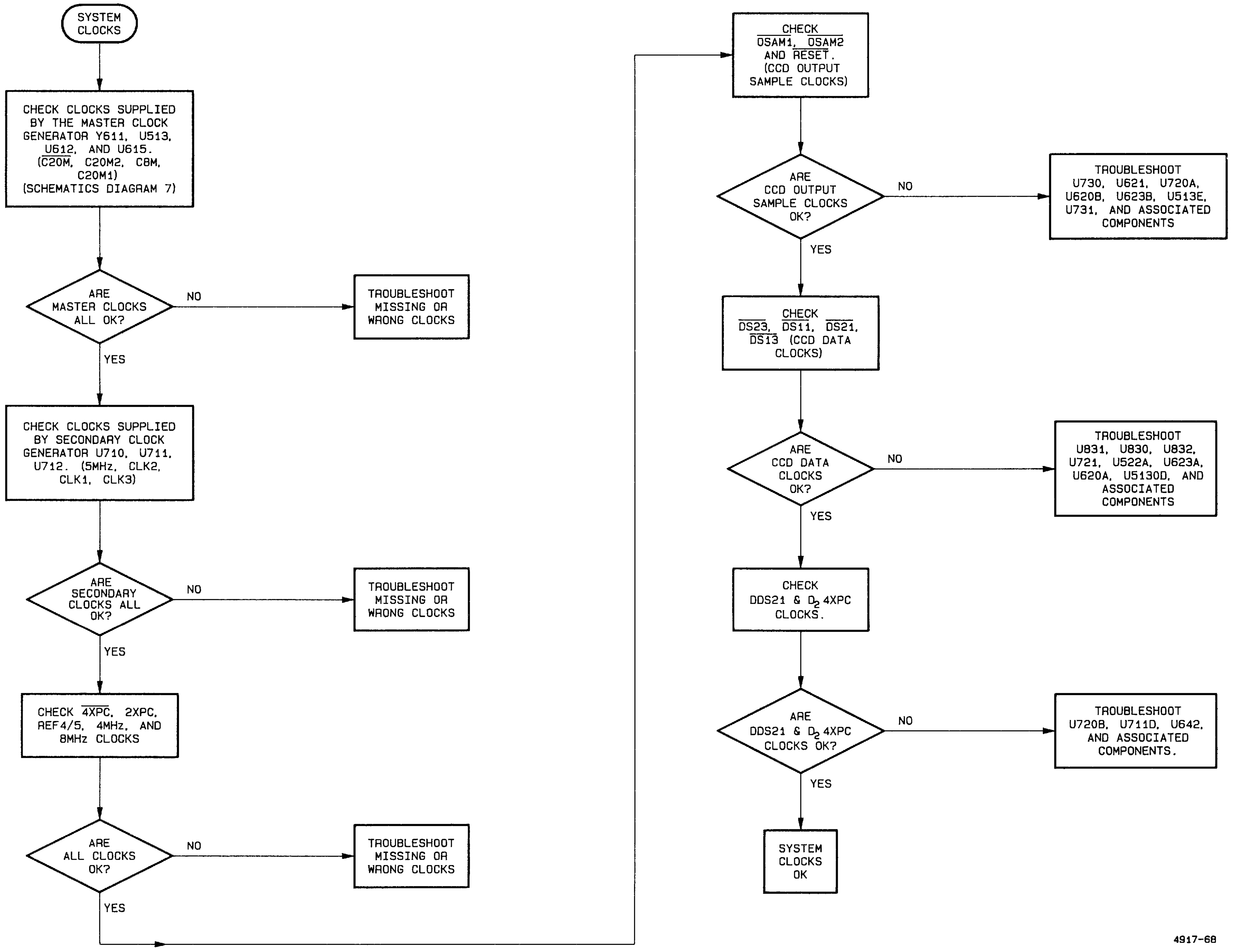
4917-19



4917-66



4917-65



SYSTEM CLOCK TROUBLESHOOTING

REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

1 2 3 4 5   Name & Description

Assembly and/or Component
Attaching parts for Assembly and/or Component
**** END ATTACHING PARTS ****
  Detail Part of Assembly and/or Component
  Attaching parts for Detail Part
  **** END ATTACHING PARTS ****
    Parts of Detail Part
    Attaching parts for Parts of Detail Part
    **** END ATTACHING PARTS ****

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation.

Attaching parts must be purchased separately, unless otherwise specified.

ABBREVIATIONS

	INCH	ELCTRN	ELECTRON	IN	INCH	SE	SINGLE END
#	NUMBER SIZE	ELEC	ELECTRICAL	INCAND	INCANDESCENT	SECT	SECTION
ACTR	ACTUATOR	ELCTLT	ELECTROLYTIC	INSUL	INSULATOR	SEMICOND	SEMICONDUCTOR
ADPTR	ADAPTER	ELEM	ELEMENT	INTL	INTERNAL	SHLD	SHIELD
ALIGN	ALIGNMENT	EPL	ELECTRICAL PARTS LIST	LPHLDR	LAMPHOLDER	SHLDR	SHOULDERED
AL	ALUMINUM	EQPT	EQUIPMENT	MACH	MACHINE	SKT	SOCKET
ASSEM	ASSEMBLED	EXT	EXTERNAL	MECH	MECHANICAL	SL	SLIDE
ASSY	ASSEMBLY	FIL	FILLISTER HEAD	MTG	MOUNTING	SLFLKG	SELF-LOCKING
ATTEN	ATTENUATOR	FLEX	FLEXIBLE	NIP	NIPPLE	SLVG	SLEEVING
AWG	AMERICAN WIRE GAGE	FLH	FLAT HEAD	NON WIRE	NOT WIRE WOUND	SPR	SPRING
BD	BOARD	FLTR	FILTER	OBD	ORDER BY DESCRIPTION	SQ	SQUARE
BRKT	BRACKET	FR	FRAME or FRONT	OD	OUTSIDE DIAMETER	SST	STAINLESS STEEL
BRS	BRASS	FSTNR	FASTENER	OVH	OVAL HEAD	STL	STEEL
BRZ	BRONZE	FT	FOOT	PH BRZ	PHOSPHOR BRONZE	SW	SWITCH
BSHG	BUSHING	FXD	FIXED	PL	PLAIN or PLATE	T	TUBE
CAB	CABINET	GSKT	GASKET	PLSTC	PLASTIC	TERM	TERMINAL
CAP	CAPACITOR	HDL	HANDLE	PN	PART NUMBER	THD	THREAD
CER	CERAMIC	HEX	HEXAGON	PNH	PAN HEAD	THK	THICK
CHAS	CHASSIS	HEX HD	HEXAGONAL HEAD	PWR	POWER	TNSN	TENSION
CKT	CIRCUIT	HEX SOC	HEXAGONAL SOCKET	RCPT	RECEPTACLE	TPG	TAPPING
COMP	COMPOSITION	HLCPS	HELICAL COMPRESSION	RES	RESISTOR	TRH	TRUSS HEAD
CONN	CONNECTOR	HLEXT	HELICAL EXTENSION	RGD	RIGID	V	VOLTAGE
COV	COVER	HV	HIGH VOLTAGE	RLF	RELIEF	VAR	VARIABLE
CPLG	COUPLING	IC	INTEGRATED CIRCUIT	RTNR	RETAINER	W	WITH
CRT	CATHODE RAY TUBE	ID	INSIDE DIAMETER	SCH	SOCKET HEAD	WSHR	WASHER
DEG	DEGREE	IDENT	IDENTIFICATION	SCOPE	OSCILLOSCOPE	XFMR	TRANSFORMER
DWR	DRAWER	IMPLR	IMPELLER	SCR	SCREW	XSTR	TRANSISTOR

CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
00779	AMP INC	2800 FULLING MILL PO BOX 3608	HARRISBURG PA 17105
01536	TEXTRON INC CAMCAR DIV SEMS PRODUCTS UNIT	1818 CHRISTINA ST	ROCKFORD IL 61108
04811	PRECISION COIL SPRING CO	10107 ROSE ST P O BOX 5450	EL MONTE CA 91734
05006	20TH CENTURY PLASTICS INC	3628 CRENSHAW BLVD PO BOX 30231	LOS ANGELES CA 90030
05820	EG AND G WAKEFIELD ENGINEERING	60 AUDUBON RD	WAKEFIELD MA 01880-1203
07416	NELSON NAME PLATE CO	3191 CASITAS	LOS ANGELES CA 90039-2410
09772	WEST COAST LOCKWASHER CO INC	16730 E JOHNSON DRIVE P O BOX 3588	CITY OF INDUSTRY CA 91744
09922	BURNDY CORP	RICHARDS AVE	NORWALK CT 06852
13511	AMPHENOL CADRE DIV BUNKER RAMO CORP		LOS GATOS CA
16428	COOPER BELDEN ELECTRONIC WIRE AND CA SUB OF COOPER INDUSTRIES INC	NW N ST	RICHMOND IN 47374
19613	MINNESOTA MINING AND MFG CO TEXTOOL PRODUCTS DEPT ELECTRONIC PRODUCT DIV	1410 E PIONEER DR	IRVING TX 75061-7847
22526	DU PONT E I DE NEMOURS AND CO INC DU PONT CONNECTOR SYSTEMS DIV MILITARY PRODUCTS GROUP	515 FISHING CREEK RD	NEW CUMBERLAND PA 17070-3007
22670	G M NAMEPLATE INC	2040 15TH AVE WEST	SEATTLE WA 98119-2728
31918	ITT SCHADOW INC	8081 WALLACE RD	EDEN PRAIRIE MN 55344-2224
56289	SPRAGUE ELECTRIC CO WORLD HEADQUARTERS	92 HAYDEN AVE	LEXINGTON MA 02173-7929
61545	AMP KEYBOARD TECHNOLOGIES INC SUB OF AMP INC	76 BLANCHARD RD PO BOX 543	BURLINGTON MA 01803-5125
70903	COOPER BELDEN ELECTRONICS WIRE AND C SUB OF COOPER INDUSTRIES INC	2000 S BATAVIA AVE	GENEVA IL 60134-3325
71400	BUSSMANN DIV OF COOPER INDUSTRIES INC	114 OLD STATE RD PO BOX 14460	ST LOUIS MO 63178
73743	FISCHER SPECIAL MFG CO	111 INDUSTRIAL RD	COLD SPRING KY 41076-9749
78189	ILLINOIS TOOL WORKS INC SHAKEPROOF DIV	ST CHARLES ROAD	ELGIN IL 60120
79338	COMPLEX TOOLING INC	4635 NAUTILUS COURT S	BOULDER CO 80301
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500 MS 53-111	BEAVERTON OR 97707-0001
83014	HARTWELL CORP	900 S RICHFIELD RD	PLACENTIA CA 92670-6732
83385	MICRODOT MFG INC GREER-CENTRAL DIV	3221 W BIG BEAVER RD	TROY MI 48098
83486	ELCO INDUSTRIES INC	1101 SAMUELSON RD	ROCKFORD IL 61101
86928	SEASTROM MFG CO INC	701 SONORA AVE	GLENDALE CA 91201-2431
91836	KINGS ELECTRONICS CO INC	40 MARBLEDALE ROAD	TUCKAHOE NY 10707-3420
93410	ESSEX GROUP ING CONTROLS DIV LEXINGTON PLANT	45-55 PLYMOUTH ST P O BOX 1007	LEXINGTON OH 44904
93907	TEXTRON INC CAMCAR DIV	600 18TH AVE	ROCKFORD IL 61108-5181
C013C	LEMOSA INC	2015 SECOND ST.	BERKELEY CA 94710
S3109	FELLER	ASA ADOLF AG STOTZWEID CH8810	HORGEN SWITZERLAND
S3629	SCHURTER AG H C/O PANEL COMPONENTS CORP	2015 SECOND STREET	BERKELEY CA 94170
TK0060	WRIGHT ENGINEERING PLASTICS INC	10350 OLD REDWOOD HWY	WINDSOR CA 95492-9208
TK0858	STAUFFER SUPPLY CO (DIST)	810 SE SHERMAN	PORTLAND OR 97214
TK0861	H SCHURTER AG DIST PANEL COMPONENTS	2015 SECOND STREET	BERKELEY CA 94170
TK1154	COMPLEX TOOLING INC	4635 NAUTILUS COURT SOUTH	BOULDER CO 80301
TK1169	DIEMAKERS INC	801 2ND ST PO BOX 278	MONROE CITY MO 63456-1441
TK1170	DTM INDUSTRIES	4725 NAUTILUS COURT SOUTH	BOULDER CO 80301
TK1285	GEROME MFG CO INC	PO BOX 737	NEWBURG OR 97132
TK1336	PARSONS MFG CORP	1055 OBRIEN	MENLO PARK CA 94025
TK1373	PATELEC-CEM (ITALY)	10156 TORINO	VAICENTALLO 62/45S ITALY

CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
TK1544	COMPUTER CONNECTIONS	2427 PRATT AVE	HAYWARD CA 94544
TK1634	SCHRAMM PLASTIC FABRICATIORS	7885 SW HUNZIKER	TIGARD OR 97223
TK2165	TRI-QUEST CORP	3000 LEWIS AND CLARK HWY	VANCOUVER WA 98661-2999

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
1-1	334-5584-00			1	MARKER,IDENT:MKD GPIB	80009	334-5584-00
-2	366-1833-01			1	KNOB:DOVE GRAY,0.25 ID X 0.392 OD X 0.466 H	80009	366-1833-01
	377-0512-01			1	INSERT,KNOB:0.172 ID X 0.28 OD X 0.64,NYL	80009	377-0512-01
-3	366-2036-00			3	PUSH BUTTON:GY,0.206 SQ,1.445 H	TK0060	93340-000
-4	334-5582-00			1	MARKER,IDENT:MKD CRT CONTROLS	80009	334-5582-00
-5	105-0608-00			5	ACTUATOR,SWITCH:MENU,ABS,SMOKE TAN	80009	105-0608-00
-6	200-2779-00			1	COVER,TOP:TRIM	TK1170	ORDER BY DESCR
-7	348-0740-00			2	FOOT,CABINET:BOTTOM FRONT,PLASTIC	TK1154	ORDER BY DESCR
					ATTACHING PARTS		
-8	211-0718-00			2	SCREW,MACHINE:6-32 X 0.312,FLH,100 DEG,STL	83486	ORDER BY DESCR
					END ATTACHING PARTS		
-9	101-0096-00			1	TRIM,DECORATIVE:FRONT	80009	101-0096-00
					ATTACHING PARTS		
-10	211-0718-00			6	SCREW,MACHINE:6-32 X 0.312,FLH,100 DEG,STL	83486	ORDER BY DESCR
					END ATTACHING PARTS		
-11	337-2926-03			1	SHLD,IMPLOSION:4.44 X 3.67 X 0.06,CLEAR	80009	337-2926-03
-12	334-5581-00	B010100	B011937	1	MARKER,IDENT:MKD SAFETY,STANDARD	80009	334-5581-00
	334-5581-03	B011938		1	MARKER,IDENT:MKD SAFETY,TEKTRONIX	07416	ORDER BY DESCR
-13	334-5458-00			1	MARKER,IDENT:MKD CONNECTOR IDENT,STD	80009	334-5458-00
	334-5457-00			1	MARKER,IDENT:MKD CONN IDENT,PROBE PWR (OPTION 11 ONLY)	80009	334-5457-00
-14	334-5696-00			1	MARKER,IDENT:MKD OPTION	80009	334-5696-00
-15	348-0729-00			2	FOOT,CABINET:W/CORD WRAP,REAR,BLACK PU	80009	348-0729-00
					ATTACHING PARTS		
-16	212-0154-00			4	SCREW,MACHINE:8-32 X 1.125,PNH,STL	83385	ORDER BY DESCR
					END ATTACHING PARTS		
-17	200-2961-00			1	COVER,REAR:POLYCARBONATE,SMOKE TAN	80009	200-2961-00
-18	334-5579-00			1	MARKER,IDENT:MKD TEKTRONIX 2430,HANDLE	80009	334-5579-00
-19	367-0303-04			1	HANDLE,CARRYING:12.86 L,GRIP & INDEX	80009	367-0303-04
					ATTACHING PARTS		
-20	212-0144-00			2	SCREW,TPG,TF:8-16 X 0.562,PLASTITE,SPCL HD	93907	225-38131-012
					END ATTACHING PARTS		
-21	437-0139-00			1	CABINET,SCOPE:	80009	437-0139-00
-22	211-0730-00			2	SCR,ASSEM WSHR:6-32 X 0.375,PNH,STL,T15	80009	211-0730-00

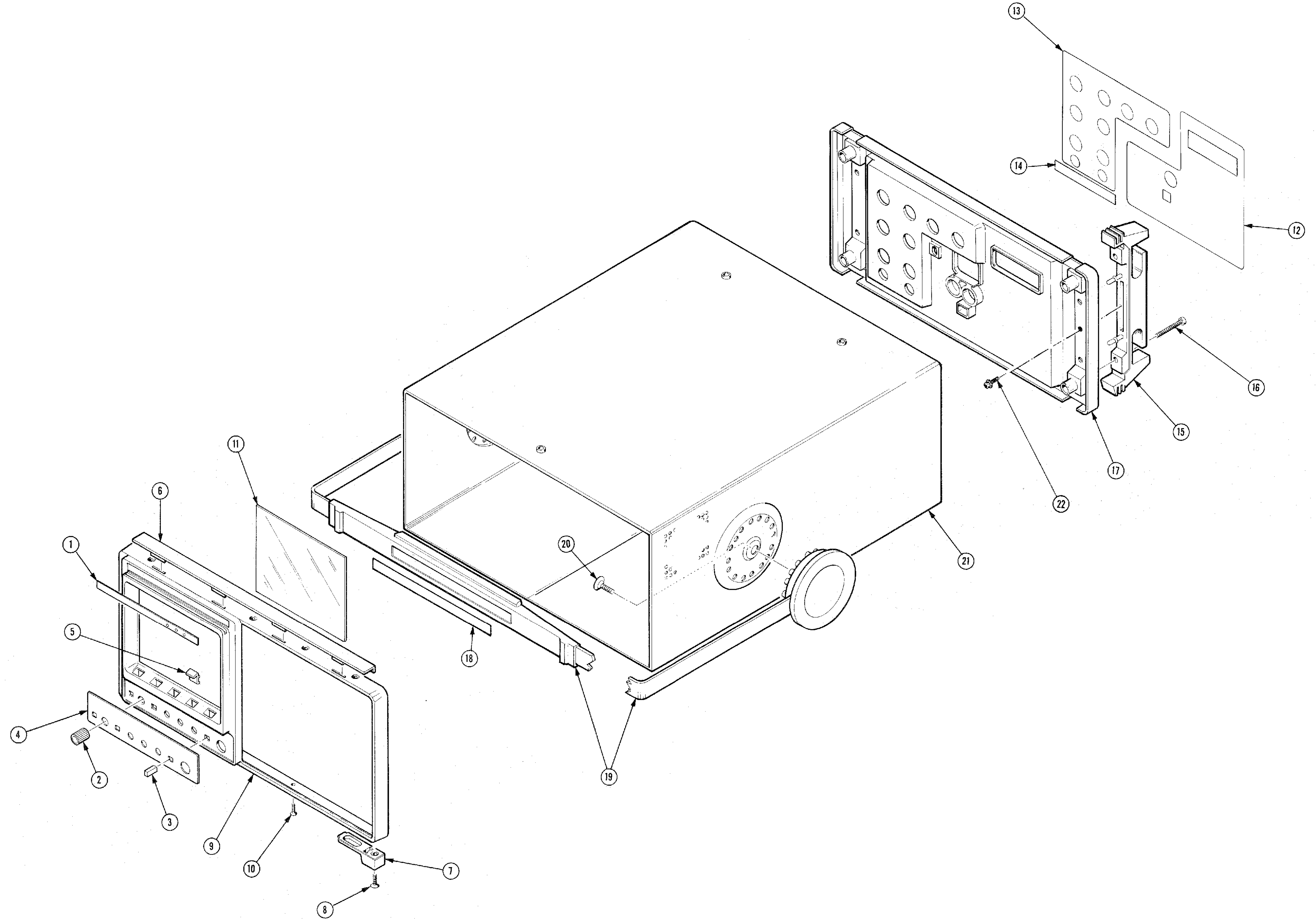


FIG. 1 CABINET

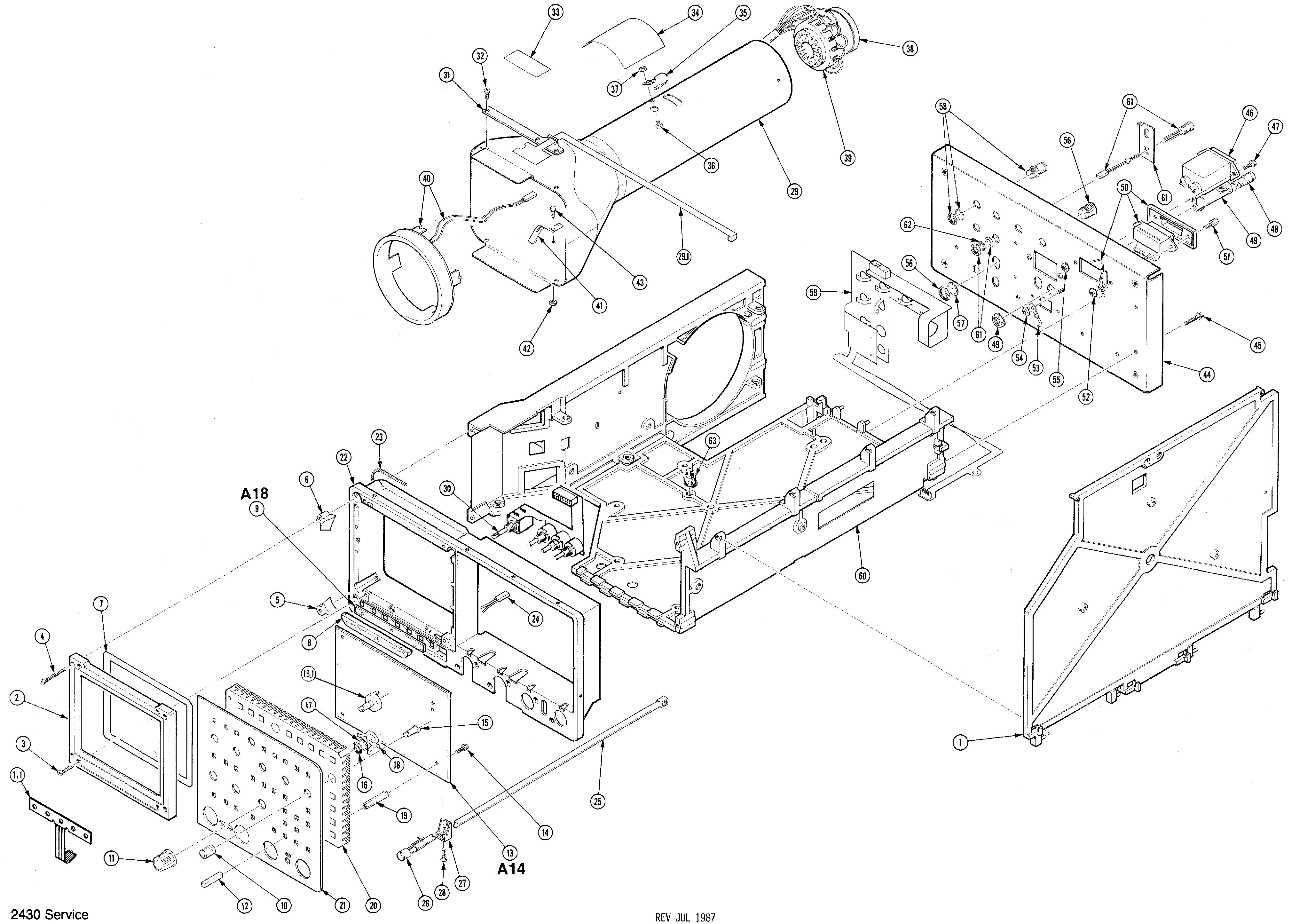


FIG. 2 CHASSIS, REAR

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
2-1	441-1563-00			1	CHASSIS,SCOPE:TOP	80009	441-1563-00
-1.1	260-2173-00			1	SW,PUSH BUTTON:MOMENTARY,5 BUTTON	61545	CP85-41313
-2	426-1864-01			1	FRAME,CRT:	TK1169	ORDER BY DESCR
					ATTACHING PARTS		
-3	213-0914-00			4	SCREW,TPG,TR:6-32 X 0.75,FLH,100 DEG,STL	83385	ORDER BY DESCR
-4	211-0713-00			4	SCREW,MACHINE:6-32 X 1.25,FLH,100 DEG,STL	83385	ORDER BY DESCR
					END ATTACHING PARTS		
-5	343-0992-00			2	RETAINER,CRT:CLEAR,PLASTIC	80009	343-0992-00
-6	343-0993-00			2	RETAINER,CRT:BLACK,PLASTIC	80009	343-0993-00
-7	348-0731-01			1	GASKET:CRT,POLYETHYLENE	80009	348-0731-01
-8	378-0204-00			1	REFLECTOR,LIGHT:INT SCALE ILLUMINATION	80009	378-0204-00
-9	----- -----			1	CIRCUIT BD ASSY:SCALE ILLUM (SEE A18 REPL)		
-10	366-1833-01			6	KNOB:DOVE GRAY,0.25 ID X 0.392 OD X 0.466 H	80009	366-1833-01
-11	366-0555-00			3	KNOB:	80009	366-0555-00
-12	366-2017-00			29	PUSH BUTTON:0.18 SQ X 0.644 H,IVORY GY	79338	ORDER BY DESCR
-13	----- -----			1	CIRCUIT BD ASSY:FRONT PANEL (SEE A14 REPL)		
					ATTACHING PARTS		
-14	211-0304-00			4	SCR,ASSEM WSHR:4-40 X 0.312,PNH,STL,T9 TORX	01536	ORDER BY DESCR
					END ATTACHING PARTS		
					FRONT PANEL BOARD ASSEMBLY INCLUDES:		
-15	377-0550-01			2	.INSERT,KNOB:0.178 ID X 0.37 OD X 0.64	80009	377-0550-01
-16	220-0495-00			3	.NUT,PLAIN,HEX:0.375-32 X 0.438 HEX,BRS	73743	ORDER BY DESCR
-17	210-0012-00			3	.WASHER,LOCK:0.384 ID,INTL,0.022 THK,STL	09772	ORDER BY DESCR
-18	210-0077-01			3	.WASHER,SPR TNSN:0.382 ID X 0.625 OD X 0.007	86928	5806-123-1
-18.1	377-0383-00			4	.INSERT,KNOB:0.178 ID 0.78 OD X 1.0,PLSTC	80009	377-0383-00
-19	129-0938-00			4	SPACER,POST:1.102 L,4-40 EA END,AL	80009	129-0938-00
-20	354-0465-00	B010100	B012084	1	RING,MOUNTING:6.065 X 4.16,BRASS	80009	354-0465-00
	354-0465-01	B012085		1	RING,MOUNTING:6.065 X 4.16,BRASS	80009	354-0465-01
-21	333-3094-00			1	PANEL,FRONT:	80009	333-3094-00
	333-3095-00			1	PANEL,FRONT: (OPTION 05 ONLY)	80009	333-3095-00
-22	386-4728-01			1	SUBPANEL,FRONT:	80009	386-4728-01
-23	348-0792-01			1	GASKET:ELECTRICAL SHIELD,34.0 L	80009	348-0792-01
-24	175-4593-00	B010100	B010709	1	CA ASSY,SP,ELEC:2,26 AWG,4.0 L,RIBBON	80009	175-4593-00
	175-4593-01	B010710		1	CA ASSY,SP,ELEC:2,22 AWG,3.5 L,RIBBON	80009	175-4593-01
-25	384-0837-00			1	EXTENSION SHAFT:13.470 L X 0.250 X 0.300	80009	384-0837-00
-26	366-1767-00			1	PUSH BUTTON:BLACK,YELLOW INDICATOR	31918	160597
-27	407-2904-01	B010100	B011079	1	BRACKET,EXT SFT:POLYCARBONATE	80009	407-2904-01
	407-2904-02	B011080		1	BRACKET,EXT SFT:POWER,POLYCARBONATE	80009	407-2904-02
					ATTACHING PARTS		
-28	211-0718-00			1	SCREW,MACHINE:6-32 X 0.312,FLH,100 DEG,STL	83486	ORDER BY DESCR
					END ATTACHING PARTS		
-29	337-2931-01			1	SHIELD,CRT:	TK1285	337-2931-01
-29.1	175-9270-00			1	FLEX CKT ASSY:GPIB,POLYMIDE	80009	175-9270-00
-30	175-9359-00			1	FLEX CKT ASSY:CRT CONTROLS,POLYMIDE	80009	175-9359-00
-31	386-0867-00			1	PLATE,MOUNTING:LED	80009	386-0867-00
					ATTACHING PARTS		
-32	211-0304-00			4	SCR,ASSEM WSHR:4-40 X 0.312,PNH,STL,T9 TORX	01536	ORDER BY DESCR
					END ATTACHING PARTS		
-33	334-1379-00			1	MARKER,IDENT:MKD HI VACUUM	07416	ORDER BY DESCR
-34	334-1951-00			1	MARKER,IDENT:MKD WARNING,CRT VOLTAGES	22670	ORDER BY DESCR
-35	195-6851-01			1	LEAD,ELECTRICAL:BRAIDED,1.65 L	80009	195-6851-01
					ATTACHING PARTS		
-36	211-0324-00			1	SCR,ASSEM WSHR:4-40 X 0.188,PNH,T9 TORX DR	01536	829-06780-024
-37	210-0586-00			1	NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	78189	211-041800-00
					END ATTACHING PARTS		
-38	200-0917-01			1	COVER,CRT SKT:2.052 OD X 0.291 H,PLASTIC	80009	200-0917-01
-39	175-9271-00			1	LEAD SET,ELEC:14,24 AWG,9.5 L	80009	175-9271-00
	136-0304-03			1	SKT,PL-IN ELEK:ELECTRON TUBE,14 CONTACT	80009	136-0304-03
-40	----- -----			1	COIL,TUBE DEFL:FXD,TRACE ROTATION (SEE L1000, CHASSIS PART, REPL)		
-41	214-0291-00			2	CONTACT,ELEC:CRT CONNECTOR,CU BE SIL PL	04811	ORDER BY DESCR
					ATTACHING PARTS		
-42	210-0586-00			2	NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	78189	211-041800-00
-43	211-0324-00			2	SCR,ASSEM WSHR:4-40 X 0.188,PNH,T9 TORX DR	01536	829-06780-024
					END ATTACHING PARTS		
-44	441-1562-00			1	CHASSIS,SCOPE:REAR	80009	441-1562-00
					ATTACHING PARTS		

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
2-45	213-0942-00			4	SCREW,TPG,TR:6-32 X 0.75,TYPE TT,PNH,STL	TK0858	ORDER BY DESCR
					END ATTACHING PARTS		
-46	----- -----			1	FILTER,RFI:6A,250V,50-400HZ (SEE FL1000, CHASSIS PARTS, REPL)		
					ATTACHING PARTS		
-47	211-0304-00			2	SCR,ASSEM WSHR:4-40 X 0.312,PNH,STL,T9 TORX	01536	ORDER BY DESCR
					END ATTACHING PARTS		
-48	200-2264-00			1	CAP,FUSEHOLDER:3AG FUSES	S3629	FEK 031 1666
-49	204-0832-00			1	BODY,FUSEHOLDER:3AG & 5 X 20MM FUSES	TK0861	031 1673
-50	175-9229-00			1	CA ASSY,SP,ELEC:24,28 AWG,7.0 L,RIBBON	80009	175-9229-00
					ATTACHING PARTS		
-51	129-1003-00			1	SPCR,POST:0.705 L,6-32 EXT/M3.5 X 6-6G INT	80009	129-1003-00
-52	210-0457-00			1	NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	78189	511-061800-00
					END ATTACHING PARTS		
-53	195-3990-00			1	LEAD,ELECTRICAL:18 AWG,4.5 L,5-4	80009	195-3990-00
					ATTACHING PARTS		
-54	210-0457-00			1	NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	78189	511-061800-00
					END ATTACHING PARTS		
-55	210-0457-00			1	NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	78189	511-061800-00
-56	131-1471-00			1	CONN,RCPT,ELEC:RA,3 EA MALE & FEMALE CONT	C0130	RA1306
-57	210-0021-00			1	WASHER,LOCK:0.476 ID,INTL,0.018 THK,STL	78189	1222-01
-58	131-0955-00			7	CONN,RCPT,ELEC:BNC,FEMALE	13511	31-279
-59	175-9357-00			1	FLEX CKT ASSY:REAR PANEL,POLYMIDE	80009	175-9357-00
-60	441-1574-00			1	CHASSIS,SCOPE:MAIN	80009	441-1574-00
-61	131-0771-00			2	CONN,RCPT,ELEC:2 MALE,2 FEM,PNL MT W/O HDW	91836	1904-2M58
	220-0551-00			2	NUT,PLAIN,HEX:9 MM X 1.00,BRS NP	73743	ORDER BY DESCR
-62	210-0012-00			2	WASHER,LOCK:0.384 ID,INTL,0.022 THK,STL (OPTION 11 ONLY)	09772	ORDER BY DESCR
-63	361-1276-00			18	SPACER,CKT BD:0.25 STANDOFF,POLYSULFONE,BLK	83014	HNST4-250-1

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
3-1	----- -----			1	CIRCUIT BD ASSY:TIME BASE (SEE A11 REPL)		
					ATTACHING PARTS		
-2	213-0942-00	B010100	B010447	3	SCREW,TPG,TR:6-32 X 0.75,TYPE TT,PNH,STL	TK0858	ORDER BY DESCR
	213-0927-00	B010448		3	SCREW,TPG,TR:6-32 X 0.875,TYPE TT,PNH,STL	TK0858	ORDER BY DESCR
	131-1428-00	B010448	B011145	1	CONTACT,ELEC:GROUNDING,CU BE CD PL	80009	131-1428-00
	210-1266-00	B010448	B011145	1	WASHER,FLAT:0.193 ID X 0.475 OD X 0.075,STL	86928	5702-79-75C
	210-0202-00	B010448	B011145	1	TERMINAL,LUG:0.146 ID,LOCKING,BRZ TIN PL	86928	A-373-158-2
					END ATTACHING PARTS		
	175-9353-00	B010100	B013283	1	CABLE ASSY,RF:4,50 OHM COAX,15.0 L	80009	175-9353-00
	175-9353-01	B013284		1	CABLE ASSY,RF:8,50 OHM COAX,15.0 L	TK1544	ORDER BY DESCR
	175-9356-00			1	CA ASSY,SP,ELEC:5,26 AWG,22.75 L,RIBBON	80009	175-9356-00
-3	----- -----			1	CIRCUIT BD ASSY:PROCESSOR (SEE A12 REPL)		
-4	136-0757-00	B010100	B012056	1	.SKT,PL-IN ELEK:MICROCIRCUIT,40 DIP .(STANDARD)	09922	DILB40P-108
	136-0757-00	B010100	B012303	1	.SKT,PL-IN ELEK:MICROCIRCUIT,40 DIP .(OPTION 05)	09922	DILB40P-108
-5	136-0755-00			5	.SKT,PL-IN ELEK:MICROCIRCUIT,28 DIP	09922	DILB28P-108
-6	136-0751-00	B010100	B010447	2	.SKT,PL-IN ELEK:MICROCKT,24 PIN	09922	DILB24P108
-7	136-0813-00			1	.SKT,PL-IN ELEK:CHIP CARRIER,68 CONTACTS	19613	268-5400-00-1102
-7.1	----- -----			1	.MICROCKT,DGTL:(SEE A12U470 REPL)		
-7.2	214-3637-00	B010100	B011334	1	.HEAT SINK,ELEC:CHIP CARRIER,ALUMINUM	05820	ORDER BY DESCR
	214-3637-01	B011335		1	.HT SK,MICROCKT:ALUMINUM,BLACK ANODIZE	80009	214-3637-01
-8	131-0993-00			4	.BUS,CONDUCTOR:SHUNT ASSEMBLY,BLACK	22526	65474-005
-9	----- -----			1	CHASSIS,SCOPE:TOP (SEE FIGURE 2)		
-10	----- -----			1	CHASSIS,SCOPE:MAIN (SEE FIGURE 2)		
-11	----- -----			1	CIRCUIT BD ASSY:SIDE (SEE A13 REPL)		
					ATTACHING PARTS		
-12	213-0942-00	B010100	B010447	1	SCREW,TPG,TR:6-32 X 0.75,TYPE TT,PNH,STL	TK0858	ORDER BY DESCR
	213-0927-00	B010448		1	SCREW,TPG,TR:6-32 X 0.875,TYPE TT,PNH,STL	TK0858	ORDER BY DESCR
					END ATTACHING PARTS		
	352-0171-00	B010258	B010299	1	.HLDR,TERM CONN:1 WIRE,BLACK	80009	352-0171-00
-13	----- -----			1	CIRCUIT BD ASSY:MAIN (SEE A10 REPL)		
					ATTACHING PARTS		
-14	213-0942-00	B010100	B010447	1	SCREW,TPG,TR:6-32 X 0.75,TYPE TT,PNH,STL	TK0858	ORDER BY DESCR
	213-0927-00	B010448		1	SCREW,TPG,TR:6-32 X 0.875,TYPE TT,PNH,STL	TK0858	ORDER BY DESCR
-15	210-0586-00			2	NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	78189	211-041800-00
					END ATTACHING PARTS		
					MAIN BOARD ASSEMBLY INCLUDES:		
-16	214-3637-00	B010100	B011334	2	.HEAT SINK,ELEC:CHIP CARRIER,ALUMINUM	05820	ORDER BY DESCR
	214-3637-01	B011335		2	.HT SK,MICROCKT:ALUMINUM,BLACK ANODIZE	80009	214-3637-01
-17	----- -----			2	.INTEGRATED CKT:TRIGGER LOGIC,M299 .(SEE A10U370,U470 REPL)		
-18	136-0813-00			2	.SKT,PL-IN ELEK:CHIP CARRIER,68 CONTACTS	19613	268-5400-00-1102
-19	----- -----			2	.MICROCKT,HYBRID:PEAK DETECTOR .(SEE A10U340,U440 REPL)		
-20	136-0764-00			2	.SKT,PL-IN ELEK:48 LINE CONT IMPD HYBRID	00779	ORDER BY DESCR
					ATTACHING PARTS		
-21	210-0586-00			8	.NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	78189	211-041800-00
					END ATTACHING PARTS		
-22	----- -----			2	.MICROCKT,HYBRID:CCD/DRIVER ASSSEMBLY .(SEE A10U350,U450 REPL)		
-23	136-0764-00			2	.SKT,PL-IN ELEK:48 LINE CONT IMPD HYBRID	00779	ORDER BY DESCR
					ATTACHING PARTS		
-24	210-0586-00			8	.NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	78189	211-041800-00
					END ATTACHING PARTS		
-25	----- -----			2	.MICROCKT,LINEAR:TRIGGER PREAMP .(SEE A10U100,U150 REPL)		
-26	136-0764-00			2	.SKT,PL-IN ELEK:48 LINE CONT IMPD HYBRID	00779	ORDER BY DESCR
					ATTACHING PARTS		
-27	210-0586-00			8	.NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	78189	211-041800-00
					END ATTACHING PARTS		
-28	337-3031-00			2	.SHIELD,ELEC:PRE-AMP	80009	337-3031-00
					ATTACHING PARTS		
-29	211-0324-00			4	.SCR,ASSEM WSHR:4-40 X 0.188,PNH,T9 TORX DR	01536	829-06780-024
					END ATTACHING PARTS		
-30	129-0985-00			4	.SPACER,POST:0.350 L,4-40 THRU,STL,0.25 HEX	80009	129-0985-00
-31	----- -----			2	.MICROCKT,HYBRID:(SEE A10U320,U420 REPL)		
-32	136-0763-00			2	.SKT,PL-IN ELEK:26 LINE CONT IMPD HYBRID	00779	ORDER BY DESCR

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
3-					ATTACHING PARTS		
-33	210-0586-00			4	.NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	78189	211-041800-00
					END ATTACHING PARTS		
-34	----- -----			2	.ATTENUATOR,VAR:PRGM 1X-100X,10DB,CH1		
					.(SEE A10AT300,AT400 REPL)		
					ATTACHING PARTS		
-35	211-0304-00			4	.SCR,ASSEM WSHR:4-40 X 0.312,PNH,STL,T9 TORX	01536	ORDER BY DESCR
					END ATTACHING PARTS		
-36	351-0677-00	B010100	B011482	2	.GUIDE,MAG CATCH:	80009	351-0677-00
	351-0677-01	B011483		2	.GUIDE,MAG CATCH:BLACK,PLOYCARBONATE	80009	351-0677-01
-37	136-0252-07			32	.SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
-38	361-0382-00			6	.SPACER,PB SW:0.275 L,BROWN POLYCARBONATE	80009	361-0382-00
-39	214-0973-00			1	.HEAT SINK,XSTR:TO-92,CU BE CD PL	80009	214-0973-00

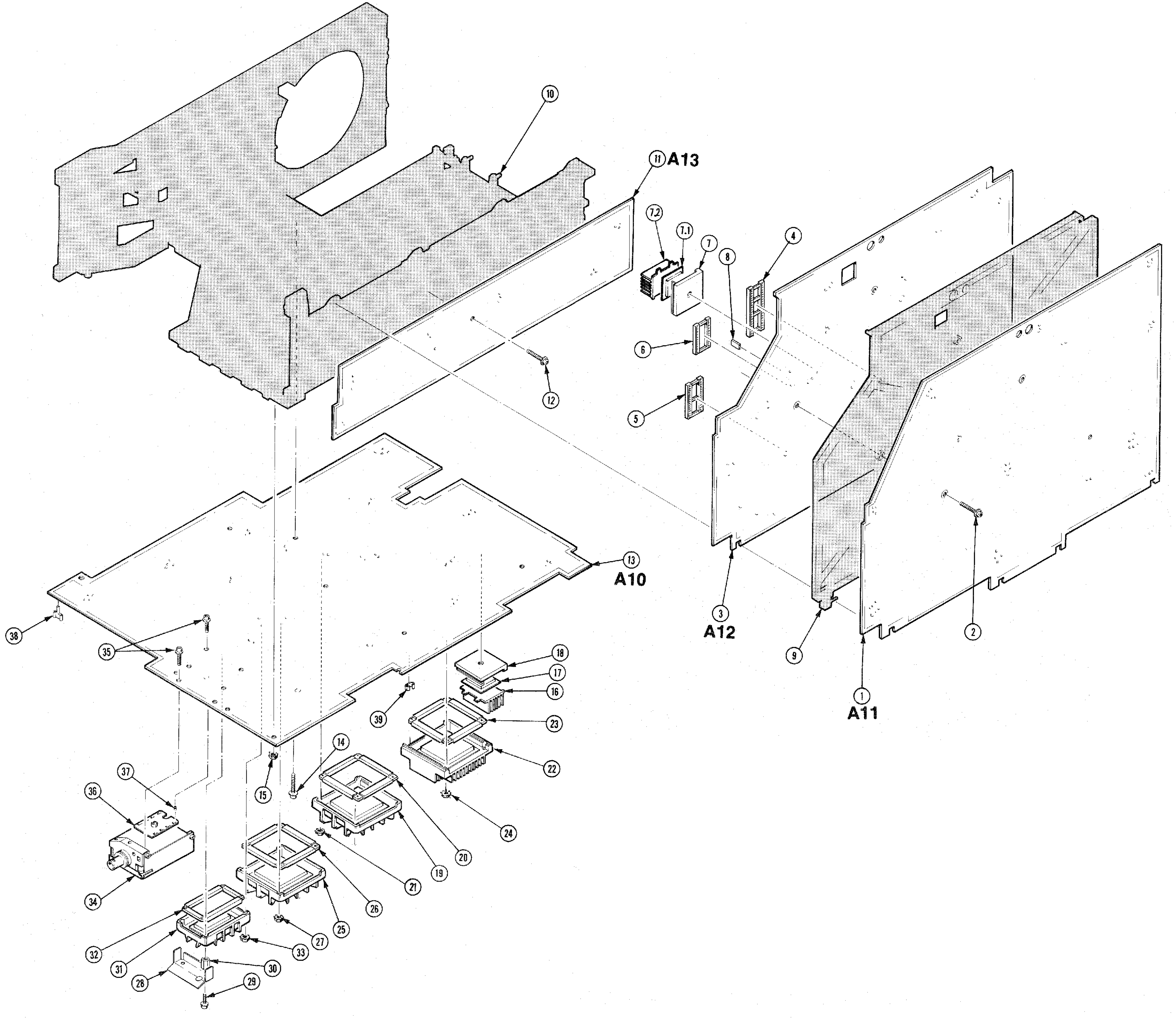


FIG. 3 CIRCUIT BOARDS

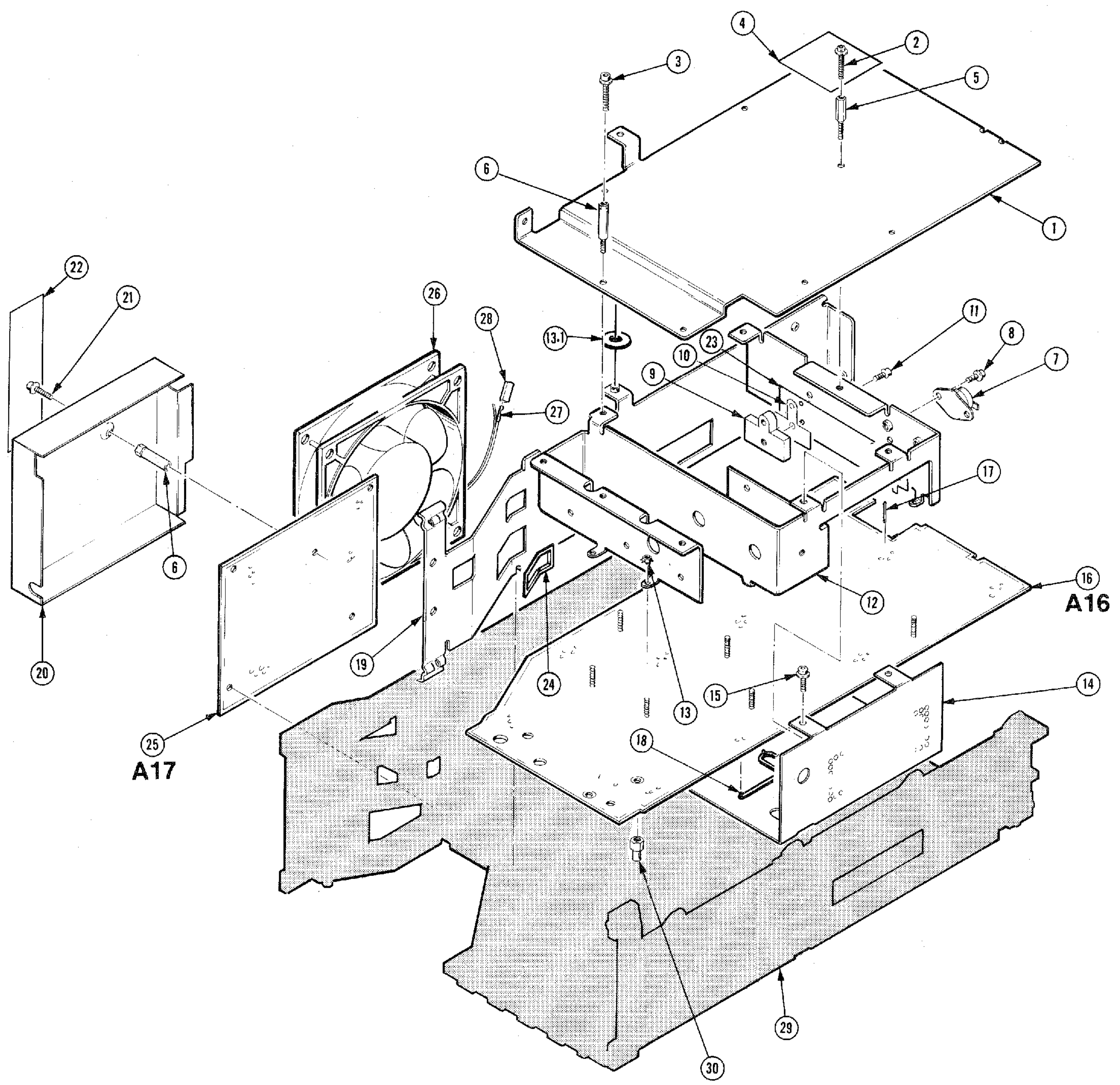


FIG. 4 LV, HV PWR SUPPLY

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
4-1	337-3163-00	B010100	B013150	1	SHIELD,ELEC:LOW VOLTAGE POWER SUPPLY	80009	337-3163-00
	337-3163-01	B013151		1	SHIELD,ELEC:LV,UPPER	80009	337-3163-01
					ATTACHING PARTS		
-2	211-0730-00			1	SCR,ASSEM WSHR:6-32 X 0.375,PNH,STL,T15	80009	211-0730-00
-3	211-0730-00			1	SCR,ASSEM WSHR:6-32 X 0.375,PNH,STL,T15	80009	211-0730-00
					END ATTACHING PARTS		
-4	334-4759-00			1	MARKER,IDENT:MKD SHIELDS INVERTER	80009	334-4759-00
-5	129-0473-00	B010100	B013150	1	SPACER,POST:0.640 L,6-32,STL,0.250 HEX	80009	129-0473-00
	129-0474-00	B013151		1	SPACER,POST:0.92 L,0.24 DIA STEEL,0.250HEX	80009	129-0474-00
-6	129-0474-00			2	SPACER,POST:0.92 L,0.24 DIA STEEL,0.250HEX	80009	129-0474-00
-7	----- -----			1	SWITCH,THRMSTC:NC,OPEN 83.3,CL 66.7,10A (SEE A16S1020 REPL)		
					ATTACHING PARTS		
-8	211-0730-00			2	SCR,ASSEM WSHR:6-32 X 0.375,PNH,STL,T15	80009	211-0730-00
					END ATTACHING PARTS		
-9	343-0527-00			7	RETAINER,XSTR:POLYCARBONATE	80009	343-0527-00
-10	342-0676-00			7	INSULATOR,XSTR:SILICON RUBBER,0.006 THK	80009	342-0676-00
					ATTACHING PARTS		
-11	211-0730-00			7	SCR,ASSEM WSHR:6-32 X 0.375,PNH,STL,T15	80009	211-0730-00
					END ATTACHING PARTS		
-12	407-2843-00	B010100	B013150	1	BRACKET,XSTR:ALUMINUM	80009	407-2843-00
	407-2843-01	B013151		1	BRACKET,XSTR:ALUMINUM	80009	407-2843-01
					ATTACHING PARTS		
-13	210-0586-00			7	NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	78189	211-041800-00
					END ATTACHING PARTS		
-13.1	210-0917-00	B010440	B012056	1	WASHER,FLAT:0.191 ID X 0.625 OD X 0.025 (STANDARD)	86928	ORDER BY DESCR
	210-0917-00	B010440	B012304	1	WASHER,FLAT:0.191 ID X 0.625 OD X 0.025 (OPTION 05)	86928	ORDER BY DESCR
-14	337-3175-00	B010100	B013150	1	SHIELD,ELEC:LV,LOWER	80009	337-3175-00
					ATTACHING PARTS		
-15	211-0730-00			2	SCR,ASSEM WSHR:6-32 X 0.375,PNH,STL,T15	80009	211-0730-00
					END ATTACHING PARTS		
-16	----- -----			1	CIRCUIT BD ASSY:LV PWR SPLY (SEE A16 REPL)		
-17	131-0608-00			1	.TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
-18	361-1346-00	B010100	B013150	1	.SPACER,CKT BD:0.25 SPACING,POLYCARBONATE	80009	361-1346-00
-19	441-1573-00	B010100	B013150	1	CHASSIS,SCOPE:CENTER	80009	441-1573-00
	441-1573-01	B013151		1	CHASSIS,SCOPE:CENTER	TK1285	ORDER BY DESCR
-20	337-1925-00			1	SHIELD,ELEC:CIRCUIT BOARD	80009	337-1925-00
					ATTACHING PARTS		
-21	211-0730-00			1	SCR,ASSEM WSHR:6-32 X 0.375,PNH,STL,T15	80009	211-0730-00
					END ATTACHING PARTS		
-22	334-5583-00			1	MARKER,IDENT:MKD CAUTION HIGH VOLTAGE	80009	334-5583-00
-23	337-3196-00			1	SHIELD,ELEC:FARADAY,POLYMIDE	80009	337-3196-00
-24	348-0897-00			1	GROMMET,PLASTIC:1.534 ID,BLACK,RECTANGULAR	80009	348-0897-00
-25	----- -----			1	CIRCUIT BD ASSY:HV (SEE A17 REPL)		
-26	----- -----			1	FAN,TUBEAXIAL:12V,1.72 W,42 CFM W/CONN (SEE B1000, CHASSIS PARTS, REPL)		
-27	131-0707-00			2	.CONTACT,ELEC:22-26 AWG,BRS,CU BE GLD PL	22526	47439-000
-28	204-0805-00			1	.CONN BODY,PLUG:2 CONTACTS,SINGLE ROW	80009	204-0805-00
-29	----- -----			1	CHASSIS,SCOPE:MAIN (SEE FIGURE 2)		
-30	129-1044-00			1	SPACER,POST:0.575 L,6-32 INT THRU,STL	80009	129-1044-00

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
5-							
					STANDARD ACCESSORIES		
-1	016-0692-00			1	POUCH,ACCESSORY:	80009	016-0692-00
-2	386-4849-00			1	PLATE,MOUNTING:ACCESSORY POUCH,ALUMINUM	80009	386-4849-00
-3	378-0199-03			1	FILTER,LT,CRT:BLUE,3.415 X 4.105 X 0.03	TK1634	378019903
	378-0199-04			1	FILTER,LT,CRT:BLUE,4.105 X 3.415 X 0.03 THK	80009	378-0199-04
	378-0199-05			1	FILTER,LT,CRT:BLUE,4.105 X 3.415 X 0.03 THK	80009	378-0199-05
	378-0208-00			1	FILTER,LT,CRT:CLEAR,4.105 X 3.415,PC	80009	378-0208-00
-4	159-0098-00	B010100	B010184	1	FUSE,CARTRIDGE:DIN,1.6A	71400	GDB 1.6
	159-0014-00	B010185		1	FUSE,CARTRIDGE:3AG,5A,250V,0.8SEC	71400	MTH-CW-5
-5	200-2742-02	B010100	B013567	1	COVER,PROT:FRONT PANEL	80009	200-2742-02
	200-3199-01	B013568		1	COVER,FRONT:ABS (2430 ONLY)	TK2165	ORDER BY DESCR
	200-2742-02	B010100	B010126	1	COVER,PROT:FRONT PANEL	80009	200-2742-02
	200-3199-01	B010127		1	COVER,FRONT:ABS (2430M ONLY)	TK2165	ORDER BY DESCR
-6	161-0104-00			1	CABLE ASSY,PWR,:3 WIRE,98.0 L,W/RTANG CONN (STANDARD ONLY)	16428	CH8352, FH-8352
-7	343-1213-00			1	CLAMP,PWR CORD:POLYMIDE	80009	343-1213-00
-8	161-0104-06			1	CABLE ASSY,PWR,:3 X 0.75MM SQ,220V,98.0 L (OPTION A1 ONLY)	S3109	ORDER BY DESCR
-9	161-0104-07			1	CABLE ASSY,PWR,:3 X 0.75MM SQ,240V,98.0 L (OPTION A2 ONLY)	TK1373	A25UK-RA
-10	161-0104-05			1	CABLE ASSY,PWR,:3,18 AWG,240V,98.0 L (OPTION A3 ONLY)	S3109	ORDER BY DESCR
-11	161-0104-08			1	CABLE ASSY,PWR,:3,18 AWG,240V,98.0 L (OPTION A4 ONLY)	70903	ORDER BY DESCR
-12	161-0167-00			1	CABLE ASSY,PWR,:3.0 X 0.75,6A,240V,2.5M L (OPTION A5 ONLY)	S3109	ORDER BY DESCR
	----- -----			2	PROBE,VOLTAGE:P6131,10X,1.3M W/ACCESSORIES		
	----- -----			4	PROBE,VOLTAGE:P6131,10X,1.3M W/ACCESSORIES (OPTION 22 ONLY)		
	016-0537-00			1	POUCH,ACCESSORY:6 IN X 9 IN W/ZIPPER	05006	ZIP-6X9ID
	070-4918-00			1	MANUAL,TECH:OPERATORS,2430	80009	070-4918-00
	070-5497-00			1	MANUAL,TECH:REFERENCE,2430	80009	070-5497-00
	070-5705-00			1	MANUAL,TECH:INSTR,2430	80009	070-5705-00
	070-4366-00	B010100	B013408	1	SHEET,TECHNICAL:INSTR,016-0691-00 RACK	80009	070-4366-00
	070-5859-01	B013409		1	SHEET,TECHNICAL:INSTR,2400 SERIES	80009	070-5859-01
					OPTIONAL ACCESSORIES		
	016-0180-00			1	VISOR,CRT:FOLDING	TK2165	ORDER BY DESCR
	016-0566-00			1	VISOR,CRT:	TK2165	ORDER BY DESCR
	016-0691-02			1	RACK MOUNT KIT:	80009	016-0691-02
	016-0792-01			1	CASE,CARRYING:24.5 X 16.5 X 11.5	TK1336	ORDER BY DESCR
	070-4917-00			1	MANUAL,TECH:SERVICE,2430	80009	070-4917-00
	346-0199-00			1	STRAP,CARRYING:MKD TEKTRONIX	80009	346-0199-00
	016-0825-00	B010100	B013408	1	RACK MOUNT KIT:	80009	016-0825-00
	016-0825-01	B013409		1	RACK MOUNT KIT: 2430/2445A/2465A/2467	80009	016-0825-01

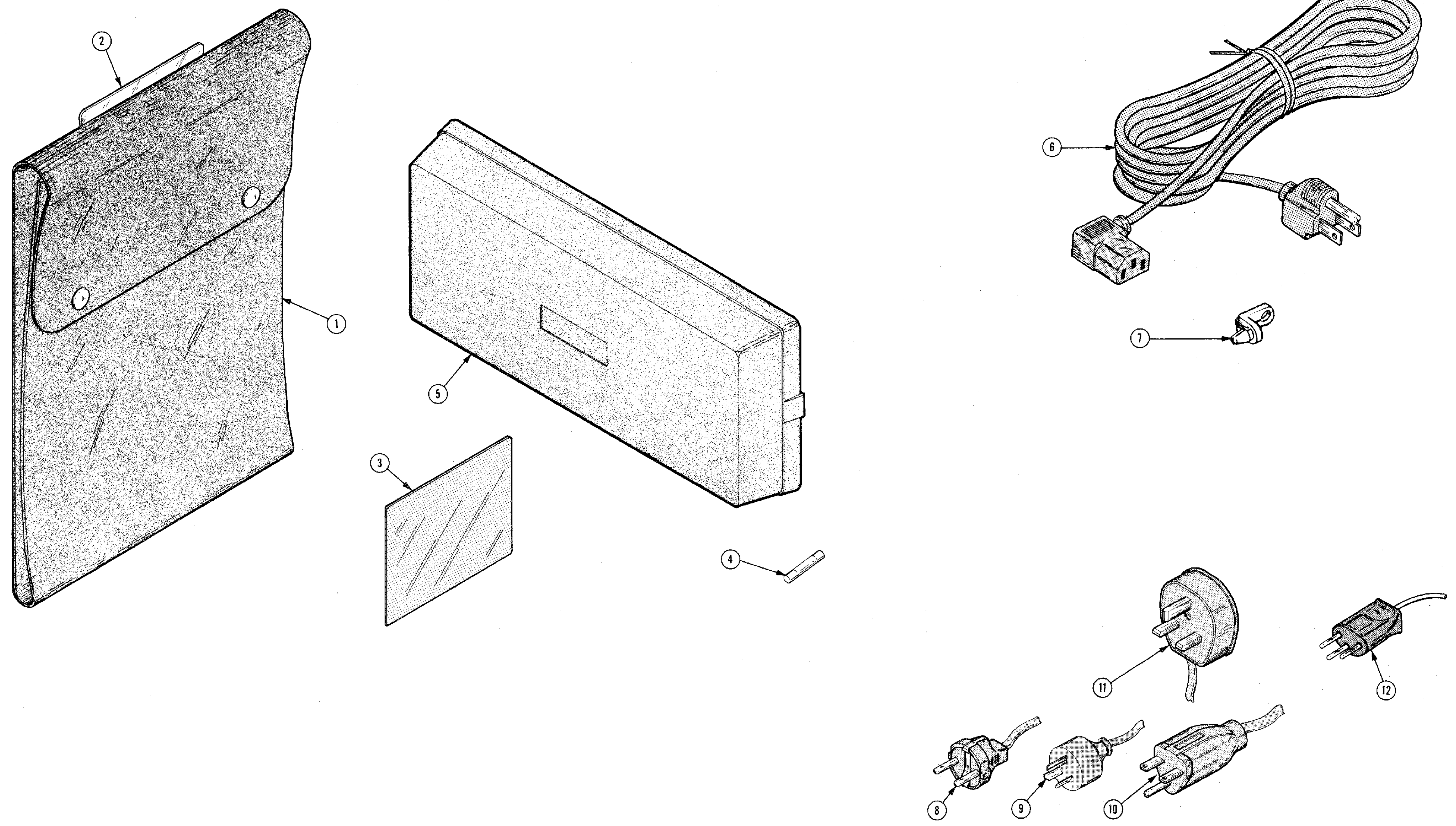


FIG. 5 ACCESSORIES

INDEX

Tektronix®

REVISION INFORMATION

Manual Part No. 070-4917-00 First Printing May 1986

Product: 2430 Service Manual Revised September 1994

Manual Insert Status

DATE	CHANGE REFERENCE	STATUS
5-AUG-87	M63255	Effective
2-SEP-87	M64144	Effective
2-OCT-87	M64299	Effective
18-DEC-87	C7/1287	Effective
8-SEP-88	C8/0988	Effective
17-NOV-88	C9/1188	Effective
23-OCT-91	M71475	Effective

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MANUAL CHANGE INFORMATION

Date: 08-05-87 Change Reference: M63255

Product: 2430 SERVICE Manual Part No.: 070-4917-00

DESCRIPTION Product Group 37

EFFECTIVE SERIAL NUMBER: B014161

REPLACEABLE ELECTRICAL PARTS LIST CHANGES

ADD:

A10R809	313-1471-00	RES,FXD,FILM:470 OHM,5%,0.2W

CHANGE TO:

A10R142	315-0100-00	RES,FXD,FILM:10 OHM,5%,0.25W
A10R269	315-0100-00	RES,FXD,FILM:10 OHM,5%,0.25W
A10R372	315-0391-00	RES,FXD,FILM:390 OHM,5%,0.25W
A10R375	315-0391-00	RES,FXD,FILM:390 OHM,5%,0.25W
A10R376	315-0201-00	RES,FXD,FILM:200 OHM,5%,0.25W
A10R377	315-0201-00	RES,FXD,FILM:200 OHM,5%,0.25W
A10R510	315-0100-00	RES,FXD,FILM:10 OHM,5%,0.25W
A10R531	315-0100-00	RES,FXD,FILM:10 OHM,5%,0.25W
A10R535	321-0292-00	RES,FXD,FILM:10.7K OHM,1%,0.125W
A10R536	321-1332-00	RES,FXD,FILM:28.4K OHM,1%,0.125W
A10R545	321-0292-00	RES,FXD,FILM:10.7K OHM,1%,0.125W
A10R635	321-1332-00	RES,FXD,FILM:28.4K OHM,1%,0.125W
A10R636	321-0292-00	RES,FXD,FILM:10.7K OHM,1%,0.125W
A10R640	321-1332-00	RES,FXD,FILM:28.4K OHM,1%,0.125W
A10R641	321-1332-00	RES,FXD,FILM:28.4K OHM,1%,0.125W
A10R642	321-0292-00	RES,FXD,FILM:10.7K OHM,1%,0.125W
A10R850	315-0100-00	RES,FXD,FILM:10 OHM,5%,0.25W
A10U350	165-2074-02	MICROCKT,HYBRID:CCD/DRIVER
A10U450	165-2074-02	MICROCKT,HYBRID:CCD/DRIVER

DESCRIPTION

DIAGRAM CHANGES

DIAGRAM ⟨5⟩ SYSTEM DAC & ACQ. CONTROL REG.

Change R142, R269, R531 and R850 (locations 2K, 1G, 2F, and 5E) to 10 Ω resistors.

DIAGRAM ⟨6⟩ SYSTEM DAC (cont) & AUX FRONT PANEL

Add R809 (location 6H) a 470 Ω resistor to the base of Q180 as shown below.

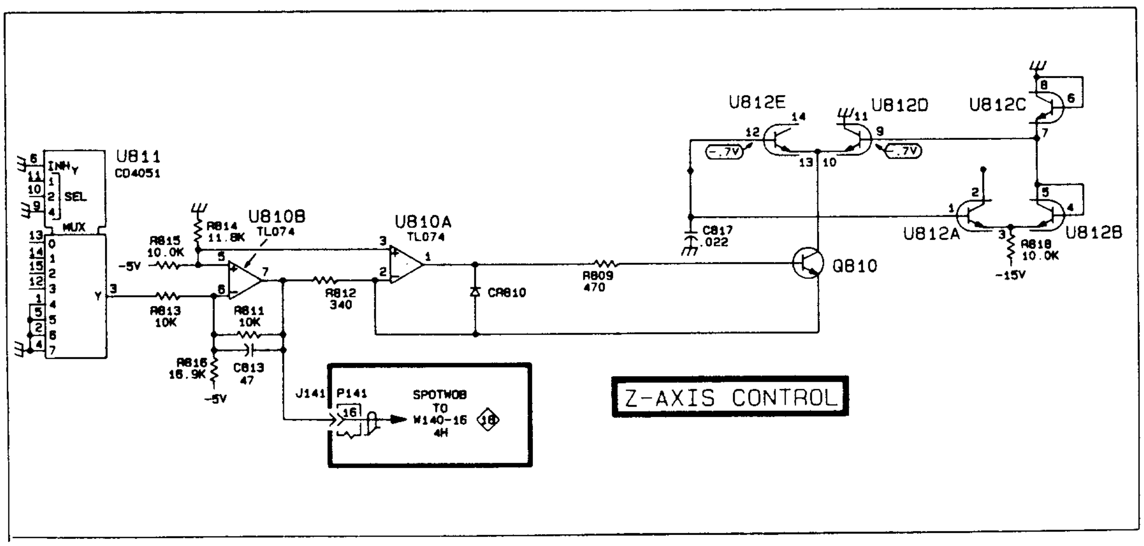

DIAGRAM ⟨9⟩ ATTENUATORS AND PREAMPS

Change R510 (location 2B) to a 10 Ω resistor.

DIAGRAM ⟨10⟩ PEAK DETECTORS & CCD/CLOCK DRIVERS

Change R372 and R375 (locations 5N and 3N) to 390 Ω resistors.

Change R376 and R377 (locations 3N and 5N) to 200 Ω resistors.

Change R535, R545, R636, and R642 (locations 4D, 2D, 6D, and 1D) to 10.7K Ω resistors.

Change R536, R635, R640, and R641 (locations 4D, 6D, 2D, and 1D) to 28.4K Ω resistors.

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MANUAL CHANGE INFORMATION

Date: 9-02-87 Change Reference: M64144

Product: 2430 SERVICE Manual Part No.: 070-4917-00

DESCRIPTION Product Group 37

EFFECTIVE SERIAL NUMBER: 2430 B014162

REPLACEABLE ELECTRICAL PARTS LIST CHANGES

CHANGE TO:

A10	670-8163-10	CIRCUIT BD ASSY:MAIN
A10R679	321-0222-00	RES,FXD,FILM:2K OHM,1%,0.125W (NOMINAL VALUE)
	321-0210-00	RES,FXD,FILM:1.5K OHM,1%,0.125W (TEST SELECTABLE)
A10R767	321-0222-00	RES,FXD,FILM:2K OHM,1%,0.125W (NOMINAL VALUE)
	321-0210-00	RES,FXD,FILM:1.5K OHM,1%,0.125W (TEST SELECTABLE)
A10R867	321-0222-00	RES,FXD,FILM:2K OHM,1%,0.125W (NOMINAL VALUE)
	321-0210-00	RES,FXD,FILM:1.5K OHM,1%,0.125W (TEST SELECTABLE)
A10R878	321-0222-00	RES,FXD,FILM:2K OHM,1%,0.125W (NOMINAL VALUE)
	321-0210-00	RES,FXD,FILM:1.5K OHM,1%,0.125W (TEST SELECTABLE)
A13	670-9749-01	CIRCUIT BD ASSY:SIDE
A18	670-7280-00	CIRCUIT BD ASSY:SCALE ILLUM

DIAGRAM ⟨14⟩ CCD OUTPUT

Change resistors R679 (location 6C), R767 (location 1B), R867 (location 3C), and R878 (location 7C) from 2.0K Ω to Test Selectable (SEL).

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MANUAL CHANGE INFORMATION

Date: 10-02-87 Change Reference: M64299

Product: 2430 Service Manual Part No.: 070-4917-00

DESCRIPTION Product Group 37

EFFECTIVE SERIAL NUMBER: 2430 B014162

REPLACEABLE ELECTRICAL PARTS LIST CHANGES

ADD:

A10C310	281-0909-00	CAP,FXD,CER DI:0.022UF,20%,50V
A10R310	313-1220-00	RES,FXD,FILM:22 OHM,5%,0.2W
A10W421	131-0566-00	BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L

CHANGE TO:

A10R379	321-0387-00	RES,FXD,FILM:105.0K OHM,1%,0.125W
A10U350	165-2074-03	MICROCKT,HYBRID:CCD/DRIVER
A10U450	165-2074-03	MICROCKT,HYBRID:CCD/DRIVER

REMOVE:

A10LR421	108-0284-00	COIL,RF:FIXED,97 NH

DIAGRAM CHANGES

DIAGRAM ⟨9⟩ ATTENUATORS AND PREAMPS

Change coil LR421 (location 2L) to wire W421 as shown below.

Add capacitor C310 and resistor R310, (location 2L), as shown below.

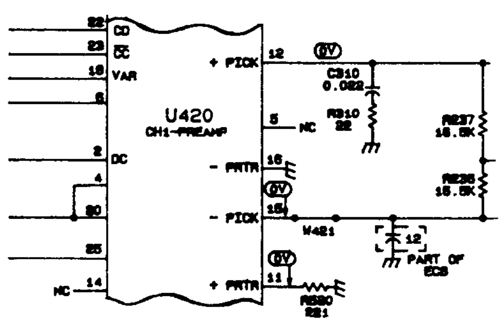

DIAGRAM ⟨10⟩ PEAK DETECTORS AND CCD/CLOCK DRIVERS

Change R379 (location 5M) to a 105.0K Ω resistor.

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MANUAL CHANGE INFORMATION

Date: 12-18-87 Change Reference: C7/1287

Product: 2430 Service Manual Part No.: 070-4917-00

DESCRIPTION Product Group 37

EFFECTIVE ALL SERIAL NUMBERS

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ADD the following note to step 7, Check Square-Wave Flatness (Video Option 05 only):

NOTE

For this step, use a PG 506 Calibration Generator (Item 2) listed in the equipment required at the beginning of "ADDITIONAL VERIFICATIONS AND CHECK" procedure.

Change part b to the following:

b. Connect the fast-rise, positive going square-wave output to the CH1 input connector via a 50-Ω cable and a 50-Ω terminator. The square wave should step from -1 V to 0 V.

Change part i and m to the following (20 mV was changed to 5 mV):

i. Set the CH2 VOLTS/DIV control to 5 mV.

m. Move the cable from the CH2 input connector to the CH1 input connector. Set the CH1 VOLTS/DIV control to 5 mV.

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MANUAL CHANGE INFORMATION

Date: 09-08-88

Change Reference: C8-0988

Product: 2430 SERVICE

Manual Part Number: 070-4917-00

DESCRIPTION

PRODUCT GROUP 37

EFFECTIVE ALL SERIAL NUMBERS

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Change steps 56 and 59 to read as follows:

56. CHECK—That the readout indicates about 10 V.

59. CHECK—That the readout indicates about 25 V^2.

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MANUAL CHANGE INFORMATION

Date: 11-17-88 Change Reference: C9/1188

Product: 2430 Service Manual Part Number: 070-4917-00

DESCRIPTION PRODUCT GROUP 37

EFFECTIVE ALL SERIAL NUMBERS

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Add the following front panel setup to step 6.

Select COUPLING/INVERT
Set: 50 Ω ON| OFF OFF

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MANUAL CHANGE INFORMATION

Date: 23-OCT-91 **Change Reference:** M71475

Product: 2430 Service **Manual Part No.:** 070-4917-00

DESCRIPTION **Product Group 37**

EFFECTIVE SERIAL NUMBERS: B014161 and above

REPLACEABLE ELECTRICAL PARTS LIST CHANGES

CHANGE:

A16	670-9902-05	CIRCUIT BD ASSY:LV PWR SPLY
A16Q421	151-1195-00	TRANSISTOR,PWR:MOS,N-CH,500V,8.0A
A16Q423	151-1195-00	TRANSISTOR,PWR:MOS,N-CH,500V,8.0A
A16R324	315-0750-00	RES,FXD,FILM:75 OHM,5%,0.25W
A16R624	315-0750-00	RES,FXD,FILM:75 OHM,5%,0.25W
A17	670-9748-02	CIRCUIT BD ASSY:HV POWER SPLY
A17R162	313-1272-00	RES,FXD,FILM:2.7KOHM,5%,0.2W

DIAGRAM CHANGES

Diagram ⟨22⟩ **LV POWER SUPPLY**

Change the value of resistors R324 and R624 (location 1F) to 75 Ω.